0.9 V to 2.5 V, 55 mΩ Load Switch in WCSP4

DESCRIPTION

SiP32451, SiP32452 and SiP32453 are n-channel integrated high side load switches that operate from 0.9 V to 2.5 V input voltage range.

SiP32451, SiP32452 and SiP32453 have low input logic control threshold that can interface with low voltage control GPIO directly without extra level shift or driver. There is a pull down at this EN logic control pin.

Turn on time is fast, less than 25 µs typically for input voltage of 1.2 V or higher. SiP32451 and SiP32452 have fast turn off delay time of less than 1 µs while SiP32453 features a guaranteed turn off delay of greater than 30 µs, typically 90 µs.

SiP32451 features an output discharge for fast turn off.

SiP32451, SiP32452 and SiP32453 are available in compact wafer level CSP package, WCSP4 0.8 mm x 0.8 mm with 0.4 mm pitch.

FEATURES

- Low input voltage, 0.9 V to 2.5 V
- Low R_{ON}, 55 mΩ typical
- Fast turn on time
- Low logic control with hysteresis
- Reverse current blocking when disabled
- Integrated pull down at EN pin
- Output discharge (SiP32451)
- 4 bump WCSP 0.8 mm x 0.8 mm with 0.4 mm pitch package
- Material categorization: For definitions of compliance please see www.vishay.com/doc?9991

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Battery operated devices
- Smart phones
- GPS and PMP
- Computer
- Medical and healthcare equipment
- Industrial and instrument
- Cellular phones and portable media players
- Game console

TYPICAL APPLICATION CIRCUIT

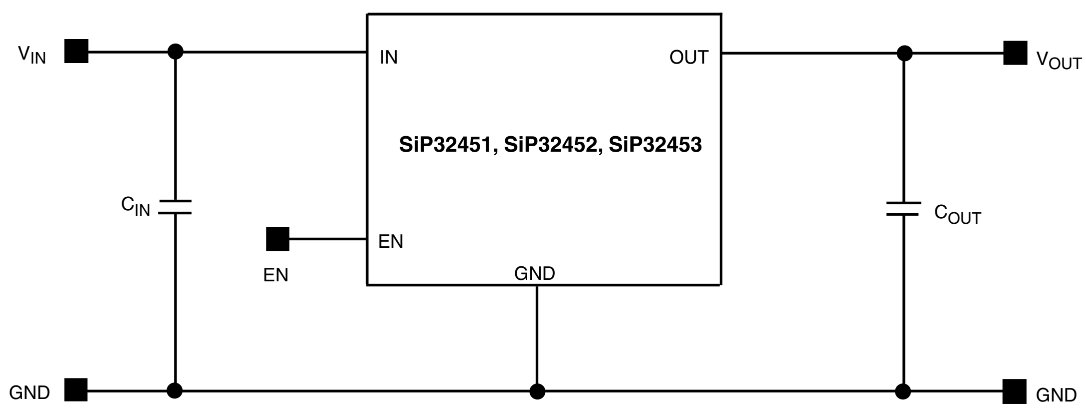


Figure 1 - SiP32451, SiP32452, and SiP32453 Typical Application Circuit

ORDERING INFORMATION

Temperature Range	Package	Marking	Part Number
- 40 °C to 85 °C	WCSP4: 4 Bumps (2 x 2, 0.4 mm pitch, 208 µm bump height, 0.8 mm x 0.8 mm die size)	AA	SiP32451DB-T2-GE1
		AB	SiP32452DB-T2-GE1
		AC	SiP32453DB-T2-GE1

Note:
GE1 denotes halogen-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Supply Input Voltage (V_{IN})	- 0.3 to 2.75	V
Enable Input Voltage (V_{EN})	- 0.3 to 2.75	
Output Voltage (V_{OUT})	- 0.3 to 2.75	
Maximum Continuous Switch Current ($I_{max.}$)	1.2	A
Maximum Pulsed Current (I_{DM}) V_{IN} (Pulsed at 1 ms, 10 % duty cycle)	2	
ESD Rating (HBM)	4000	V
Junction Temperature (T_J)	- 40 to 150	°C
Thermal Resistance (θ_{JA})[a]	280	°C/W
Power Dissipation (P_D)[a]	196	mW

Notes:
a. Device mounted with all leads and power pad soldered or welded to PC board.
b. Derate 3.6 mW/°C above T_A = 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
Input Voltage Range (V_{IN})	0.9 to 2.5	V
Operating Junction Temperature Range	- 40 to 125	°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 1 V, T_A = - 40 °C to 85 °C (Typical values are at T_A = 25 °C)		Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Operating Voltage[c]	V_{IN}			0.9	-	2.5	V
Quiescent Current	I_Q	V_{IN} = 1.2 V, V_{EN} = V_{IN}, OUT = open		-	10	15	µA
		V_{IN} = 2.5 V, V_{EN} = V_{IN}, OUT = open		-	34	60	
Off Supply Current	$I_{Q(off)}$	SiP32451	EN = GND, OUT = open	-	-	30	
		SiP32452, SiP32453		-	-	1	
Off Switch Current	$I_{DS(off)}$	EN = GND, OUT = 0 V		-	-	30	
Reverse Blocking Current	I_{RB}	V_{OUT} = 2.5 V, V_{IN} = 0.9 V, V_{EN} = 0 V		-	0.001	10	
On-Resistance	$R_{DS(on)}$	V_{IN} = 1 V, I_L = 200 mA, T_A = 25 °C		-	56	65	mΩ
		V_{IN} = 1.2 V, I_L = 200 mA, T_A = 25 °C		-	55	65	
		V_{IN} = 1.8 V, I_L = 200 mA, T_A = 25 °C		-	54	65	
		V_{IN} = 2.5 V, I_L = 200 mA, T_A = 25 °C		-	54	65	
On-Resistance Temp.-Coefficient	TC_{RDS}			-	3900	-	ppm/°C
Output Pulldown Resistance	R_{PD}	V_{EN} = 0 V, T_A = 25 °C (SiP32451 only)		-	425	550	Ω
EN Input Low Voltage[c]	V_{IL}	V_{IN} = 1 V		-	-	0.1	V
EN Input High Voltage[c]	V_{IH}	V_{IN} = 2.5 V		1.5	-	-	
EN Input Leakage	I_{EN}	V_{IN} = 2.5 V, V_{EN} = 0 V		-	-	1	µA
		V_{IN} = 2.5 V, V_{EN} = 2.5 V		-	10	15	
Output Turn-On Delay Time	$t_{d(on)}$	V_{IN} = 1.2 V	R_{LOAD} = 10 Ω, C_L = 0.1 µF, T_A = 25 °C	-	0.4	1	µs
		V_{IN} = 2.5 V		-	0.05	1	
Output Turn-On Rise Time	t_r	V_{IN} = 1.2 V		10	20	30	
		V_{IN} = 2.5 V		5	9.8	20	
Output Turn-Off Delay Time	$t_{d(off)}$	SiP32451, SiP32452 V_{IN} = 1.2 V		-	0.25	1	
		SiP32451, SiP32452 V_{IN} = 2.5 V		-	0.15	1	
		SiP32453, V_{IN} = 1.2 V		30	98	150	
		SiP32453, V_{IN} = 2.5 V		30	86	150	

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. For V_{IN} outside this range consult typical EN threshold curve.

PIN CONFIGURATION

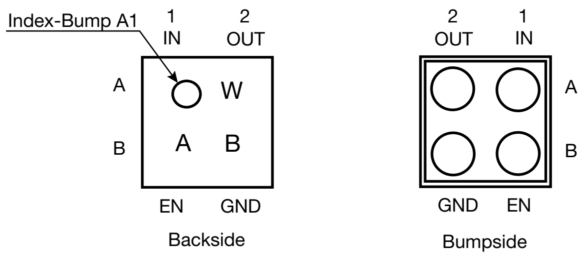


Figure 2 - WCSP4 2 x 2 Package

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
A1	IN	This pin is the n-channel MOSFET drain connection. Bypass to ground through a 4.7 µF capacitor.
A2	OUT	This pin is the n-channel MOSFET source connection. Bypass to ground through a 0.1 µF capacitor.
B1	EN	Enable input
B2	GND	Ground connection

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

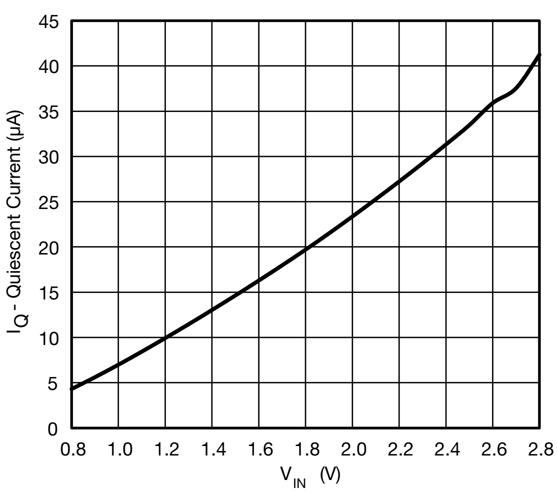


Figure 3 - Quiescent Current vs. Input Voltage

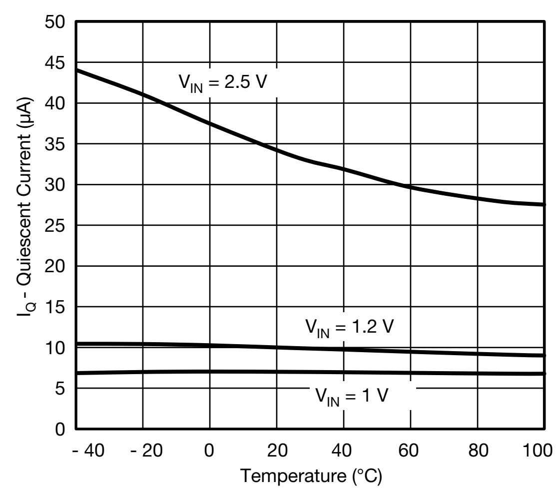


Figure 5 - Quiescent Current vs. Temperature

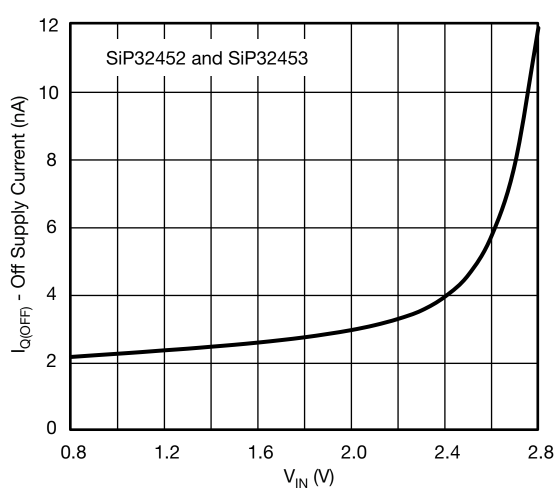


Figure 4 - Off Supply Current vs. Input Voltage

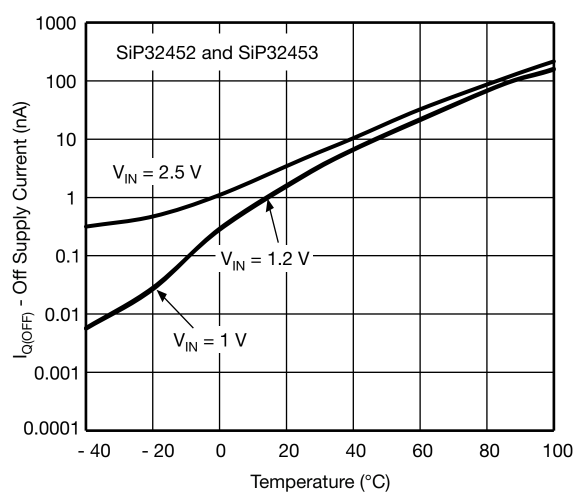


Figure 6 - Off Supply Current vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

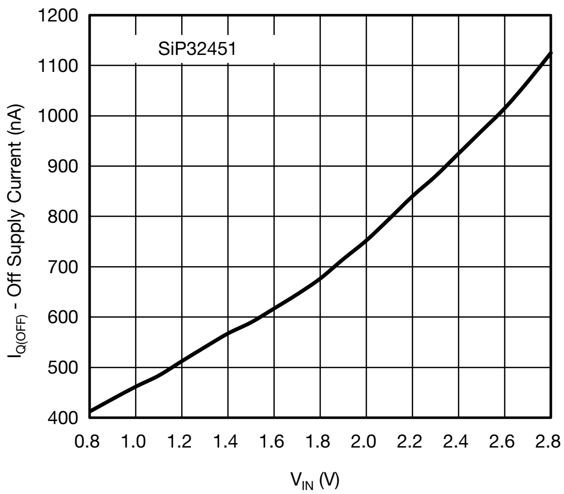


Figure 7 - Off Supply Current vs. Input Voltage

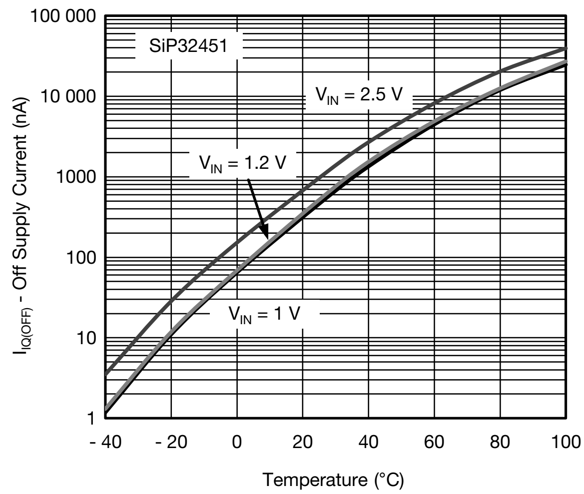


Figure 10 - Off Supply Current vs. Temperature

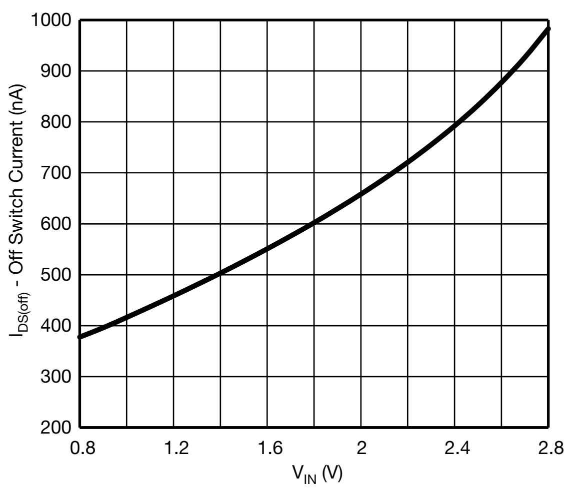


Figure 8 - Off Switch Current vs. Input Voltage

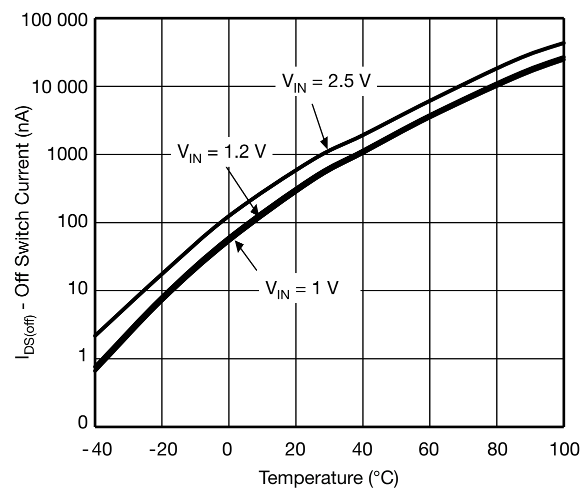


Figure 11 - Off Switch Current vs. Temperature

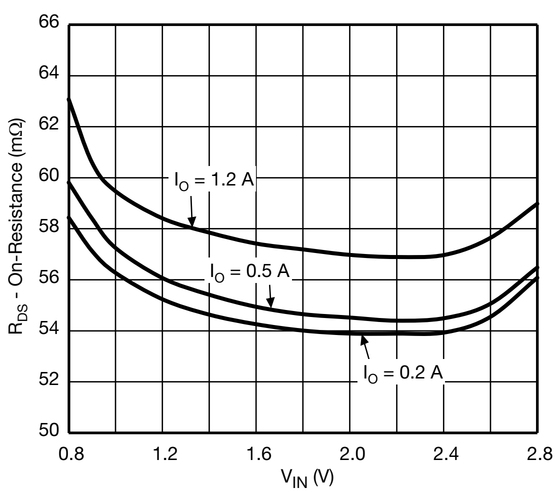


Figure 9 - $R_{DS(on)}$ vs. V_{IN}

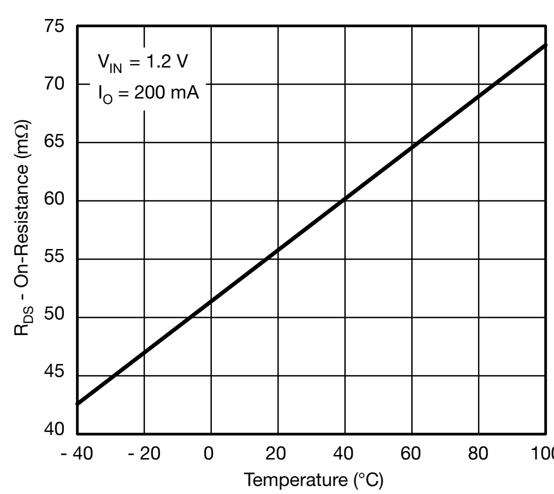


Figure 12 - $R_{DS(on)}$ vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

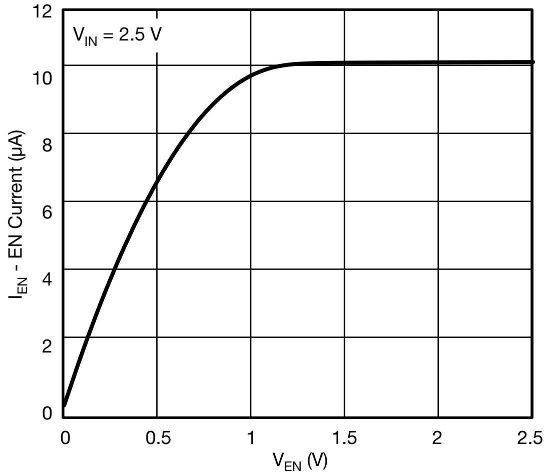


Figure 13 - I_{EN} vs. V_{EN}

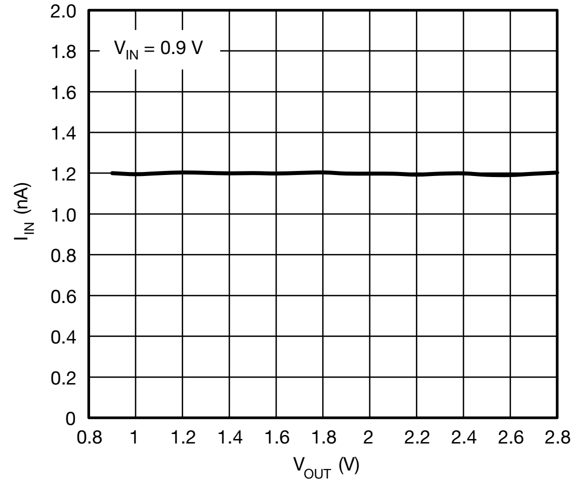


Figure 16 - Reverse Blocking Current vs. Output Voltage

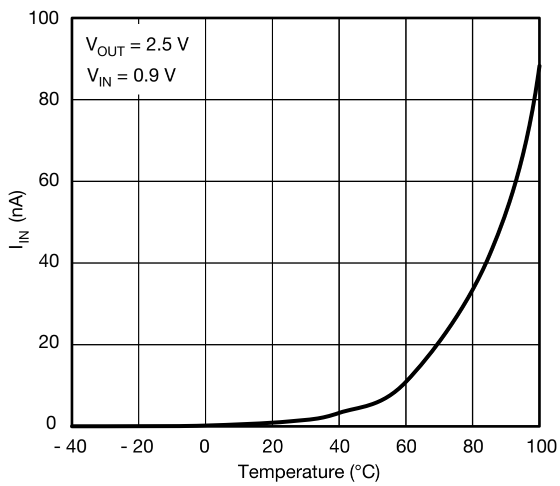


Figure 14 - Reverse Blocking Current vs. Temperature

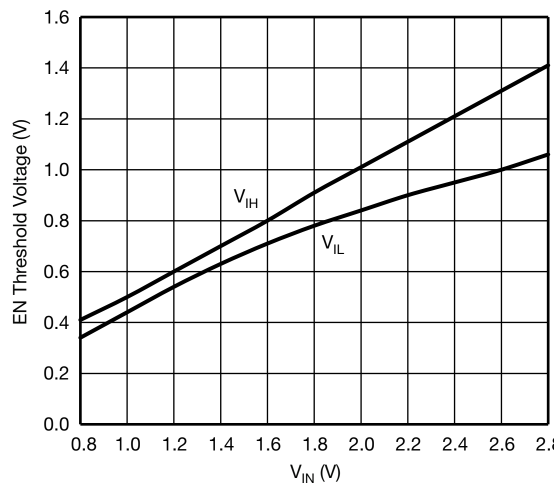


Figure 17 - EN Threshold Voltage vs. Input Voltage

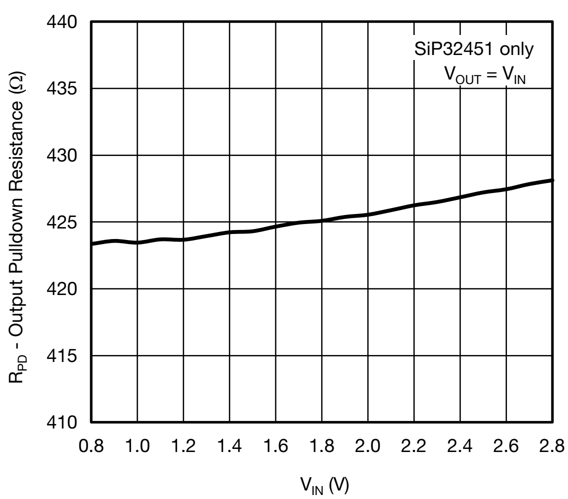


Figure 15 - Output Pulldown Resistance vs. Input Voltage

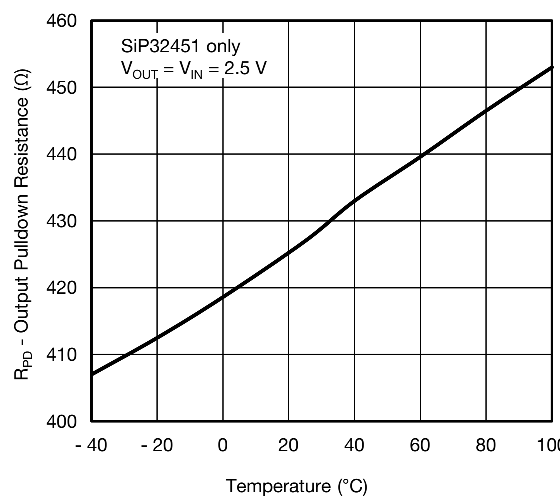


Figure 18 - Output Pulldown Resistance vs. Temperature

TYPICAL CHARACTERISTICS (internally regulated, 25 °C, unless otherwise noted)

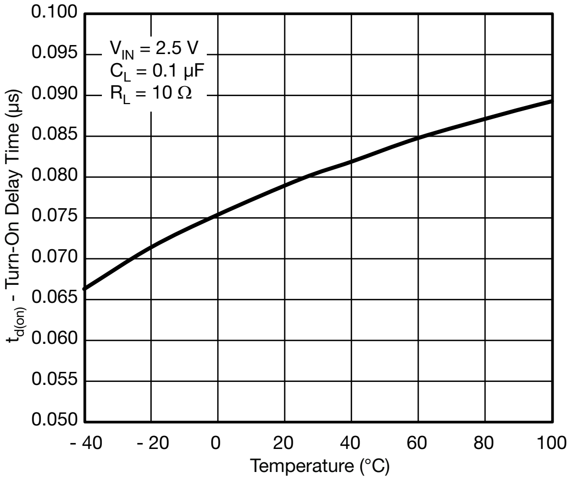


Figure 19 - Turn-On Delay Time vs. Temperature

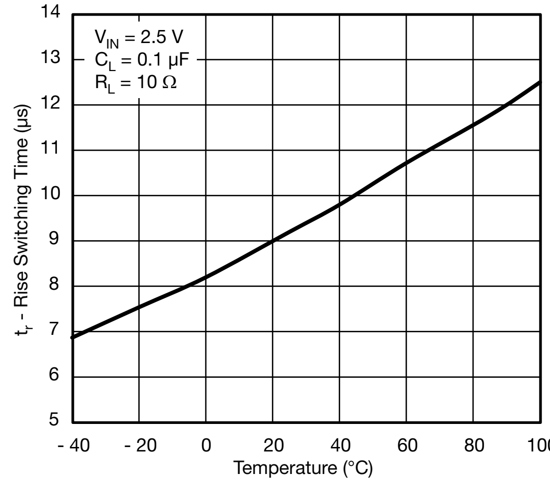


Figure 21 - Rise Time vs. Temperature

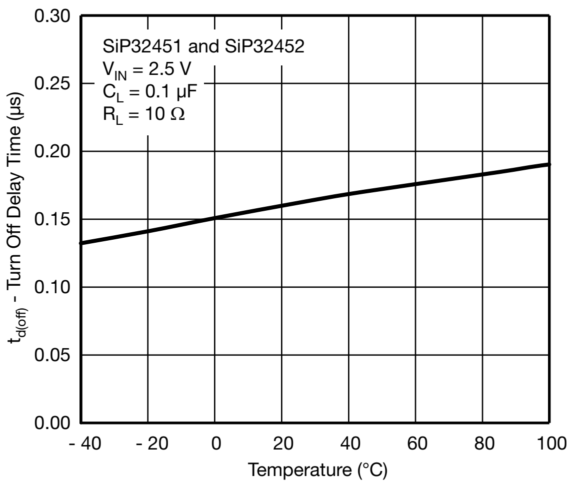


Figure 20 - Turn-Off Delay Time vs. Temperature

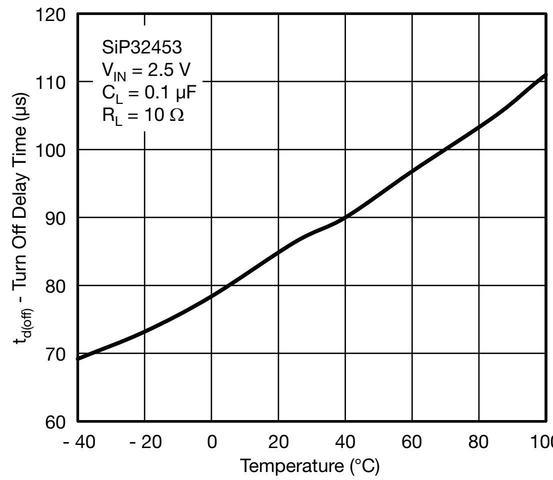


Figure 22 - Turn-Off Delay Time vs. Temperature

TYPICAL WAVEFORMS

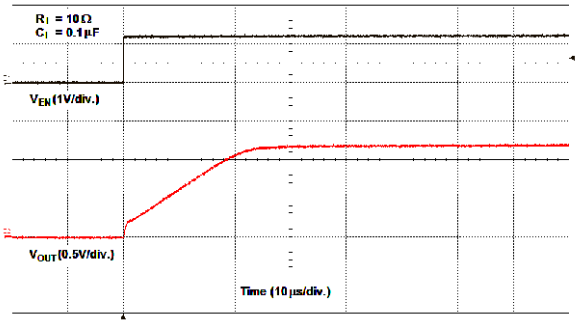


Figure 23 - Turn-On Time (V_{IN} = 1.2 V)

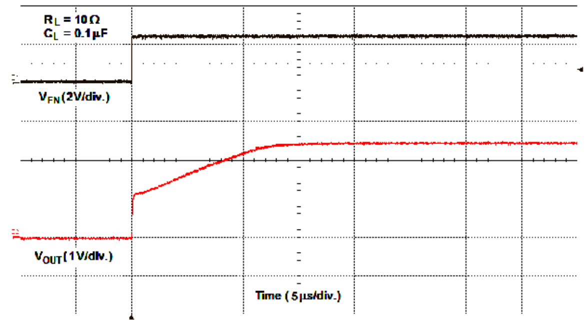


Figure 26 - Turn-On Time (V_{IN} = 2.5 V)

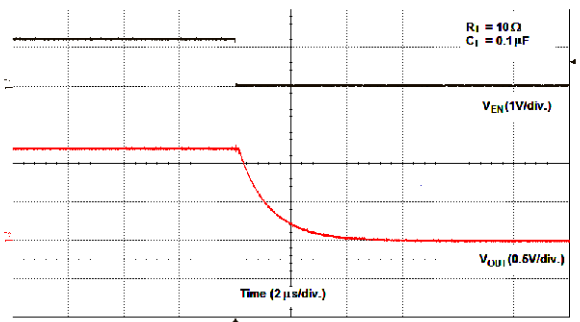


Figure 24 - SiP32451 and SiP32452 Turn-Off Time (V_{IN} = 1.2 V)

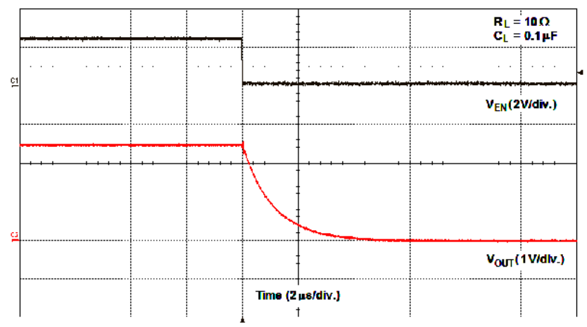


Figure 27 - SiP32451 and SiP32452 Turn-Off Time (V_{IN} = 2.5 V)

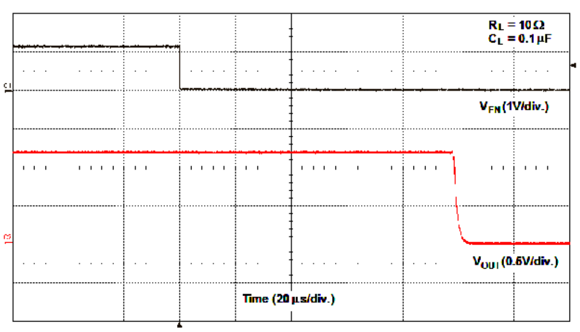


Figure 25 - SiP32453 Turn-Off Time (V_{IN} = 1.2 V)

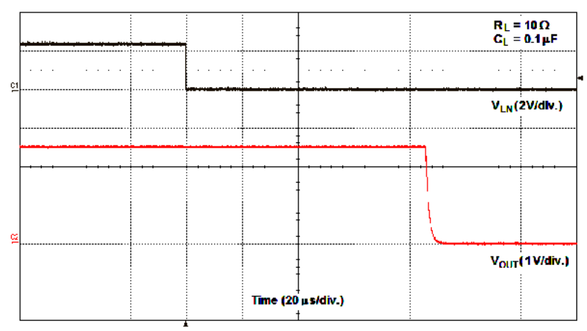


Figure 28 - SiP32453 Turn-Off Time (V_{IN} = 2.5 V)

BLOCK DIAGRAM

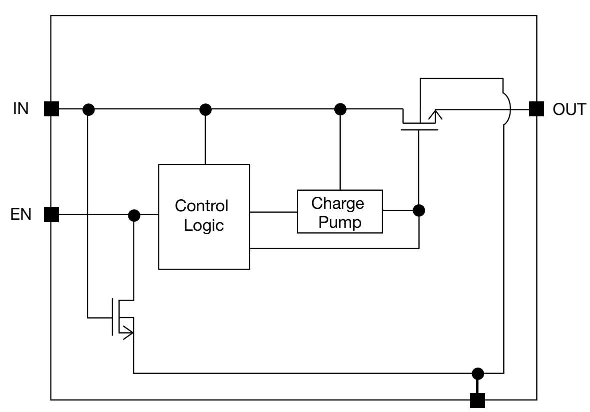


Figure 29 - Functional Block Diagram

DETAILED DESCRIPTION

SiP32451, SiP32452 and SiP32453 are n-channel power MOSFET designed as high side load switch. Once enable the device charge pumps the gate of the power MOSFET to a constant gate to source voltage for fast turn on time. The mostly constant gate to source voltage keeps the on resistance low through out the input voltage range. When disable, the SiP32451 and SiP32452 pull the gate of the output n-channel low right away for a fast turn off delay while there is a build-in turn off delay for the SiP32453. The SiP32451 especially features a output discharge circuit to help discharge the output capacitor. The turn off delay for the SiP32453 is guaranteed to be at least 30 µs. Because the body of the output n-channel is always connected to GND, it prevents the current from going back to the input in case the output voltage is higher than the output.

APPLICATION INFORMATION

Input Capacitor

While a bypass capacitor on the input is not required, a 4.7 µF or larger capacitor for C_{IN} is recommended in almost all applications. The bypass capacitor should be placed as physically close as possible to the input pin to be effective in minimizing transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 0.1 µF capacitor across V_{OUT} and GND is recommended to insure proper slew operation. There is inrush current through the output MOSFET and the magnitude of the inrush current depends on the output capacitor, the bigger the C_{OUT} the higher the inrush current. There are no ESR or capacitor type requirement.

Enable

The EN pin is compatible with CMOS logic voltage levels. It requires at least 0.1 V or below to fully shut down the device and 1.5 V or above to fully turn on the device.

Protection Against Reverse Voltage Condition

SiP32451, SiP32452 and SiP32453 can block the output current from going to the input in case where the output voltage is higher than the input voltage when the main switch is off.

Thermal Considerations

These devices are designed to maintain a constant output load current. Due to physical limitations of the layout and assembly of the device the maximum switch current is 1.2 A as stated in the Absolute Maximum Ratings table. However, another limiting characteristic for the safe operating load current is the thermal power dissipation of the package. To obtain the highest power dissipation (and a thermal resistance of 280 °C/W) the device should be connected to a heat sink on the printed circuit board.

The maximum power dissipation in any application is dependant on the maximum junction temperature, $T_{J(max.)}$ = 125 °C, the junction-to-ambient thermal resistance, θ_{J-A} = 280 °C/W, and the ambient temperature, T_A, which may be formulaically expressed as:

$$P\,(\text{max.}) = \frac{T_J\,(\text{max.}) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{280}$$

It then follows that, assuming an ambient temperature of 70 °C, the maximum power dissipation will be limited to about 196 mW.

So long as the load current is below the 1.2 A limit, the maximum continuous switch current becomes a function two things: the package power dissipation and the $R_{DS(ON)}$ at the ambient temperature.

As an example let us calculate the worst case maximum load current at T_A = 70 °C. The worst case $R_{DS(ON)}$ at 25 °C is 65 mΩ. The $R_{DS(ON)}$ at 70 °C can be extrapolated from this data using the following formula:

$R_{DS(ON)}$ (at 70 °C) = $R_{DS(ON)}$ (at 25 °C) x (1 + T_C x ΔT)

Where T_C is 3900 ppm/°C. Continuing with the calculation we have

$R_{DS(ON)}$ (at 70 °C) = 65 mΩ x (1 + 0.0039 x (70 °C - 25 °C)) = 76.4 mΩ

The maximum current limit is then determined by

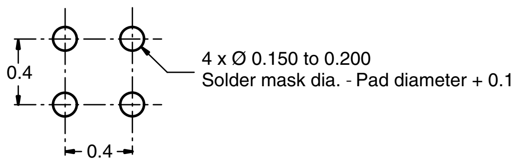
$$I_{LOAD}\,(\text{max.}) < \sqrt{\frac{P\,(\text{max.})}{R_{DS(ON)}}}$$

which in this case is 1.6 A. Under the stated input voltage condition, if the 1.6 A current limit is exceeded the internal die temperature will rise and eventually, possibly damage the device.

To avoid possible permanent damage to the device and keep a reasonable design margin, it is recommended to operate the device maximum up to 1.2 A only as listed in the Absolute Maximum Ratings table.

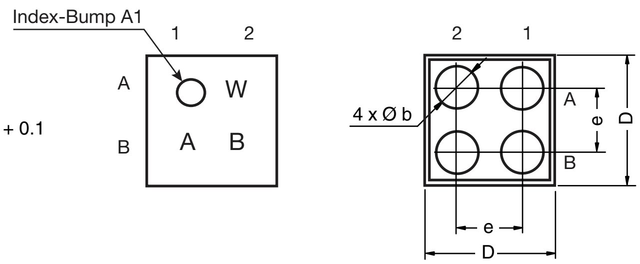
PACKAGE OUTLINE

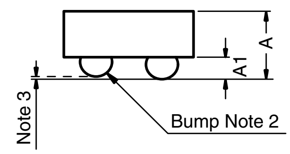
WCSP4: 4 Bumps (2 x 2, 0.4 mm Pitch, 208 µm Bump Height, 0.8 mm x 0.8 mm Die Size)



Recommended Land Pattern
All dimensions in millimeters

Mark on backside of die





Dimension	MILLIMETERS			INCHES		
	Min.	**Nom.**	**MAX.**	**Min.**	**Nom.**	**MAX.**
A	0.515	0.530	0.545	0.0202	0.0208	0.0214
A1		0.208			0.0081	
b	0.250	0.260	0.270	0.0098	0.0102	0.0106
e		0.400			0.0157	
D	0.720	0.760	0.800	0.0182	0.0193	0.0203

Notes:
1. Laser mark on the backside surface of die.
2. Bumps are SAC396.
3. 0.050 max. coplanarity.

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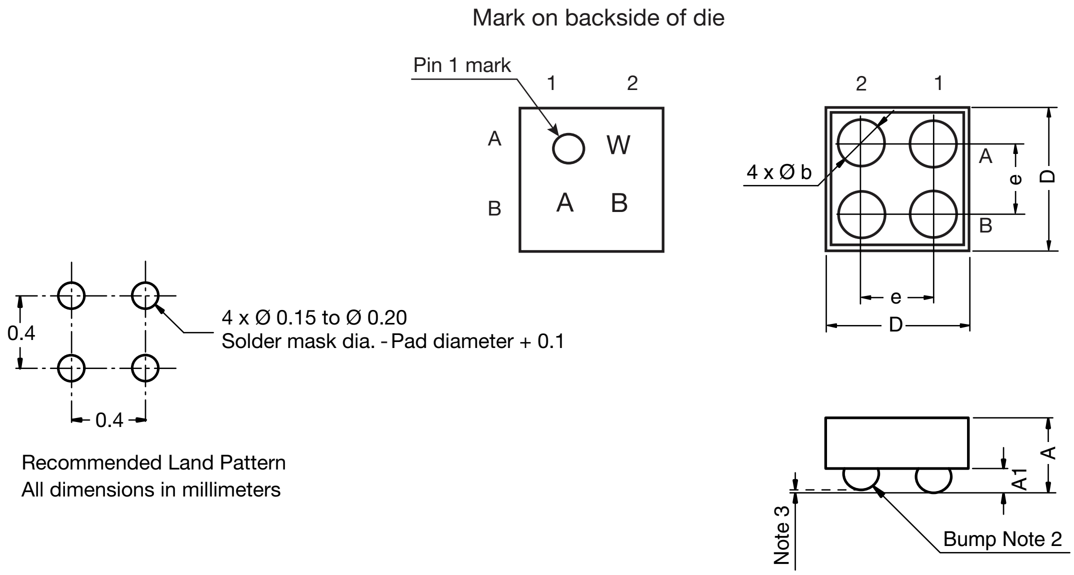
WCSP4: 4 Bumps

(2 x 2, 0.4 mm pitch, 208 µm bump height, 0.8 mm x 0.8 mm die size)



DWG-No: 6004

Notes

(1) Laser mark on the backside surface of die

(2) Bumps are SAC396

(3) 0.05 max. coplanarity

DIM.	MILLIMETERS [a]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.515	0.530	0.545	0.0202	0.0208	0.0214
A1		0.208			0.0081	
b	0.250	0.260	0.270	0.0098	0.0102	0.0106
e		0.400			0.0157	
D	0.720	0.760	0.800	0.0182	0.0193	0.0203

Note

a. Use millimeters as the primary measurement.

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