SY58020U

6GHz, 1:4 CML Fanout Buffer/Translator with Internal I/O Termination

General Description

The SY58020U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 CML fanout buffer. Optimized to provide four identical output copies with less than 15ps of skew and 27fs$_{RMS}$ of typical additive phase jitter, the SY58020U can process clock signals as fast as 6GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to differential LVPECL, LVDS, and CML signals (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the V_T pin. The outputs are optimized to drive 400mV typical swing into 50Ω loads, with extremely fast rise/fall times guaranteed to be less than 60ps.

The SY58020U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL outputs, consider the SY58021U or SY58022U 1:4 fanout buffer with 800mV and 400mV output swing, respectively. The SY58020U is part of Micrel's high-speed, Precision Edge® product line. Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

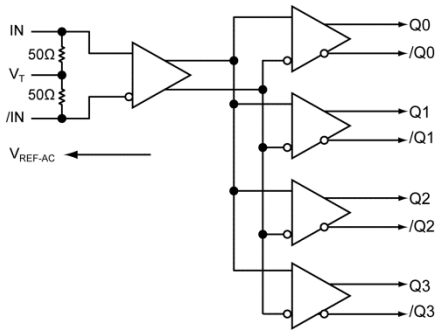
Features

- Precision 1:4, 400mV CML fanout buffer
- Guaranteed AC performance over temperature/voltage:
  - > 6GHz f_{MAX} clock
  - < 60ps t_r / t_f times
  - < 250ps t_{pd}
  - < 15ps max. skew
- Low-jitter performance:
  - 27fs$_{RMS}$ typical additive phase jitter
- Accepts an input signal as low as 100mV
- Unique patented input termination and V_T pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML
- 50Ω source terminated CML outputs
- Power supply 2.5V ±5% and 3.3V ±10%
- Industrial temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

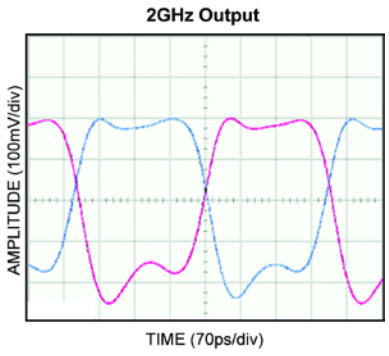
Applications

- All SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplane distribution
- Data distribution: OC-48, OC-48+FEC, XAUI
- High-end, low skew, multiprocessor synchronous clock distribution

Functional Block Diagram



Typical Performance



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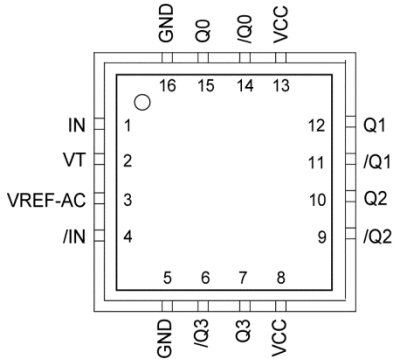
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58020UMG	QFN-16	Industrial	020U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58020UMG TR[2]	QFN-16	Industrial	020U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC electrical only.
2. Tape and Reel.

Pin Configuration



16-Pin QFN (QFN-16)

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the V_T pin. Note that this input will default to an indeterminate state if left open. See "*Input Interface Applications*" section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The V_T pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See "*Input Interface Applications*" section.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC}-1.2V. It is used when AC-coupling to differential inputs. Connect V_{REF-AC} directly to the V_T pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. See "*Input Interface Applications*" section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the pins as possible.
5, 16	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15 11, 12 9, 10 6, 7	/Q0, Q0, /Q1, Q1, /Q2, Q2, /Q3, Q3	CML Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400mV into 50Ω load. Normally terminate CML output pairs with 100Ω across Q and /Q outputs at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See "CML Output Termination" section.

Absolute Maximum Ratings[3]

Power Supply Voltage (V_{CC}) ..... -0.5V to +4.0V
Input Voltage (V_{IN}) ..... -0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC}-1.0V to V_{CC}+0.5V
Current (V_T)
  Source or sink current on V_T pin ..... ±100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Current (V_{REF})
  Source or sink current on V_{REF-AC}[6], ... ±1.5mA
Lead Temperature Soldering, (20 sec.) ..... 260°C
Storage Temperature Range (T_S) ..... -65°C to +150°C

Operating Ratings[4]

Supply Voltage (V_{CC}) ..... +2.375V to +3.60V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
  QFN (θ_{JA})
    Still-Air ..... 60°C/W
    500lfpm ..... 54°C/W
  QFN (Ψ_{JB})
    (Junction-to-Board Resistance)[5] ..... 33°C/W

DC Electrical Characteristics[7]

T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V	2.375	2.500	2.625	V
		V_{CC} = 3.3V	3.000	3.300	3.600	V
I_{CC}	Power Supply Current	No Load, VCC = max. (include internal 50Ω pull-up)		150	180	mA
V_{IH}	Input HIGH Voltage	Note 8	V_{CC}-1.600		V_{CC}	V
V_{IL}	Input LOW Voltage		0		V_{IH}-0.100	V
V_{IN}	Input Voltage Swing	See Figure 1.	0.100		1.700	V
V_{DIFF_IN}	Differential Input Voltage Swing	See Figure 2.	0.200		3.400	V
R_{IN}	IN-to-V_T Resistance		40	50	60	Ω
V_{REF-AC}	Output Reference Voltage		V_{CC}-1.300	V_{CC}-1.200	V_{CC}-1.100	V
$V_{T\ IN}$	IN-to-V_T Voltage				1.280	V

CML DC Electrical Characteristics[7]

V_{CC} = 3.3V ±10% or 2.5V ±5%; R_L = 100Ω across each output pair or equivalent; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC}-0.020	V_{CC}-0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing	See Figure 1.	325	400	500	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2.	650	800	1000	mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

Notes:

3. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
4. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
5. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
6. Due to the limited drive capability, use for input of the same package only.
7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. V_{IH} (min) not lower than 1.2V.

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AC Electrical Characteristics

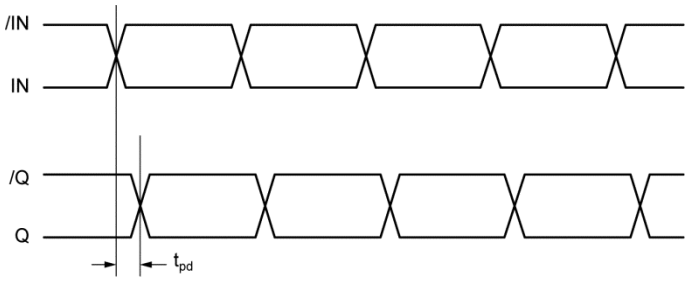
V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = -40°C to +85°C; R_L = 100Ω across each output pair or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 200mV Clock	6			GHz
		NRZ Data		10		Gbps
t_{pd}	Propagation Delay		110	180	260	ps
t_{SKEW}	Output-to-Output Skew	Note 9		4	15	ps
	Part-to-Part Skew	Note 10			50	ps
t_r, t_f	Ouptut Rise/Fall Time 20% to 80%	At full swing	20	40	60	ps
t_{JITTER}	Additive Phase Jitter	Carrier = 622MHz Integration Range: 12kHz – 20MHz		27		fs_{RMS}
		Carrier = 156.25MHz Integration Range: 12kHz – 20MHz		128		

Notes:

9. Skew is measured between outputs under identical transitions.
10. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

Timing Diagram



Single-Ended and Differential Swings

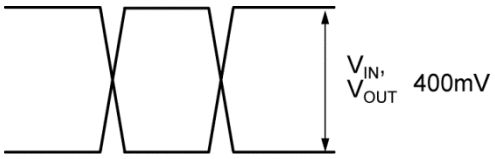


Figure 1. Single-Ended Voltage Swing

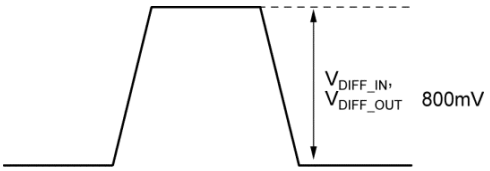


Figure 2. Differential Voltage Swing

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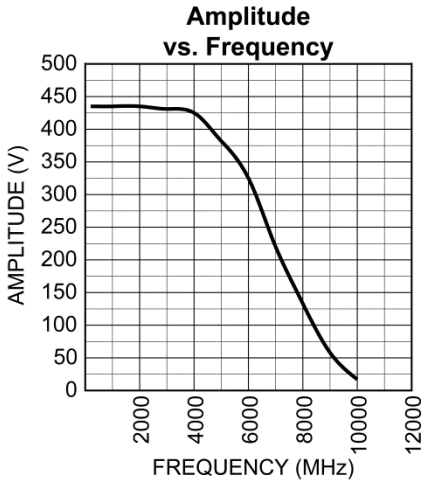
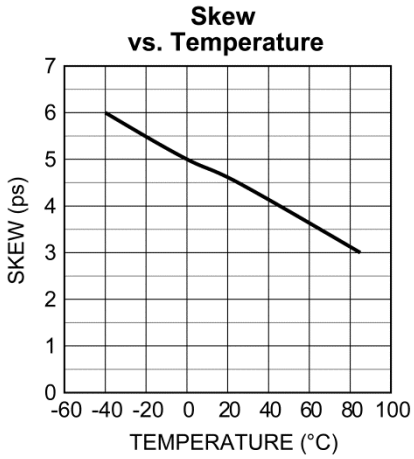
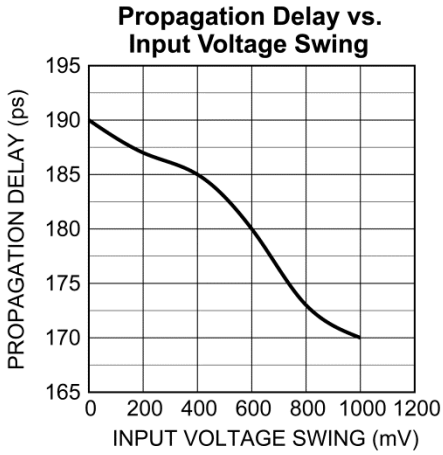
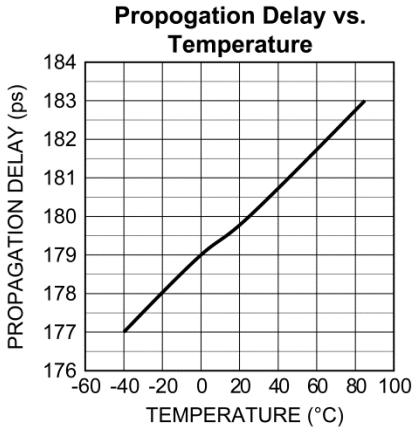
Typical Operating Characteristics

V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.





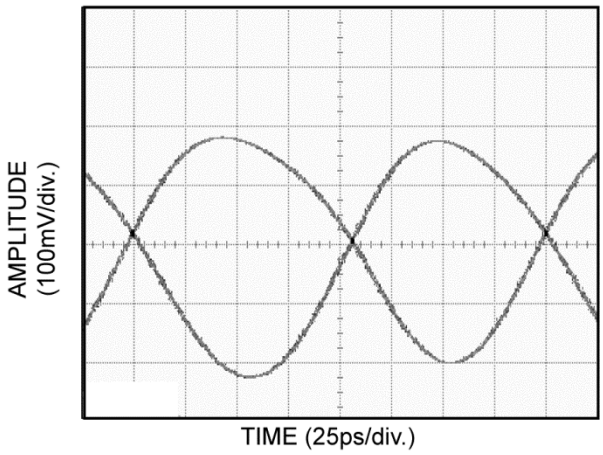




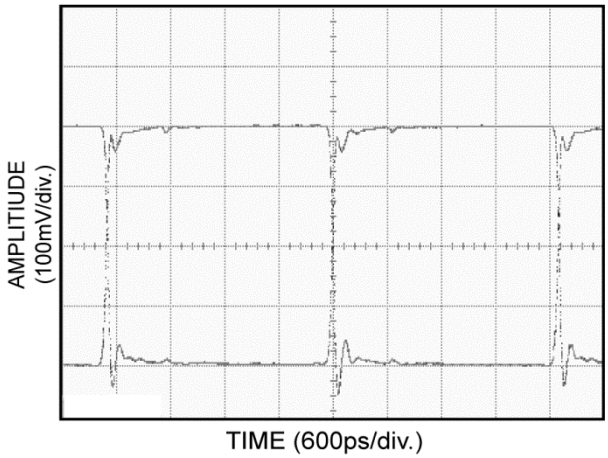
Functional Characteristics

V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

5GHz Output

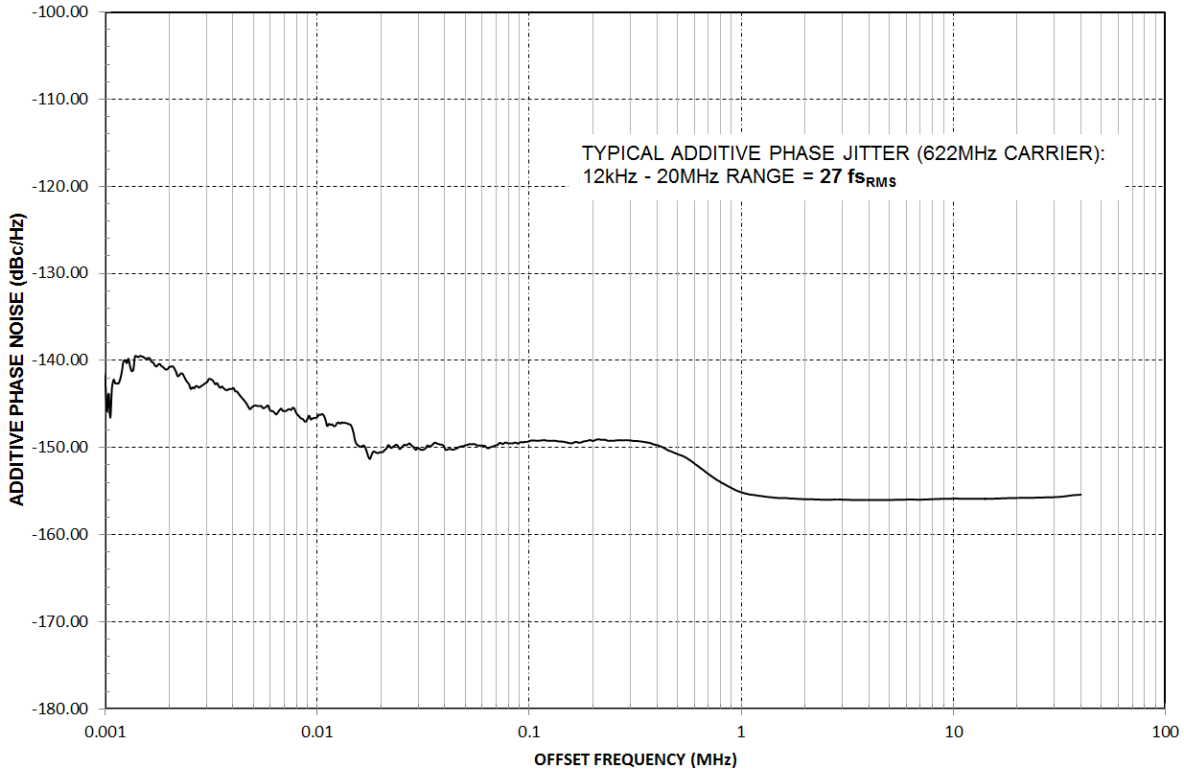


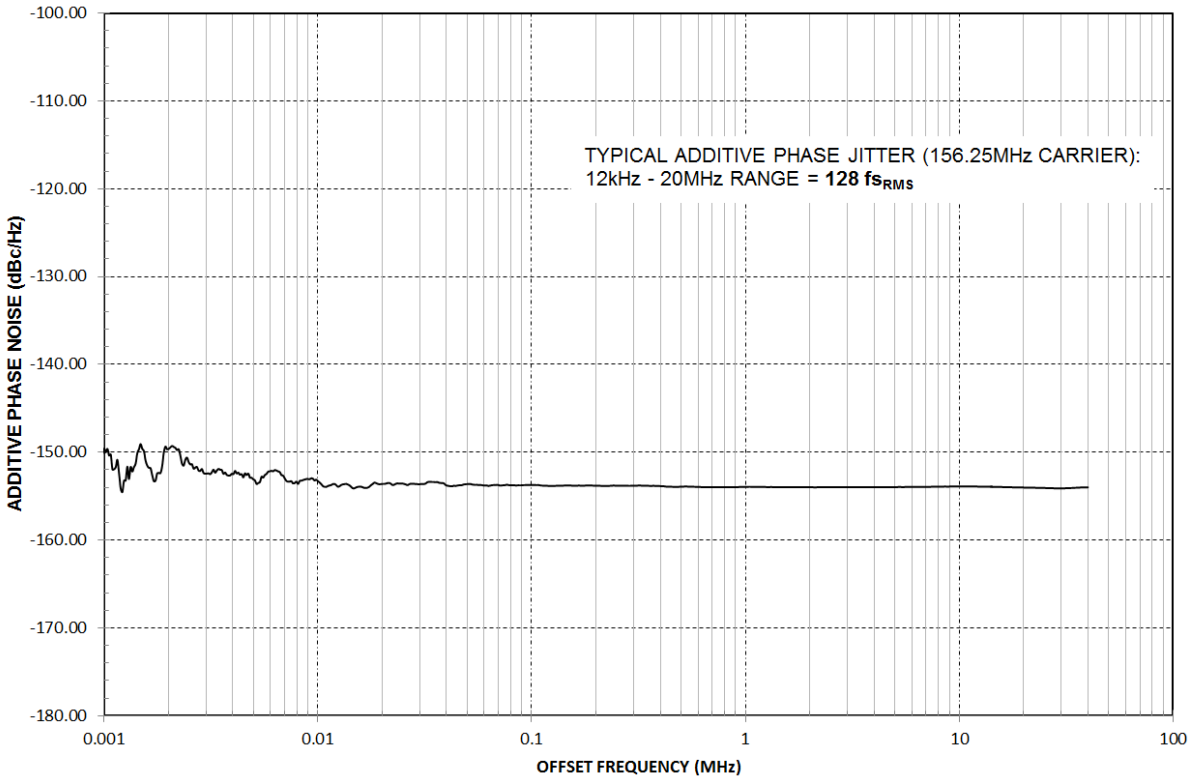
200MHz Output



Additive Phase Noise Plots

V_{CC} = 3.3V, GND = 0, T_A = 25°C.





Input Stage

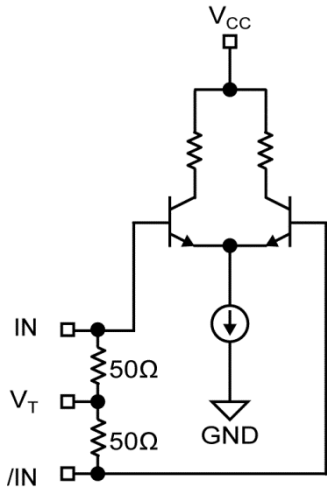


Figure 3. Simplified Differential Input Buffer

Input Interface Applications

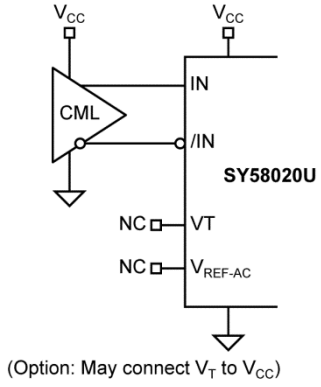


Figure 4. DC-Coupled CML Input Interface

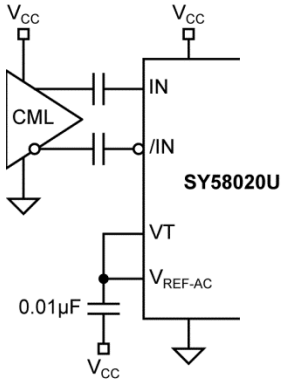


Figure 5. AC-Coupled CML Input Interface

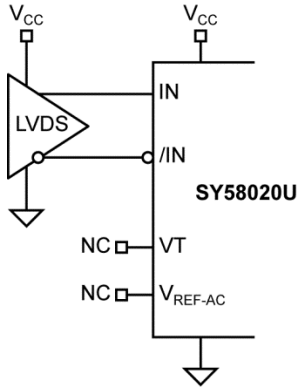


Figure 6. LVDS Input Interface

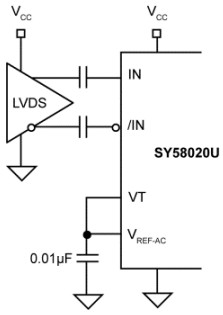


Figure 7. AC-Coupled LVDS Input Interface.

Note: Be certain that the LVDS driver can be AC-coupled.

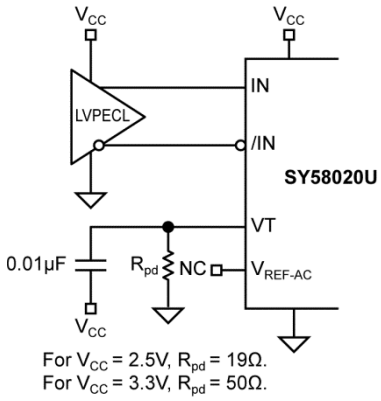


Figure 8. LVPECL Input Interface

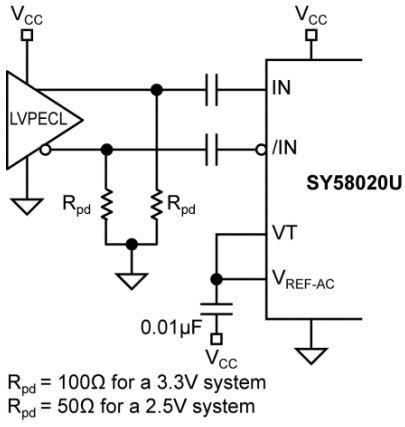


Figure 9. AC-Coupled LVPECL Input Interface

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CML Output Termination

Figures 10 and 11 illustrate a CML output using both the AC-coupled and DC-coupled configuration. All outputs of the SY58020U are 50Ω with a 16mA current source.

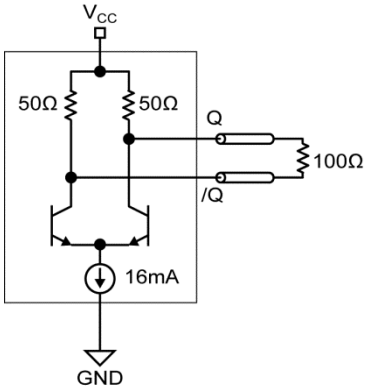


Figure 10. CML DC-Coupled

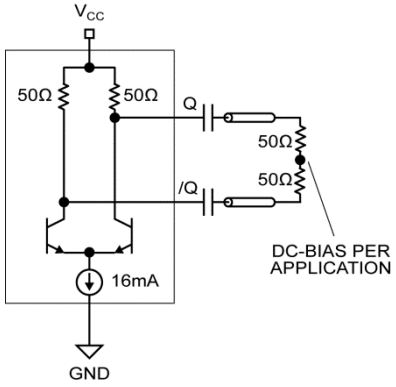
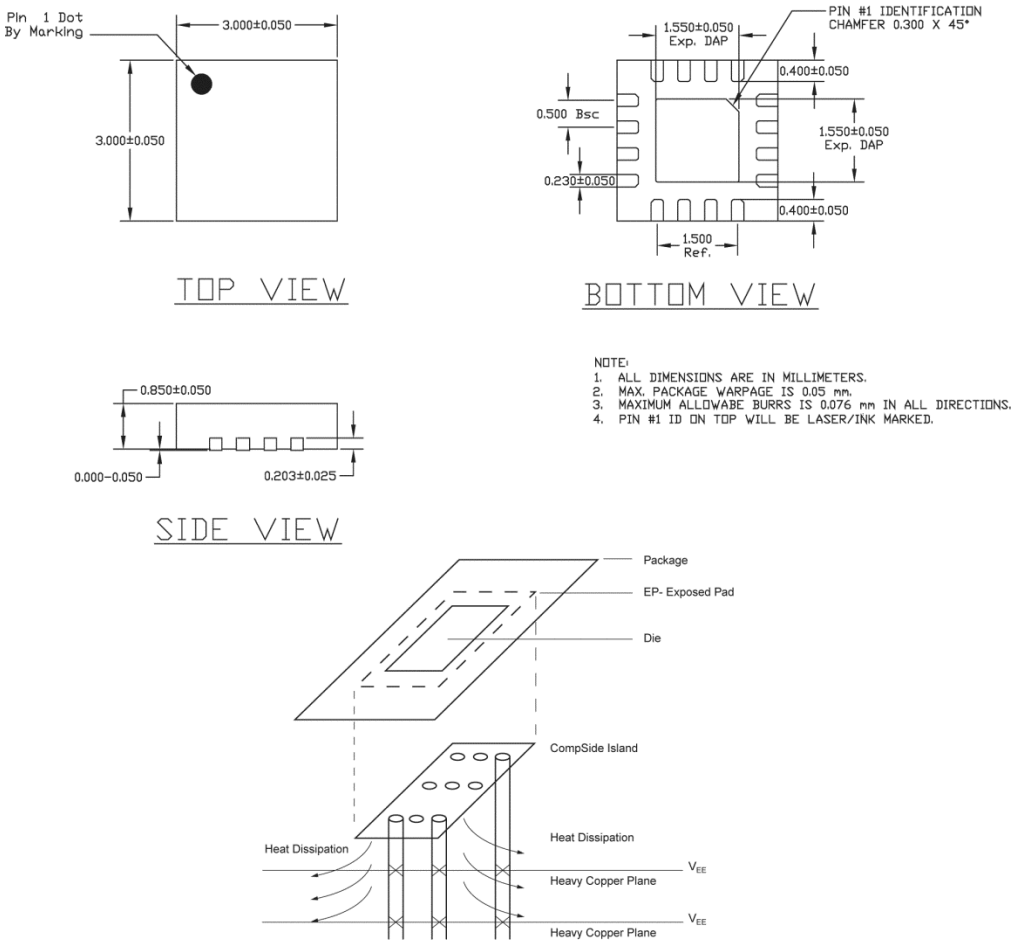


Figure 11. CML AC-Coupled Termination

Package Information[16]



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

16-Pin Package Type (QFN-16)

Note:

11. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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Revision History

Date	Change Description/Edits by:	Rev.
8/4/10	Added new paragraph to disclaimer in boiler plate. Per Colin Sturt. M.Galvan	14
1/16/13	Complete rework	15
5/8/14	Updated Contact Email	16

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