1.8-GHz, LOW DISTORTION, CURRENT-FEEDBACK AMPLIFIER

FEATURES

- **Unity-Gain Bandwidth: 1.8 GHz**
- **High Slew Rate: 6700 V/μs (G = 2 V/V, R_L = 100 Ω, 10-V Step)**
- **IMD_3: –78 dBc at 20 MHz: (G = 10 V/V, R_L = 100 Ω, 2-V_{PP} Envelope)**
- **Noise Figure: 11 dB (G = 10 V/V, R_G = 28 Ω, R_F = 255 Ω)**
- **Input-Referred Noise (f >10 MHz)**
  - **Voltage Noise: 1.65 nV/√Hz**
  - **Noninverting Current Noise: 13.4 pA/√Hz**
  - **Inverting Current Noise: 20 pA/√Hz**
- **Output Drive: 100 mA**
- **Power-Supply Voltage Range: ±3.3 V to ±7.5 V**

APPLICATIONS

- **Test and Measurement**
- **ATE**
- **High-Resolution, High-Sampling Rate ADC Drivers**
- **High-Resolution, High-Sampling Rate DAC Output Buffers**

DESCRIPTION

The THS3201 is a wideband, high-speed current-feedback amplifier, designed to operate over a wide supply range of ±3.3 V to ±7.5 V for today's high performance applications.

The wide supply range, combined with low distortion and high slew rate, makes the THS3201 ideally suited for arbitrary waveform driver applications. The distortion performance also enables driving high-resolution and high-sampling rate analog-to-digital converters (ADCs).

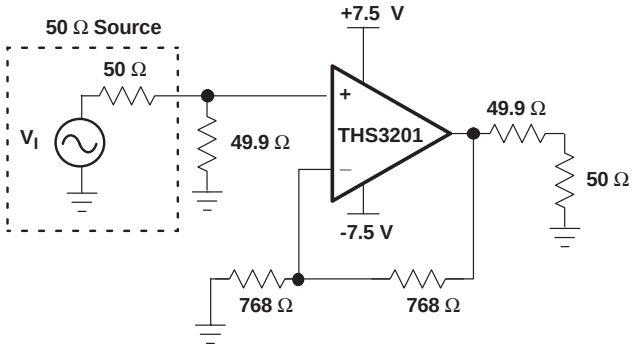
Its high voltage operation capabilities make the THS3201 especially suitable for many test, measurement, and ATE applications where lower voltage devices do not offer enough voltage swing capability. Output rise and fall times are nearly independent of step size (to first-order approximation), making the THS3201 ideal for buffering small to large step pulses with excellent linearity in high dynamic systems.

The THS3201 is offered in a 5-pin SOT-23, 8-pin SOIC, and an 8-pin MSOP with PowerPAD™ packages.

RELATED DEVICES AND DESCRIPTIONS

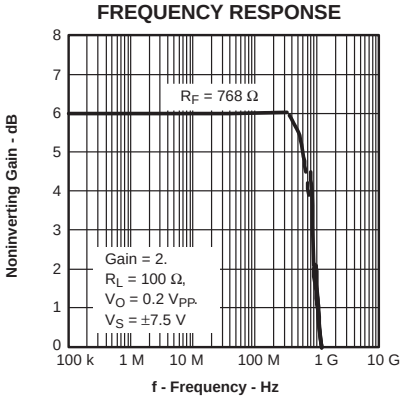
DEVICE	DESCRIPTION
THS3202	±7.5-V, 2-GHz Dual Low Distortion CFB Amplifier
THS3001	±15-V, 420-MHz Low Distortion CFB Amplifier
THS3061/2	±15-V, 300-MHz Low Distortion CFB Amplifier
THS3122	±15-V, Dual CFB Amplifier With 350 mA Drive
OPA695	±5-V, 1.7-GHz Low Distortion CFB Amplifier

Low-Noise, Low-Distortion, Wideband Application Circuit



NOTE: Power supply decoupling capacitors not shown

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted.(1)

		UNIT
V_S	Supply voltage	16.5 V
V_I	Input voltage	$\pm V_S$
I_O	Output current	175 mA
V_{ID}	Differential input voltage	±3 V
	Continuous power dissipation	See Dissipation Rating Table
T_J	Maximum junction temperature(2)	+150°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)	+125°C
T_A	Operating free-air temperature range	–40°C to +85°C
T_{STG}	Storage temperature range	–65°C to +150°C
ESD ratings	HBM	3000 V
	CDM	1500 V
	MM	100 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JC} (°C/W)	θ_{JA}(2) (°C/W)	POWER RATING(3) (T_J = +125°C)	
			$T_A \le$ +25°C	T_A= +85°C
DBV (5)	55	255.4	391 mW	156 mW
D (8)	38.3	97.5	1.02 W	410 mW
DGN (8)(1)	4.7	58.4	1.71 W	685 mW
DGK (8 pin)	54.2	260	385 mW	154 mW

(1) The THS3201 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.
(2) This data was taken using the JEDEC standard High-K test PCB.
(3) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Supply voltage	Dual supply	±3.3	±7.5	V
		Single supply	6.6	15	
T_A	Operating free-air temperature range		–40	+85	°C

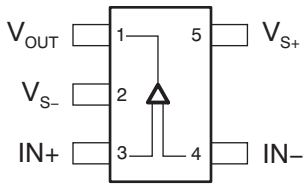
PACKAGE/ORDERING INFORMATION(1)

PART NUMBER	PACKAGE TYPE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
THS3201D	SOIC-8	—	Rails, 75
THS3201DR			Tape and Reel, 2500
THS3201DBVT	SOT-23	BEO	Tape and Reel, 250
THS3201DBVR			Tape and Reel, 3000
THS3201DGN	MSOP-8-PP	BEN	Rails, 80
THS3201DGNR			Tape and Reel, 2500
THS3201DGK	MSOP-8	BGP	Rails, 80
THS3201DGKR			Tape and Reel, 2500

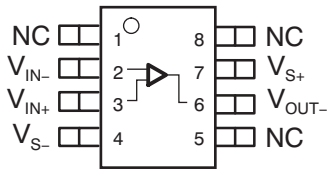
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN ASSIGNMENTS

DBV PACKAGE
SOT23-5
(TOP VIEW)



D, DGN, DGK PACKAGES
SOIC-8, MSOP-8
(TOP VIEW)



NC = No internal connection.

See Note A.

A. If a PowerPAD is used, it is electrically isolated from the active circuitry.

ELECTRICAL CHARACTERISTICS: V_S = ±7.5 V

At R_F = 768 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS		THS3201					
			TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
AC PERFORMANCE								
Small-signal bandwidth, –3 dB (V_O = 200 mV_{PP})	G = +1, R_F = 1.2 kΩ		1.8				GHz	Typ
	G = +2, R_F = 768 Ω		850				MHz	Typ
	G = +5, R_F = 619 Ω		565				MHz	Typ
	G = +10, R_F = 487 Ω		520				MHz	Typ
Bandwidth for 0.1 dB flatness	G = +2, V_O = 200 mV_{pp}		380				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 2 V_{pp}		880				MHz	Typ
Slew rate	G = +2, V_O = 5-V step, Rise/Fall		5400/4000				V/µs	Typ
	G = +2, V_O = 10-V step, Rise/Fall		9800/6700				V/µs	Typ
Rise and fall time	G = +2, V_O = 4-V step, Rise/Fall		0.7/0.9				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V step		20				ns	Typ
Settling time to 0.01%			60				ns	Typ
Harmonic distortion								
2nd-order harmonic	G = +5, f = 10 MHz, V_O = 2 V_{pp}	R_L = 100 Ω	–64				dBc	Typ
3rd-order harmonic		R_L = 100 Ω	–73				dBc	Typ
Third-order intermodulation distortion (IMD_3)	G = +10, f_c = 20 MHz, Δf = 1 MHz, $V_{O(envelope)}$ = 2 V_{pp}		–78				dBc	Typ
Noise figure	G = +10, f_c = 100 MHz, R_F = 255 Ω, R_G = 28		11				dB	Typ
Input voltage noise	f > 10 MHz		1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz		13.4				pA/√Hz	Typ
Input current noise (inverting)			20				pA/√Hz	Typ
Differential gain	G = +2, R_L = 150 Ω, R_F = 768 Ω	NTSC	0.008%					Typ
		PAL	0.004%					Typ
Differential phase		NTSC	0.007°					Typ
		PAL	0.011°					Typ
DC PERFORMANCE								
Open-loop transimpedance gain	V_O = ±1 V, R_L = 1 kΩ		300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 0 V		±0.7	±3	±3.8	±4	mV	Max
Average offset voltage drift					±10	±13	µV/°C	Typ
Input bias current (inverting)			±13	±60	±80	±85	µA	Max
Average bias current drift (–)					±300	±400	nA/°C	Typ
Input bias current (noninverting)			±14	±35	±45	±50	µA	Max
Average bias current drift (+)					±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS: V_S = ±7.5 V (continued)

At R_F = 768 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3201					
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
INPUT							
Common-mode input range		±5.1	±5	±5	±5	V	Min
Common-mode rejection ratio	V_{CM} = ±3.75 V	71	60	58	58	dB	Min
Inverting input impedance, Z_{in}	Open loop	16				Ω	Typ
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±6	±5.9	±5.8	±5.8	V	Min
	R_L = 100 Ω	±5.8	±5.7	±5.5	±5.5	V	Min
Current output, sourcing	R_L = 20 Ω	115	105	100	100	mA	Min
Current output, sinking		100	85	80	80	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Minimum operating voltage	Absolute minimum		±3.3	±3.3	±3.3	V	Min
Maximum operating voltage	Absolute maximum		±8.25	±8.25	±8.25	V	Max
Maximum quiescent current		14	18	21	21	mA	Max
Power-supply rejection (+PSRR)	V_{S+} = 7 V to 8 V	69	63	60	60	dB	Min
Power-supply rejection (–PSRR)	$V_{S–}$ = –7 V to –8 V	65	58	55	55	dB	Min

ELECTRICAL CHARACTERISTICS: V_S = ±5 V

At R_F = 715 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS		THS3201					
			TYP	OVER TEMPERATURE				
			+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
AC PERFORMANCE								
Small-signal bandwidth, –3dB (V_O = 200 mV_{PP})	G = +1, R_F= 1.2 kΩ		1.3				GHz	Typ
	G = +2, R_F = 715 Ω		725				MHz	
	G = +5, R_F = 576 Ω		540					
	G = +10, R_F = 464 Ω		480					
Bandwidth for 0.1 dB flatness	G = +2, V_O = 200 mV_{PP}		170				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 2 V_{PP}		900				MHz	Typ
Slew rate	G = +2, V_O = 5-V step, Rise/Fall		5200/4000				V/µs	Typ
Rise and fall time	G = +2, V_O = 4-V step, Rise/Fall		0.7/0.9				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V step		20				ns	Typ
Settling time to 0.01%			60				ns	Typ
Harmonic distortion								
2nd-order harmonic	G = +5, f = 10 MHz, V_O = 2 V_{pp}	R_L = 100 Ω	–69				dBc	Typ
3rd-order harmonic		R_L = 100 Ω	–75				dBc	Typ
Third-order intermodulation distortion (IMD_3)	G = +10, f_c = 20 MHz, Δf = 1 MHz, $V_{O(envelope)}$ = 2 V_{PP}		–81				dBc	Typ
Noise figure	G = +10, f_c = 100 MHz, R_F = 255 Ω, R_G = 28		11				dB	Typ
Input voltage noise	f > 10 MHz		1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz		13.4				pA/√Hz	Typ
Input current noise (inverting)			20				pA/√Hz	Typ
Differential gain	G = +2, R_L = 150 Ω, R_F = 768 Ω	NTSC	0.006%					Typ
		PAL	0.004%					Typ
Differential phase		NTSC	0.03°					Typ
		PAL	0.04°					Typ
DC PERFORMANCE								
Open-loop transimpedance gain	V_O = +1 V, R_L = 1 kΩ		300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 0 V		±0.7	±3	±3.8	±4	mV	Max
Average offset voltage drift					±10	±13	±V/°C	Typ
Input bias current (inverting)			±13	±60	±80	±85	µA	Max
Average bias current drift (–)					±300	±400	nA/°C	Typ
Input bias current (noninverting)			±14	±35	±45	±50	µA	Max
Average bias current drift (+)					±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS: V_S = ±5 V (continued)

At R_F = 715 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3201					
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C	UNITS	MIN/ TYP/ MAX
INPUT							
Common-mode input range		±2.6	±2.5	±2.5	±2.5	V	Min
Common-mode rejection ratio	V_{CM} = ±2.5 V	71	60	58	58	dB	Min
Inverting input impedance, Z_{IN}	Open loop	17.5				Ω	Typ
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±3.65	±3.5	±3.45	±3.4	V	Min
	R_L = 100 Ω	±3.45	±3.33	±3.25	±3.2		
Current output, sourcing	R_L = 20 Ω	115	105	100	100	mA	Min
Current output, sinking		100	85	80	80	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Minimum operating voltage	Absolute minimum		±3.3	±3.3	±3.3	V	Min
Maximum operating voltage	Absolute maximum		±8.25	±8.25	±8.25	V	Max
Maximum quiescent current		14	16.8	19	20	mA	Max
Power-supply rejection (+PSRR)	V_{S+} = 4.5 V to 5.5 V	69	63	60	60	dB	Min
Power-supply rejection (–PSRR)	$V_{S–}$ = –4.5 V to –5.5 V	65	58	55	55	dB	Min

TYPICAL CHARACTERISTICS

Table of Graphs (V_S = ±7.5 V)

		FIGURE
Noninverting small-signal frequency response		1, 2
Inverting small-signal frequency response		3
Noninverting large-signal frequency response		4
Inverting large-signal frequency response		5
0.1 dB gain flatness frequency response		6
Capacitive load frequency response		7
Recommended switching resistance	vs Capacitive Load	8
2nd harmonic distortion	vs Frequency	9
3rd harmonic distortion	vs Frequency	10
2nd harmonic distortion, G = 2	vs Output voltage	11
3rd harmonic distortion, G = 2	vs Output voltage	12
2nd harmonic distortion, G = 5	vs Output voltage	13
3rd harmonic distortion, G = 5	vs Output voltage	14
2nd harmonic distortion, G = 10	vs Output voltage	15
3rd harmonic distortion, G = 10	vs Output voltage	16
Third-order intermodulation distortion (IMD_3)	vs Frequency	17
S-Parameter	vs Frequency	18, 19
Input voltage and current noise	vs Frequency	20
Noise figure	vs Frequency	21
Transimpedance	vs Frequency	22
Input offset voltage	vs Case Temperature	23
Input bias and offset current	vs Case Temperature	24
Slew rate	vs Output voltage step	25
Settling time		26, 27
Quiescent current	vs Supply voltage	28
Output voltage	vs Load resistance	29
Rejection ratio	vs Frequency	30
Noninverting small-signal transient response		31
Inverting large-signal transient response		32
Overdrive recovery time		33
Differential gain	vs Number of loads	34
Differential phase	vs Number of loads	35
Closed-loop output impedance	vs Frequency	36

Table of Graphs (V_S = ±5 V)

		FIGURE
Noninverting small-signal frequency response		37
Inverting small-signal frequency response		38
0.1 dB gain flatness frequency response		39
2nd harmonic distortion	vs Frequency	40
3rd harmonic distortion	vs Frequency	41
2nd harmonic distortion, G = 2	vs Output voltage	42
3rd harmonic distortion, G = 2	vs Output voltage	43
2nd harmonic distortion, G = 5	vs Output voltage	44
3rd harmonic distortion, G = 5	vs Output voltage	45
2nd harmonic distortion, G = 10	vs Output voltage	46
3rd harmonic distortion, G = 10	vs Output voltage	47
Third-order intermodulation distortion (IMD_3)	vs Frequency	48
S-Parameter	vs Frequency	49, 50
Slew rate	vs Output voltage step	51
Noninverting small-signal transient response		52
Inverting large-signal transient response		53
Overdrive recovery time		54

V_S = ±7.5 V Graphs

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

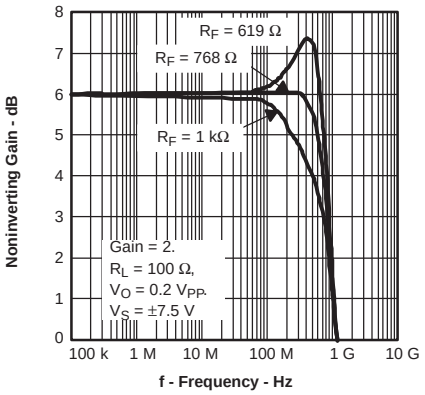


Figure 1.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

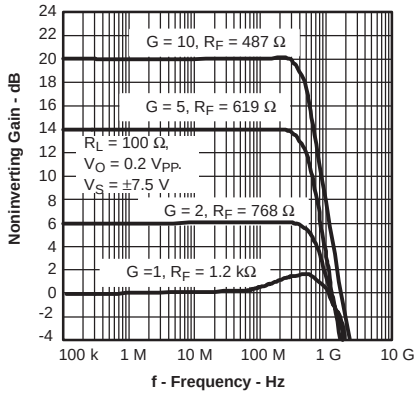


Figure 2.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

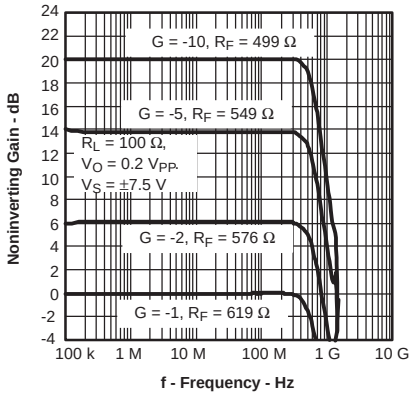


Figure 3.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

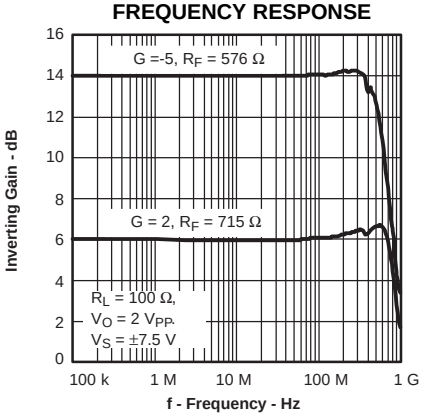


Figure 4.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

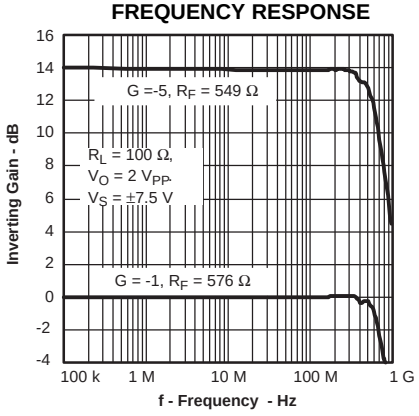


Figure 5.

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

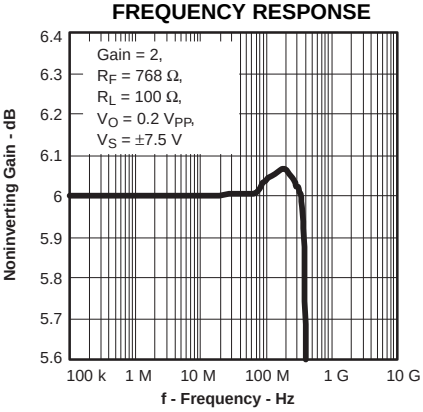


Figure 6.

CAPACITIVE LOAD FREQUENCY RESPONSE

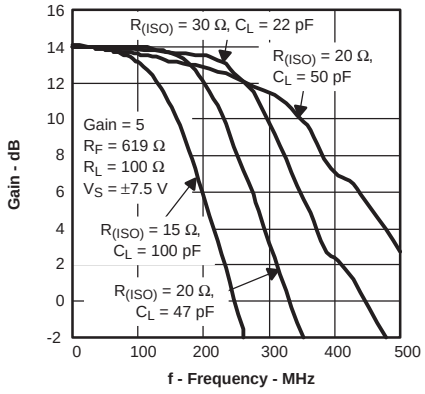


Figure 7.

RECOMMENDED R_{ISO} VS CAPACITIVE LOAD

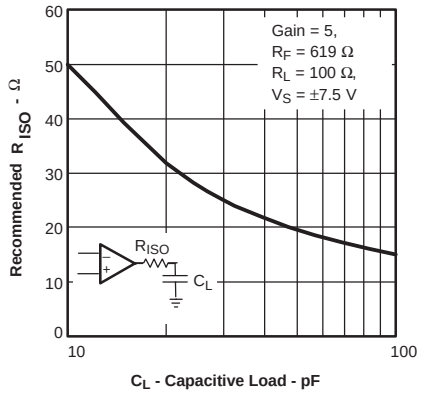


Figure 8.

2nd HARMONIC DISTORTION VS FREQUENCY

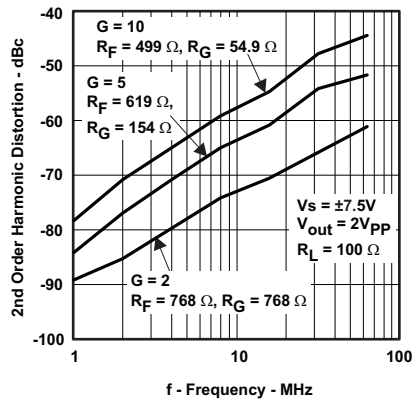


Figure 9.

V_S = ±7.5 V Graphs (continued)

3rd HARMONIC DISTORTION vs FREQUENCY

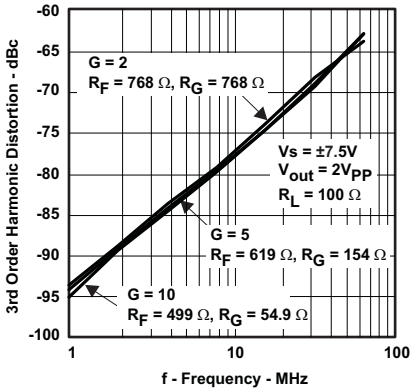


Figure 10.

2nd HARMONIC DISTORTION G = 2 vs OUTPUT VOLTAGE

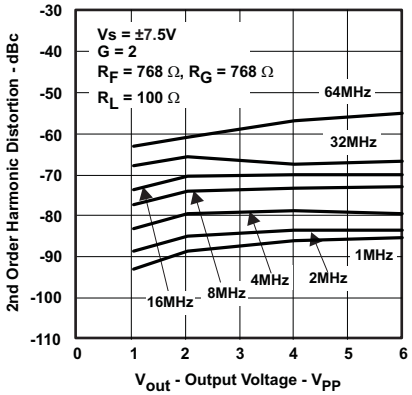


Figure 11.

3rd HARMONIC DISTORTION G = 2 vs OUTPUT VOLTAGE

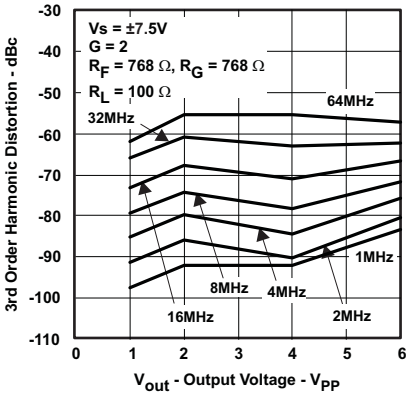


Figure 12.

2nd HARMONIC DISTORTION G = 5 vs OUTPUT VOLTAGE

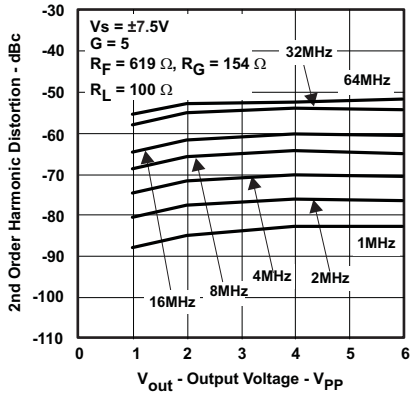


Figure 13.

3rd HARMONIC DISTORTION G = 5 vs OUTPUT VOLTAGE

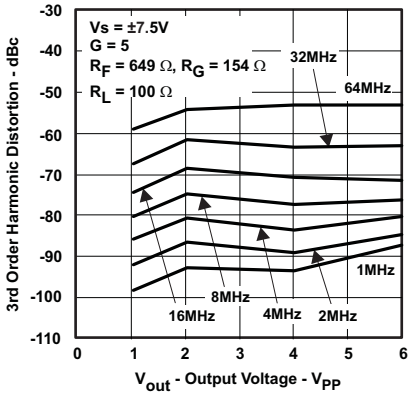


Figure 14.

2nd ORDER HARMONIC DISTORTION G = 10 vs OUTPUT VOLTAGE

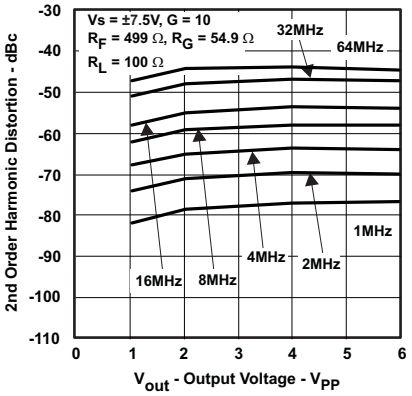


Figure 15.

3rd ORDER HARMONIC DISTORTION G = 10 vs OUTPUT VOLTAGE

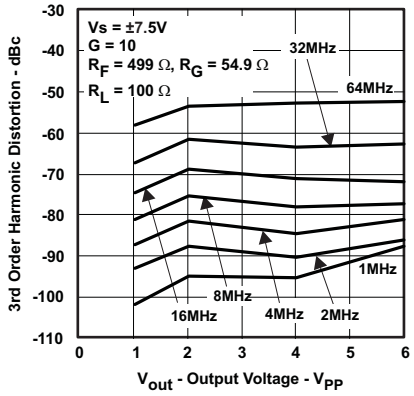


Figure 16.

3rd ORDER INTERMODULATION DISTORTION vs FREQUENCY

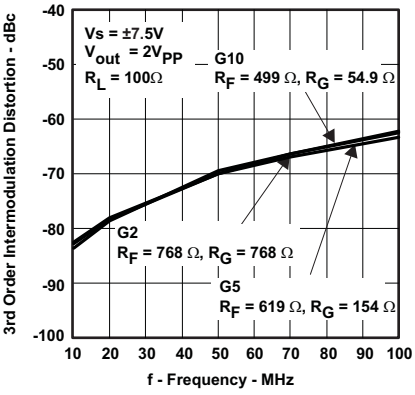


Figure 17.

S-PARAMETER vs FREQUENCY

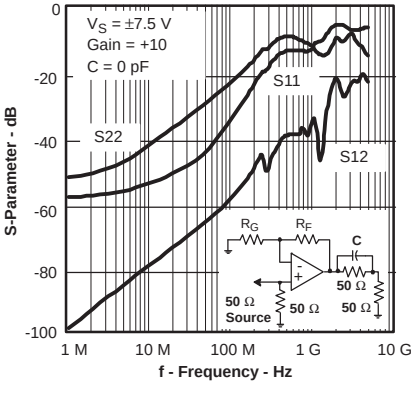


Figure 18.

V_S = ±7.5 V Graphs (continued)

S-PARAMETER vs FREQUENCY

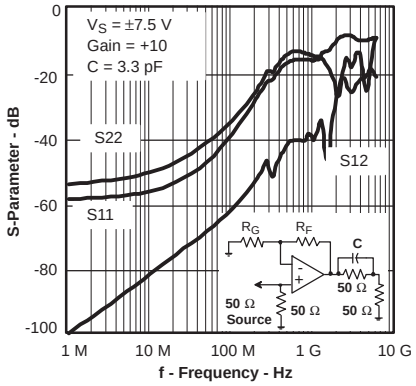


Figure 19.

INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

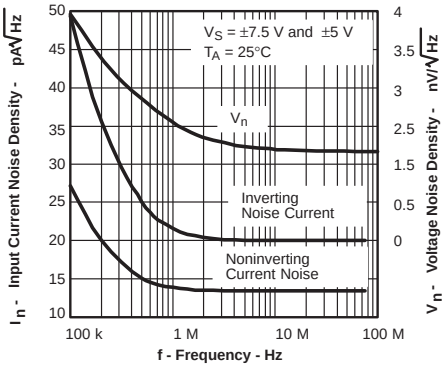


Figure 20.

NOISE FIGURE vs FREQUENCY

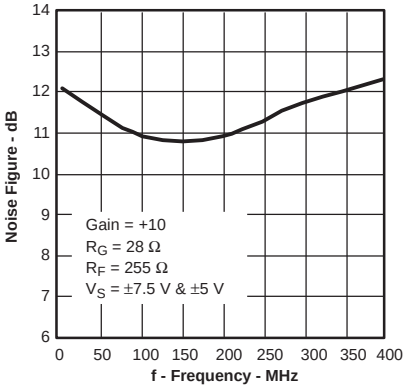


Figure 21.

TRANSIMPEDANCE vs FREQUENCY

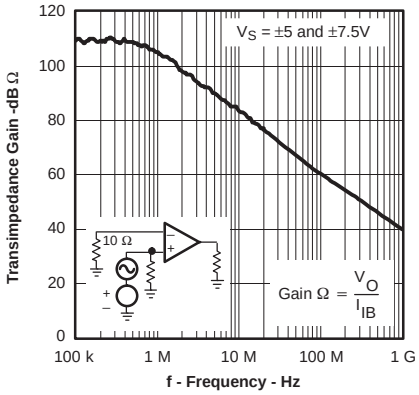


Figure 22.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

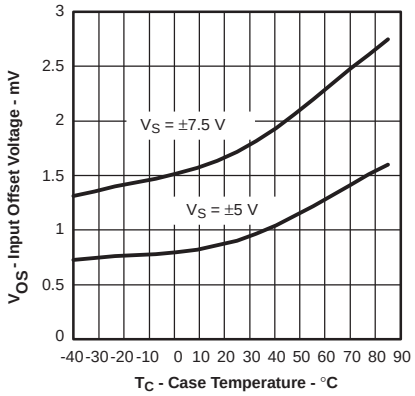


Figure 23.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

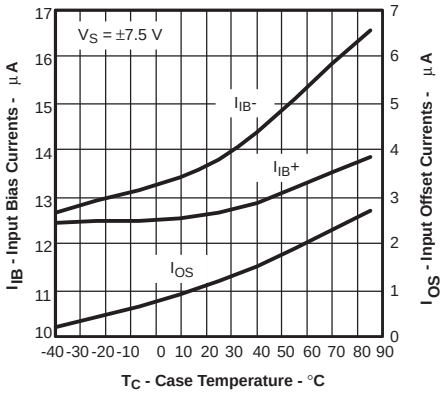


Figure 24.

SLEW RATE vs OUTPUT VOLTAGE

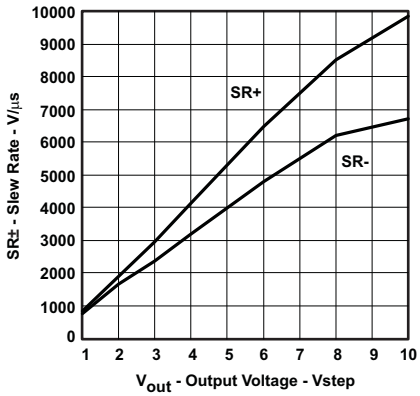


Figure 25.

SETTLING TIME

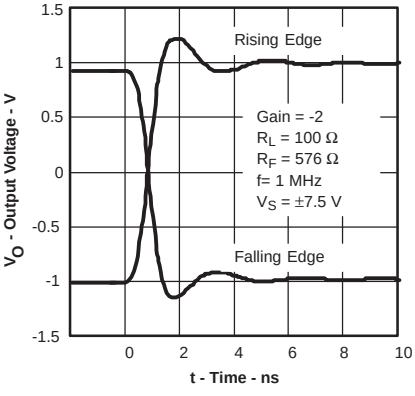


Figure 26.

SETTLING TIME

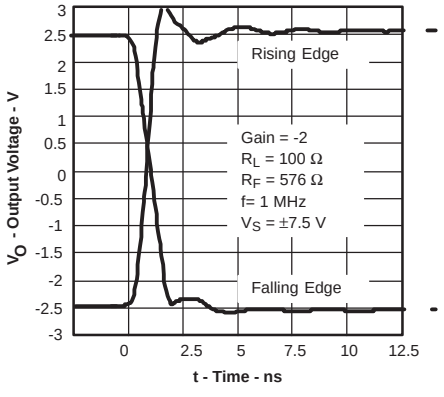


Figure 27.

V_S = ±7.5 V Graphs (continued)

QUIESCENT CURRENT vs SUPPLY VOLTAGE

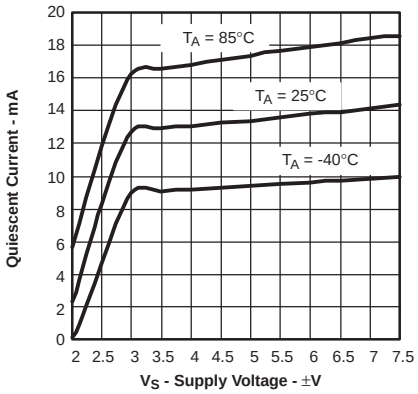


Figure 28.

OUTPUT VOLTAGE vs LOAD RESISTANCE

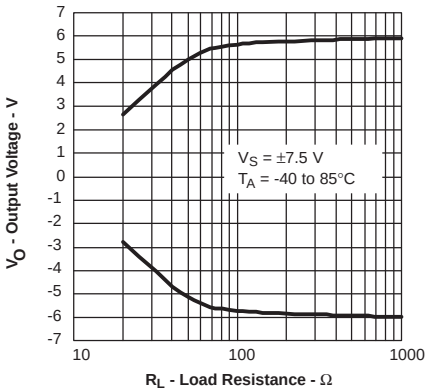


Figure 29.

REJECTION RATIO vs FREQUENCY

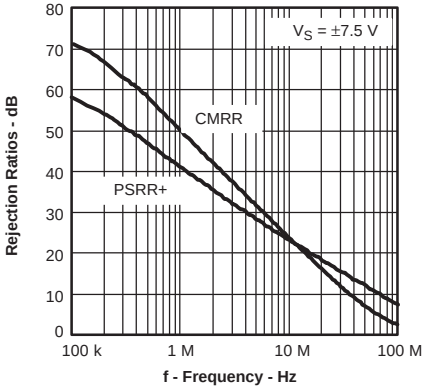


Figure 30.

NONINVERTING SMALL-SIGNAL TRANSIENT RESPONSE

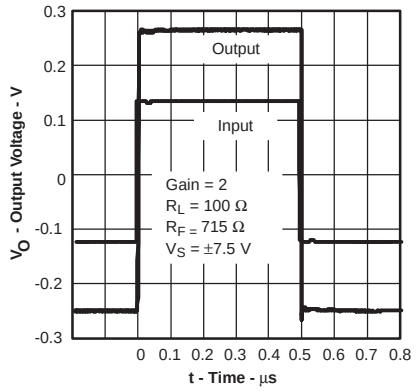


Figure 31.

INVERTING LARGE-SIGNAL TRANSIENT RESPONSE

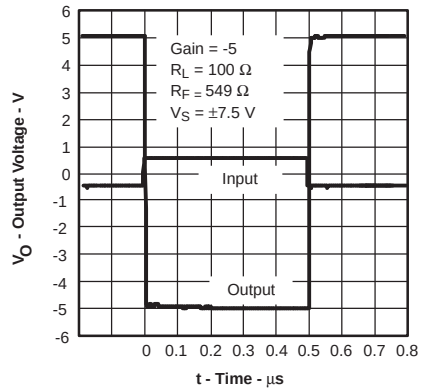


Figure 32.

OVERDRIVE RECOVERY TIME

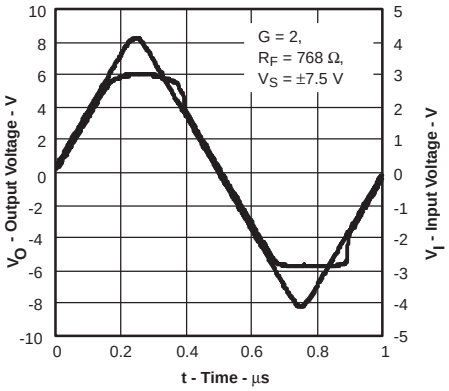


Figure 33.

DIFFERENTIAL GAIN vs NUMBER OF LOADS

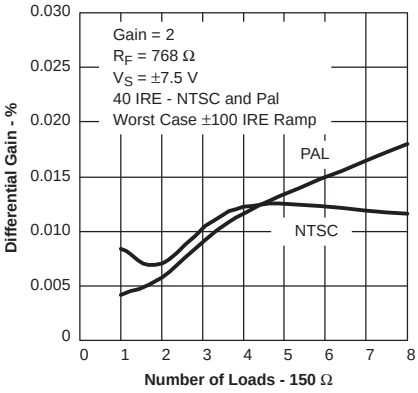


Figure 34.

DIFFERENTIAL PHASE vs NUMBER OF LOADS

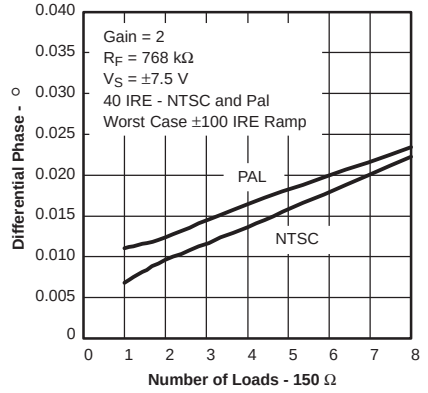


Figure 35.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

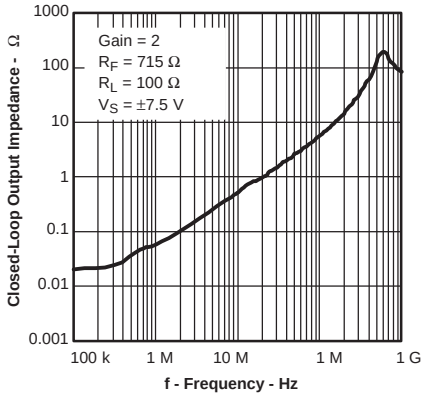


Figure 36.

V_S = ±5 V Graphs

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

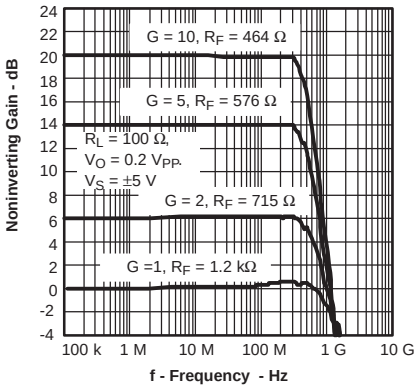


Figure 37.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

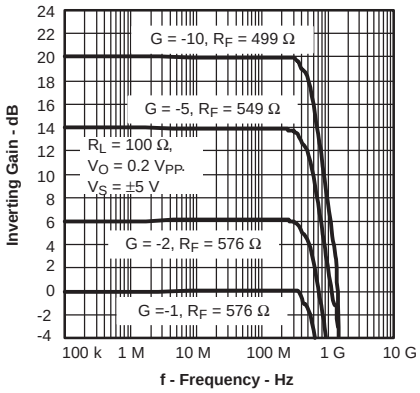


Figure 38.

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

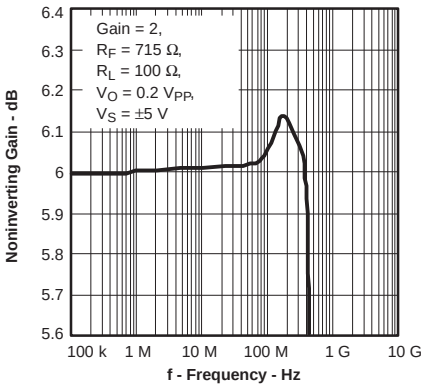


Figure 39.

2nd HARMONIC DISTORTION VS FREQUENCY

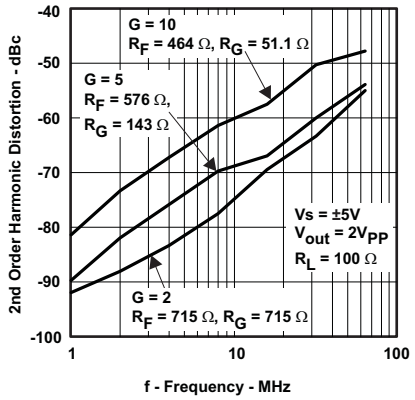


Figure 40.

3rd ORDER HARMONIC DISTORTION VS FREQUENCY

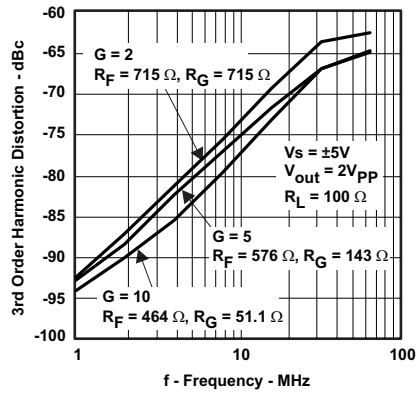


Figure 41.

2nd ORDER HARMONIC DISTORTION G = 2 VS OUTPUT VOLTAGE

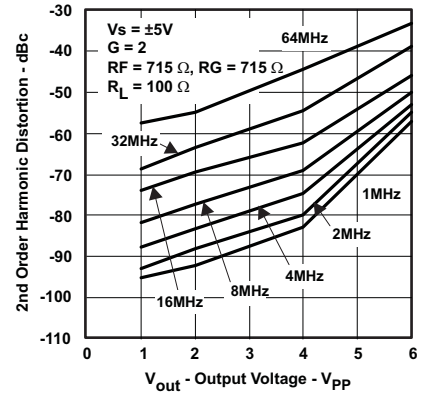


Figure 42.

3rd ORDER HARMONIC DISTORTION, G = 2 VS OUTPUT VOLTAGE

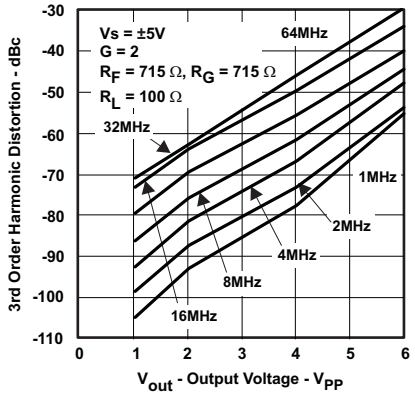


Figure 43.

2nd ORDER HARMONIC DISTORTION, G = 5 VS OUTPUT VOLTAGE

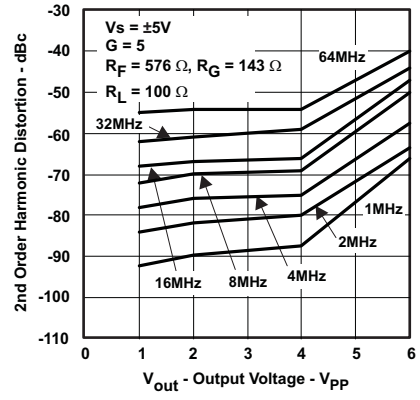


Figure 44.

3rd ORDER HARMONIC DISTORTION, G = 5 VS OUTPUT VOLTAGE

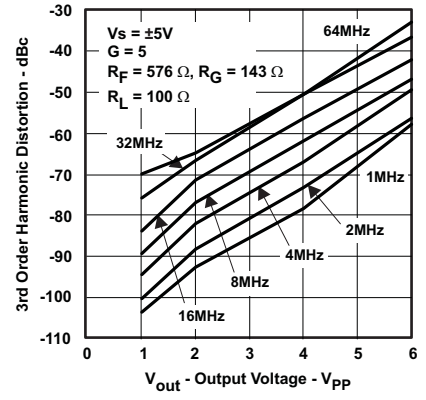


Figure 45.

V_S = ±5 V Graphs (continued)

2nd ORDER HARMONIC DISTORTION, G = 10 VS OUTPUT VOLTAGE

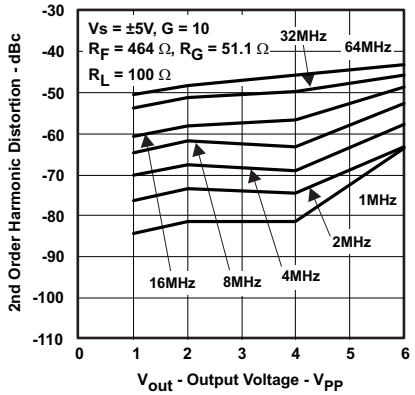


Figure 46.

3rd ORDER HARMONIC DISTORTION, G = 10 VS OUTPUT VOLTAGE

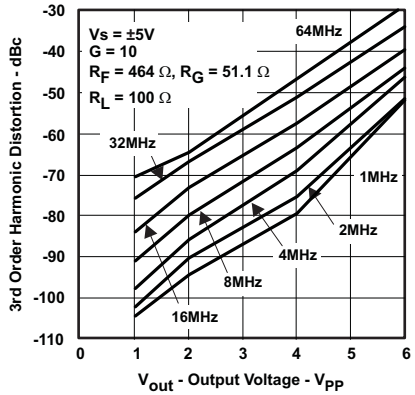


Figure 47.

3rd ORDER INTERMODULATION DISTORTION VS FREQUENCY

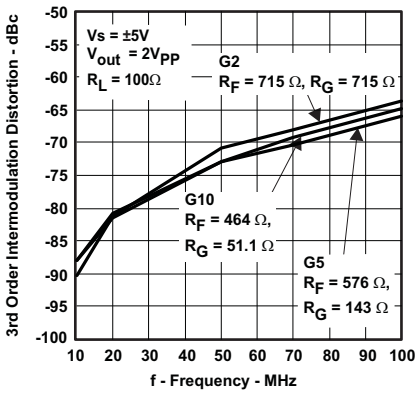


Figure 48.

S-PARAMETER VS FREQUENCY

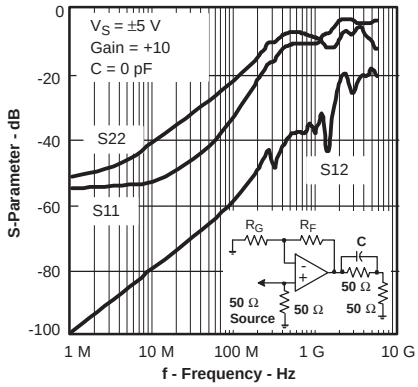


Figure 49.

S-PARAMETER VS FREQUENCY

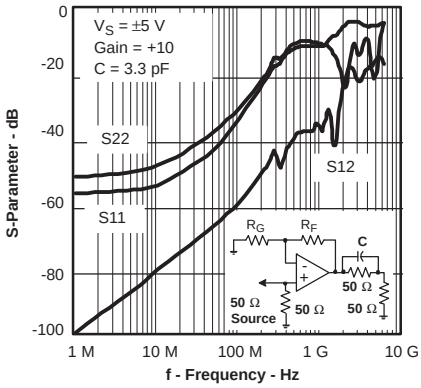


Figure 50.

SLEW RATE VS OUTPUT VOLTAGE

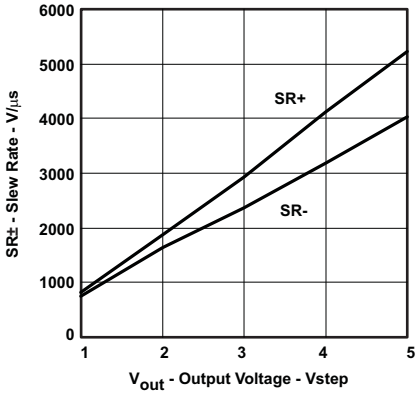


Figure 51.

NONINVERTING SMALL-SIGNAL TRANSIENT RESPONSE

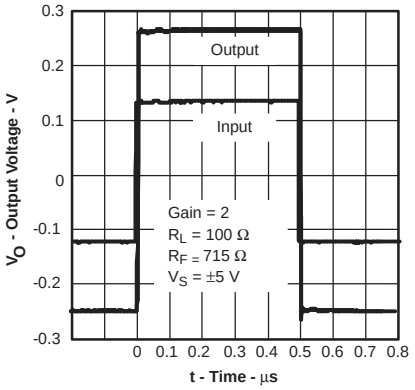


Figure 52.

INVERTING LARGE-SIGNAL TRANSIENT RESPONSE

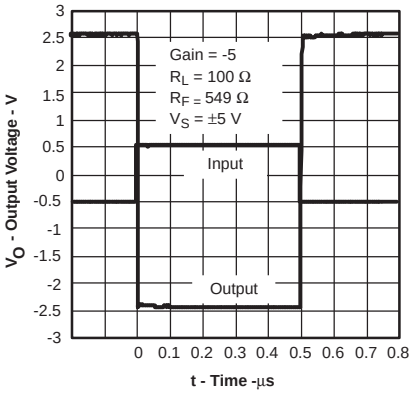


Figure 53.

OVERDRIVE RECOVERY TIME

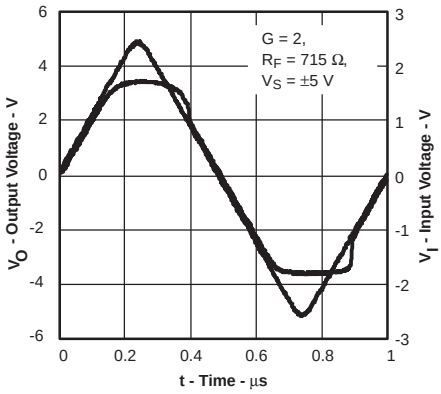


Figure 54.

APPLICATION INFORMATION

WIDEBAND, NONINVERTING OPERATION

The THS3201 is a unity-gain stable, 1.8-GHz current-feedback operational amplifier, designed to operate from a ±3.3-V to ±7.5-V power supply.

Figure 55 shows the THS3201 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance. The 49.9-Ω shunt resistor at the V_I terminal in Figure 55 matches the source impedance of the test generator.

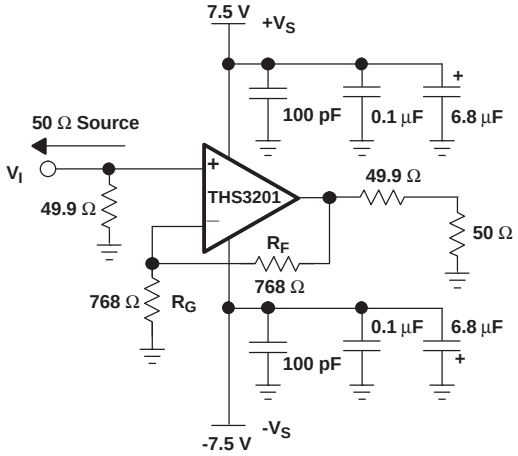


Figure 55. Wideband, Noninverting Gain Configuration

Unlike voltage-feedback amplifiers, current-feedback amplifiers are highly dependent on the feedback resistor R_F for maximum performance and stability. Table 1 shows the optimal gain setting resistors R_F and R_G at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for R_F. Conversely, increasing R_F decreases the bandwidth, but stability is improved.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3201 R_F for AC When R_{LOAD} = 100 Ω			
Gain (V/V)	Supply Voltage (V)	R_G (Ω)	R_F (Ω)
1	±7.5	—	1.2 k
	±5	—	1.2 k
2	±7.5	768	768
	±5	715	715
5	±7.5	154.9	619
	±5	143	576
10	±7.5	54.9	487
	±5	51.1	464
–1	±7.5	619	619
	±5	576	576
–2	±7.5 and ±5	287	576
–5	±7.5 and ±5	110	549
–10	±7.5 and ±5	49.9	499

WIDEBAND, INVERTING GAIN OPERATION

Figure 56 shows the THS3201 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 55 are retained in an inverting circuit configuration.

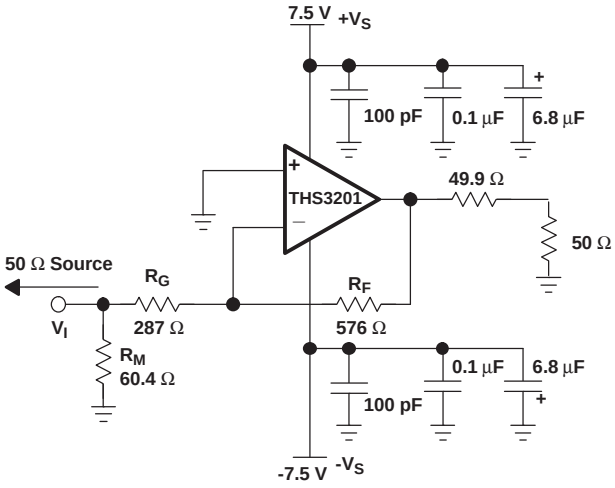


Figure 56. Wideband, Inverting Gain Configuration

SINGLE-SUPPLY OPERATION

The THS3201 has the capability to operate from a single supply voltage ranging from 6.6 V to 15 V. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 57 demonstrate methods to configure an amplifier in a manner conducive for single-supply operation.

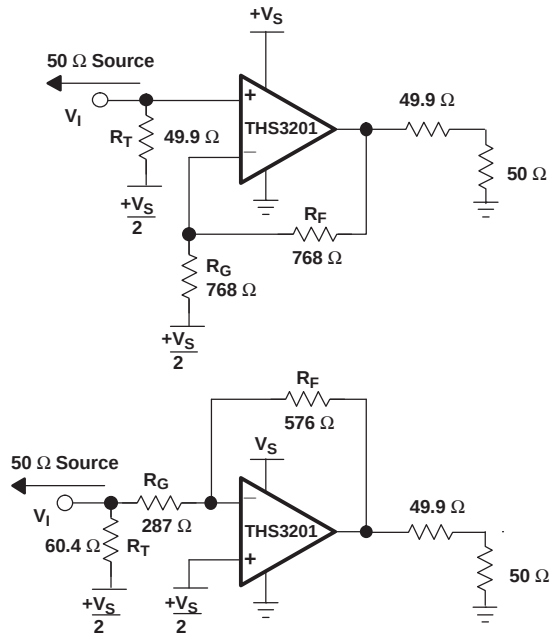


Figure 57. DC-Coupled Single-Supply Operation

VIDEO HDTV DRIVERS

The exceptional bandwidth and slew rate of the THS3201 matches the demands for professional video and HDTV. Most commercial HDTV standards requires a video passband of 30-MHz. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations—requiring 210-MHz 0.1-dB frequency flatness from the amplifier. High slew rates ensure there is minimal distortion of the video signal. Component video and RGB video signals require fast transition times and fast settling times to keep a high signal quality. The THS8135, for example, is a 240-MSPS video digital-to-analog converter (DAC) and has a transition time approaching 4 ns. The THS3201 is a perfect candidate for interfacing the output of such high-performance video components.

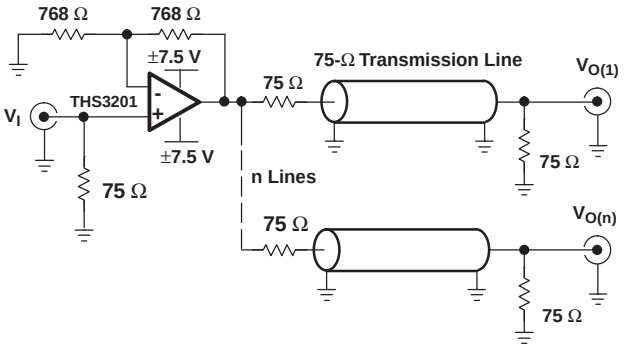


Figure 58. Video Distribution Amplifier Application

ADC DRIVER APPLICATION

The THS3201 can be used as a high-performance ADC driver in applications like radio receiver IF stages, and test and measurement devices. All high-performance ADCs have differential inputs. The THS3201 can be used in conjunction with a transformer as a drive amplifier in these applications. Figure 59 and Figure 60 show two different approaches.

In Figure 59, a transformer is used after the amplifier to convert the signal to differential. The advantage of this approach is fewer components are required. R_{OUT} and R_T are required for impedance matching the transformer.

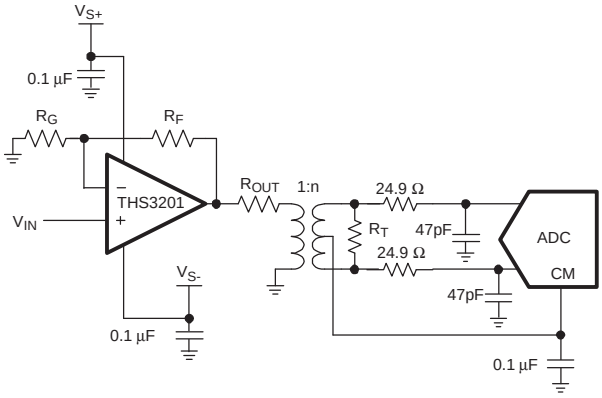


Figure 59. Differential ADC Driver Circuit 1

In Figure 60, a transformer is used before two amplifiers to convert the signal to differential. The two amplifiers then amplify the differential signal. The advantage to this approach is each amplifier is required to drive half the voltage as before. R_T is used to impedance match the transformer.

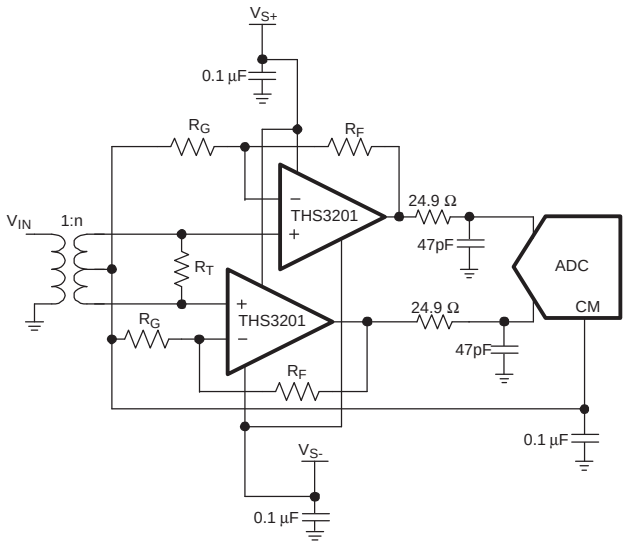


Figure 60. Differential ADC Driver Circuit 2

It is almost universally recommended to use a resistor and capacitor between the op amp output and the ADC input as shown in both figures.

This resistor-capacitor (RC) combination has multiple functions:

- The capacitor is a local charge reservoir for ADC
- The resistor isolates the amplifier from the ADC
- In conjunction, they form a low-pass noise filter

During the sampling phase, current is required to charge the ADC input sampling capacitors. By placing external capacitors directly at the input pins, most of the current is drawn from them. They are seen as a very low impedance source. They can be thought of as serving much the same purpose as a power-supply bypass capacitor to supply transient current, with the amplifier then providing the bulk charge.

Typically, a low-value capacitor in the range of 10 pF to 100 pF provides the required transient charge reservoir.

The capacitance and the switching action of the ADC is one of the worst loading scenarios that a high-speed amplifier encounters. The resistor provides a simple means of isolating the associated phase shift from the feedback network and maintaining the phase margin of the amplifier.

Typically, a low value resistor in the range of 10 Ω to 100 Ω provides the required isolation. Together, the R and C form a real pole in the s-plane located at the frequency:

$$f_P = \frac{1}{2\pi RC}$$

Placing this pole at about 10x the highest frequency of interest ensures it has no impact on the signal. Since the resistor is typically a small value, it is very bad practice to place the pole at (or very near) frequencies of interest. At the pole frequency, the amplifiers sees a load with a magnitude of:

$$\sqrt{2}\,xR$$

If R is only 10 Ω, the amplifier is very heavily loaded above the pole frequency, and generates excessive distortion.

DAC DRIVER APPLICATION

The THS3201 can be used as a high-performance DAC output driver in applications like radio transmitter stages and arbitrary waveform generators. All high-performance DACs have differential current outputs. Two THS3201s can be used as a differential drive amplifier in these applications, as shown in Figure 61.

R_{PU} on the DAC output is used to convert the output current to voltage. The 24.9-Ω resistor and 47-pF capacitor between each DAC output and the op amp input is used to reduce the images generated at multiples of the sampling rate. The values shown form a pole at 136 MHz. R_{OUT} sets the output impedance of each amplifier.

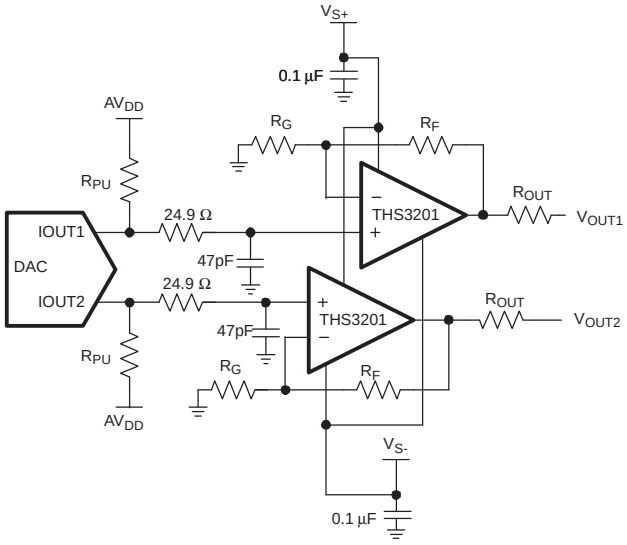


Figure 61. Differential DAC Driver Circuit

PRINTED CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high frequency amplifier-like devices in the THS3201 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any power or ground plane for the negative input and output pins by voiding the area directly below these pins and connecting traces and the feedback path. Parasitic capacitance on the output and negative input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins and the feedback path. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (<0.25") from the power-supply pins to high frequency 0.1-μF and 100 pF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (6.8 μF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the printed circuit board (PCB). The primary goal is to minimize the impedance seen in the differential-current return paths. For driving differential loads with the THS3201, adding a capacitor between the power-supply pins improves 2nd order harmonic distortion performance. This also minimizes the current loop formed by the differential drive.
- Careful selection and placement of external components preserve the high-frequency performance of the THS3201. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PCB trace length as short as possible. Never use wirebound type resistors in a high frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values >2.0 kΩ this parasitic capacitance can add a pole and/or a zero that can affect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S since the THS3201 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).
- A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3201 is used as well as a terminating shunt resistor at the input of the destination device.

  Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is un-acceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

- Socketing a high-speed part like the THS3201 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3201 parts directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS3201 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 62(a) and Figure 62(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 62(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface-mount with the, heretofore, awkward mechanical methods of heatsinking.

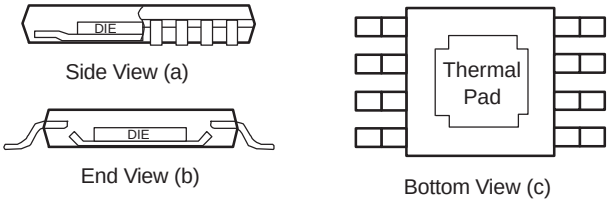


Figure 62. Views of Thermally-Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

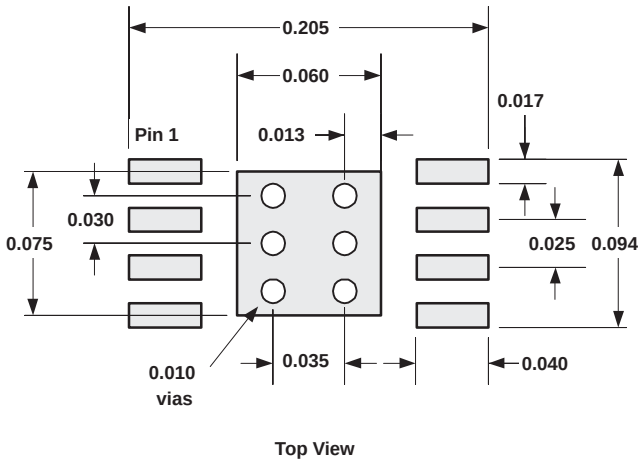


Figure 63. DGN PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 63. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS3201 IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3201 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from

being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

To maintain maximum output capabilities, the THS3201 does not incorporate automatic thermal shutoff protection. The designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of +150°C is exceeded. For best performance, design for a maximum junction temperature of +125°C. Between +125°C and +150°C, damage does not occur, but the performance of the amplifier begins to degrade.

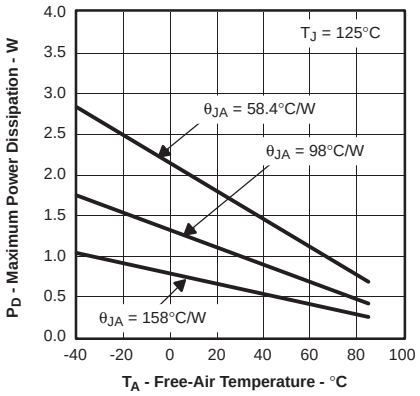
The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

Where:

- P_{DMax} is the maximum power dissipation in the amplifier (W)
- T_{Max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to the ambient air (°C/W)

For systems where heat dissipation is more critical, the THS3201 is offered in an 8-pin MSOP with PowerPAD and also available in the SOIC-8 PowerPAD package, offering even better thermal performance. The thermal coefficients for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note number SLMA002. The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3"x3"
θ_{JA} = 58.4°C/W for 8-Pin MSOP w/PowerPad (DGN)
θ_{JA} = 98°C/W for 8-Pin SOIC High Test PCB (D)
θ_{JA} = 158°C/W for 8-Pin MSOP w/PowerPad w/o Solder

Figure 64. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Evaluation Fixture, Spice Models, and Applications Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal an evaluation board has been developed for the THS3201 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments web site at www.ti.com, or through your local Texas Instruments sales representative. The schematic diagram, board layers, and bill of materials of the evaluation boards are provided below.

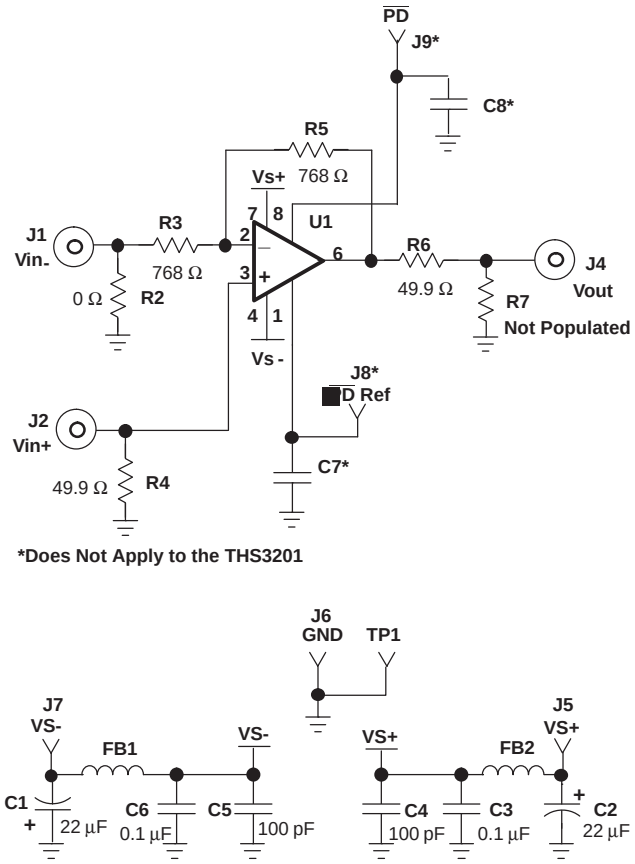


Figure 65. THS3201 EVM Circuit Configuration

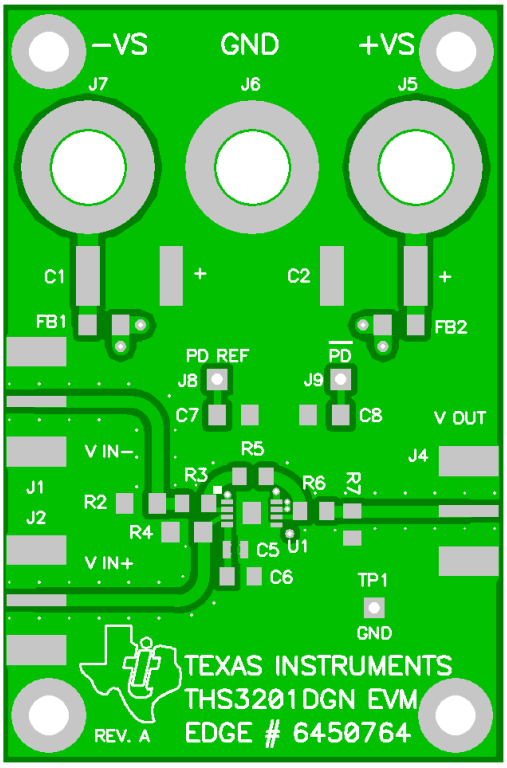


Figure 66. THS3201 EVM Board Layout (Top Layer)

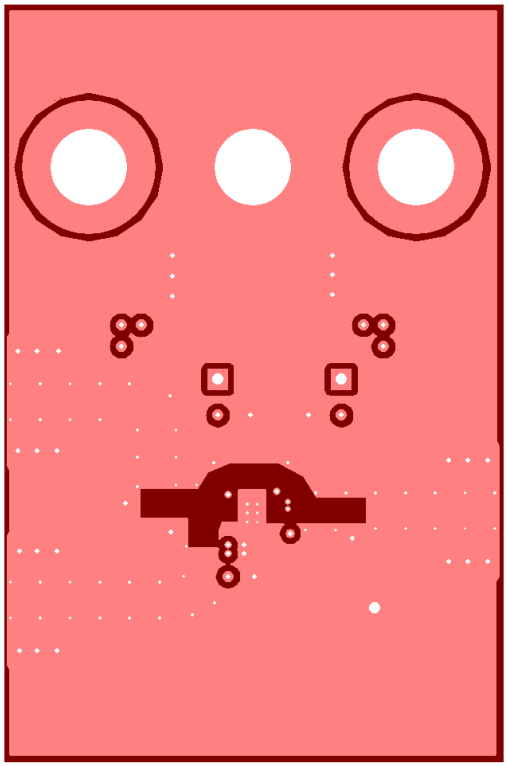


Figure 67. THS3201 EVM Board Layout (Second Layer, Ground)

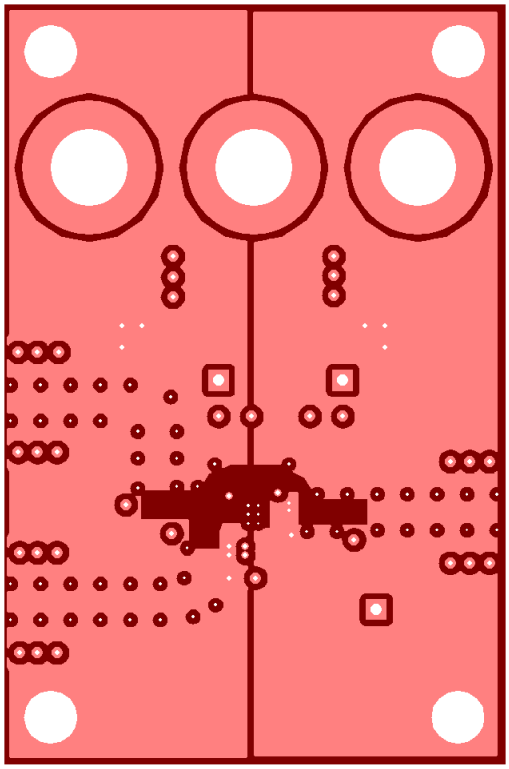


Figure 68. THS3201 EVM Board Layout (Third Layer, Power)

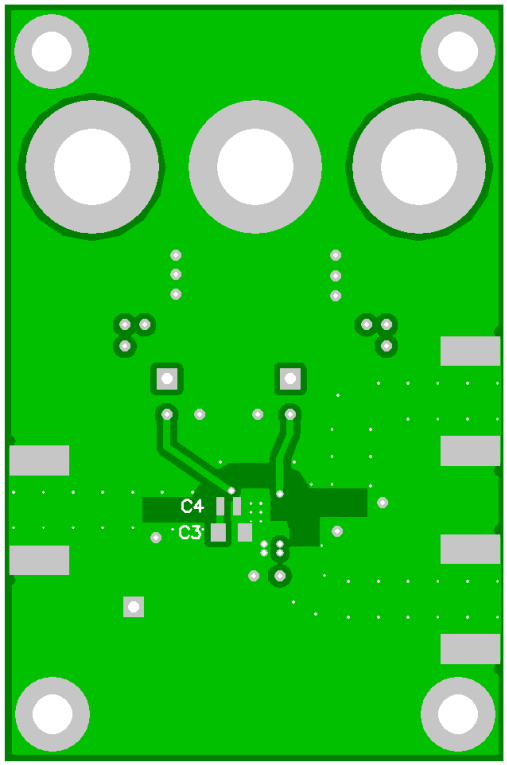


Figure 69. THS3201 EVM Board Layout (Bottom Layer)

Table 2. Bill of Materials(1)

THS3201DGN EVM					
ITEM	**DESCRIPTION**	**SMD SIZE**	**REF DES**	**PCB QUANTITY**	**MANUFACTURER'S PART NUMBER**
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00
2	Cap, 22 µF, tanatalum, 25 V, 10%	D	C1, C2	2	(AVX) TAJD226K025R
3	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C4, C5	2	(AVX) AQ12EM101JAJME
4	Cap, 0.1 µF, ceramic, X7R, 50 V	0805	C3, C6	2	(AVX) 08055C104KAT2A
6	Open	0805	R7	1	
7	Resistor, 49.9 Ω, 1/8 W, 1%	0805	R6	1	(Phycomp) 9C08052A49R9FKHFT
9	Resistor, 768 Ω, 1/8 W, 1%	0805	R3, R5	2	(Phycomp) 9C08052A7680FKHFT
10	Open	1206	C7, C8	2	
11	Resistor, 0 Ω, 1/4 W, 1%	1206	R2	1	(KOA) RK73Z2BLTD
12	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R4	1	(Phycomp) 9C12063A49R9FKRFT
13	Test point, black		TP1	1	(Keystone) 5001
14	Open		J8, J9	2	
15	Jack, Banana Receptance, 0.25” dia. hole		J5, J6, J7	3	(HH Smith) 101
16	Connector, edge, SMA PCB jack		J1, J2, J4	3	(Johnson) 142-0701-801
17	Standoff, 4-40 hex, 0.625” length			4	(Keystone) 1804
18	Screw, Phillips, 4-40, .250”			4	SHR-0440-016-SN
19	IC, THS3201		U1	1	(TI) THS3201DGN
20	Board, printed circuit			1	(TI) Edge # 6447972 Rev.A

(1) The components shown in the BOM were used in test by TI.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and R_F-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS3201 family of devices is available through the Texas Instruments web site (www.ti.com). The Product Information Center (PIC) is available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

ADDITIONAL REFERENCE MATERIAL

- PowerPAD Made Easy, application brief (SLMA004)
- PowerPAD Thermally Enhanced Package, technical brief (SLMA002)
- Voltage Feedback vs Current-Feedback Amplifiers (SLVA051)
- Current-Feedback Analysis and Compensation (SLOA021)
- Current-Feedback Amplifiers: Review, Stability, and Application (SBOA081)
- Effect of Parasitic Capacitance in Op Amp Circuits (SLOA013)

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage and the output voltage ranges as specified in the table below.

Input Range, V_S	6.6 V (±3.3V) to 16.5V (±8.25V)
Input Range, V_I	NOT TO EXCEED: Power-Supply Voltage Applied
Output Range, V_O	NOT TO EXCEED: Power-Supply Voltage Applied

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +125°C. The EVM is designed to operate properly with certain components above +125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2008) to Revision C **Page**

- Changed 5-V Step to 10-V Step in second bullet of *Features* list 1
- Deleted lead temperature row from *Absolute Maximum Ratings* table 2

Changes from Revision A (January, 2004) to Revision B **Page**

- Updated document format 1
- Updated *Features*, *Applications*, and *Description* sections 1
- Updated Package/Ordering Information 3
- Changed ±7.5-V slew rate typical values 4
- Changed ±7.5-V rise and fall time typical values 4
- Changed ±7.5-V 2nd-order harmonic typical values 4
- Changed ±7.5-V 3rd-order harmonic typical values 4
- Deleted ±7.5-V 3rd-order intermodulation distortion specifications 4
- Changed ±5-V slew rate typical values 6
- Changed ±5-V rise and fall time typical values 6
- Changed ±5-V 2nd-order harmonic typical values 6
- Changed ±5-V 3rd-order harmonic typical values 6
- Deleted ±5-V 3rd-order intermodulation distortion specifications 6
- Added Figure 9 through Figure 17; updated Figure 25 8
- Added Figure 40 through Figure 48; added Figure 51 9
- Deleted *Power Supply* section 19
- Updated first paragraph in *Printed Circuit Board Layout* section 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3201D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3201	
THS3201DBVT	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEO	
THS3201DBVTG4	NRND	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEO	
THS3201DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3201	
THS3201DGK	NRND	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	BGP	
THS3201DGN	NRND	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEN	
THS3201DGNG4	NRND	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEN	
THS3201DGNR	NRND	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEN	
THS3201DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3201	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF THS3201 :

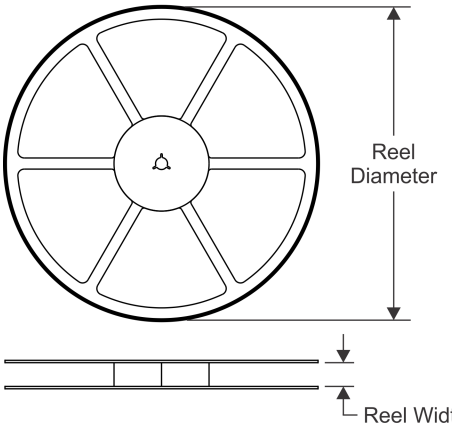
- Enhanced Product: THS3201-EP

NOTE: Qualified Version Definitions:

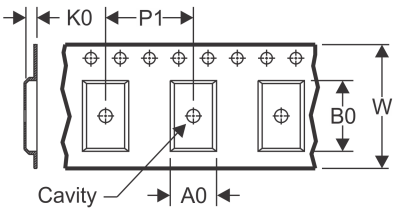
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

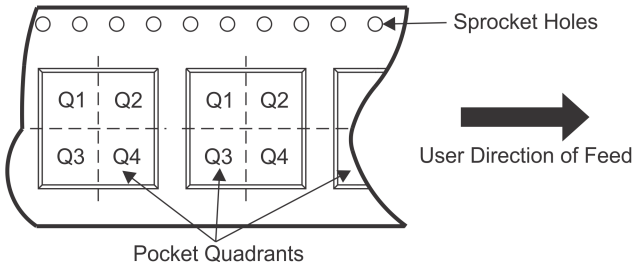


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

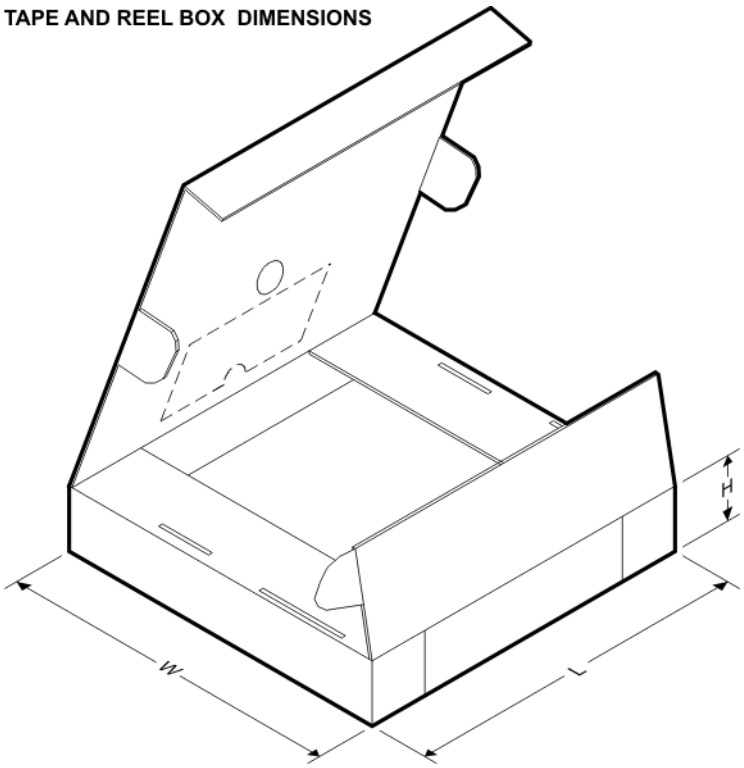
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3201DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS3201DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3201DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

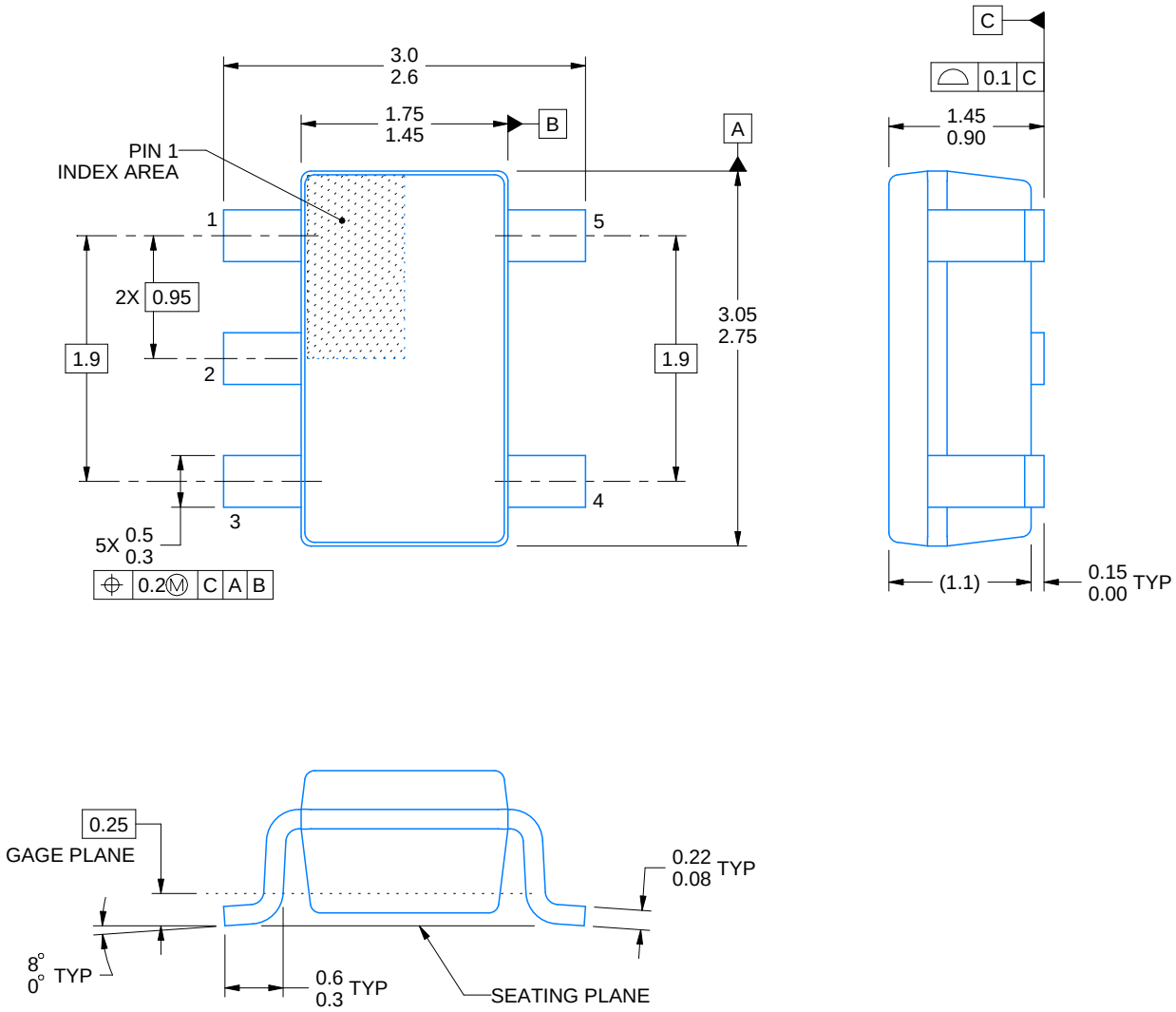
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3201DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
THS3201DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS3201DR	SOIC	D	8	2500	350.0	350.0	43.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

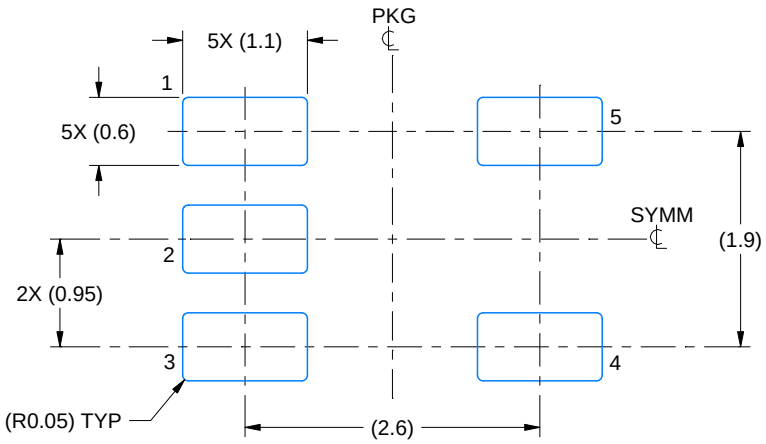
SMALL OUTLINE TRANSISTOR



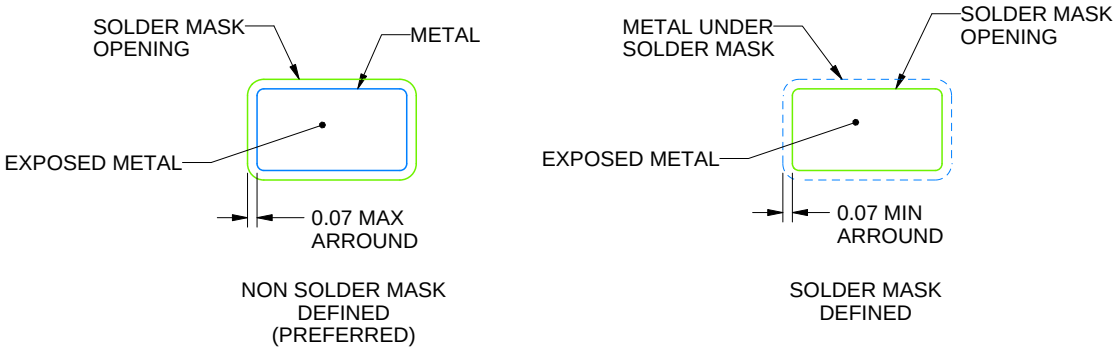
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

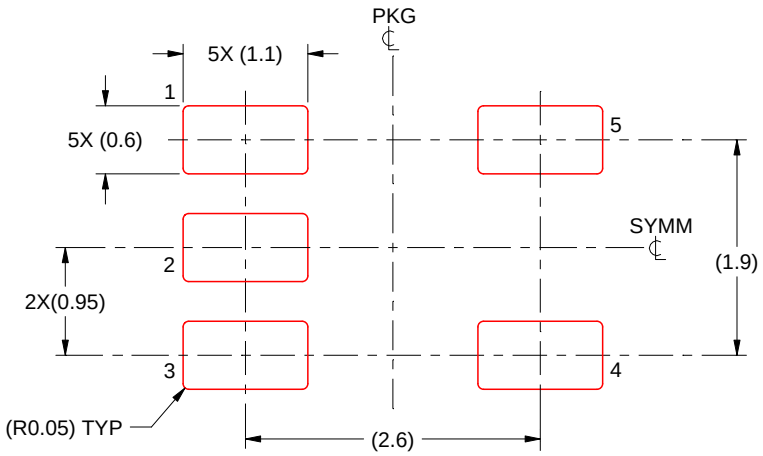


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

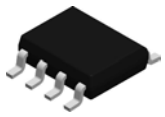


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

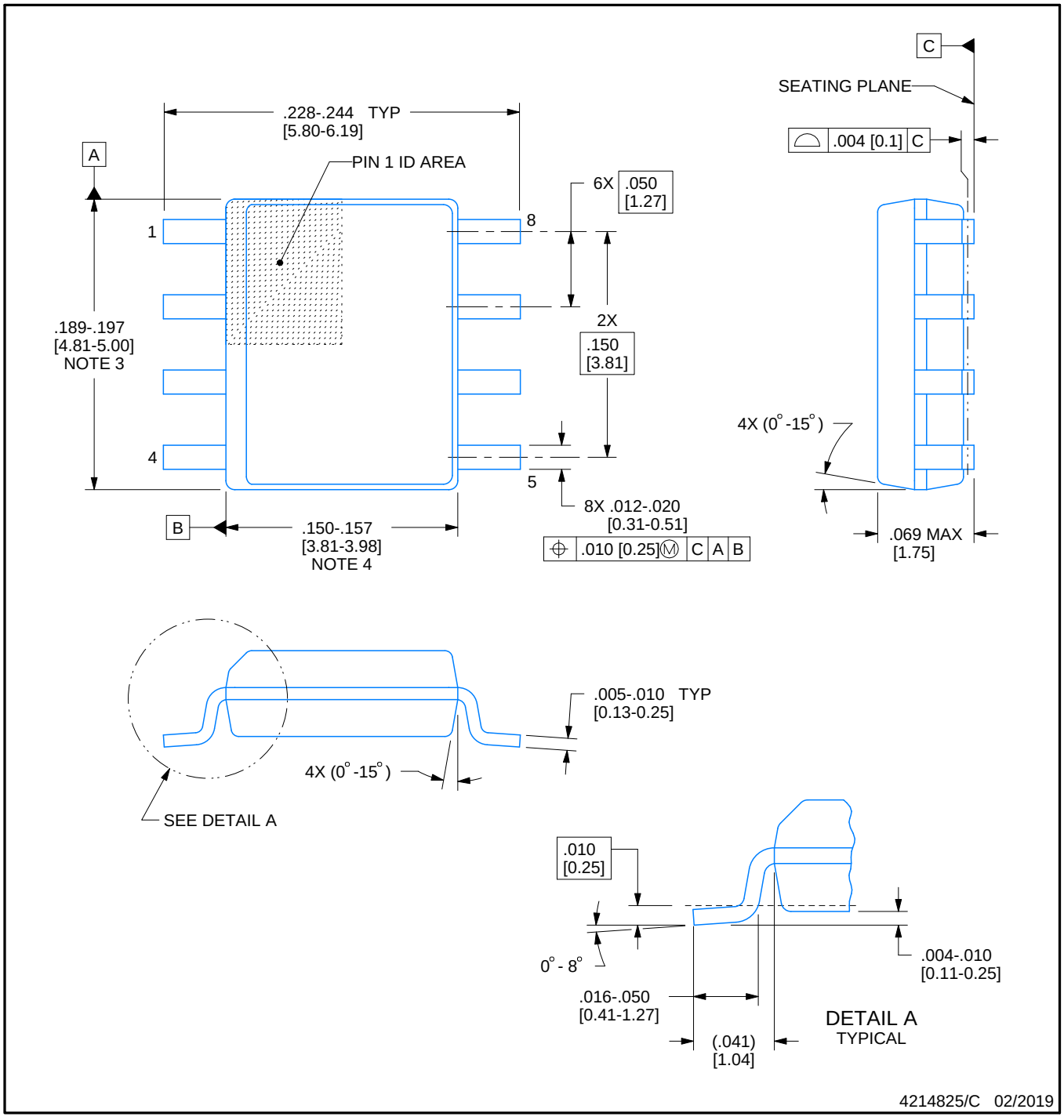


PACKAGE OUTLINE

D0008A

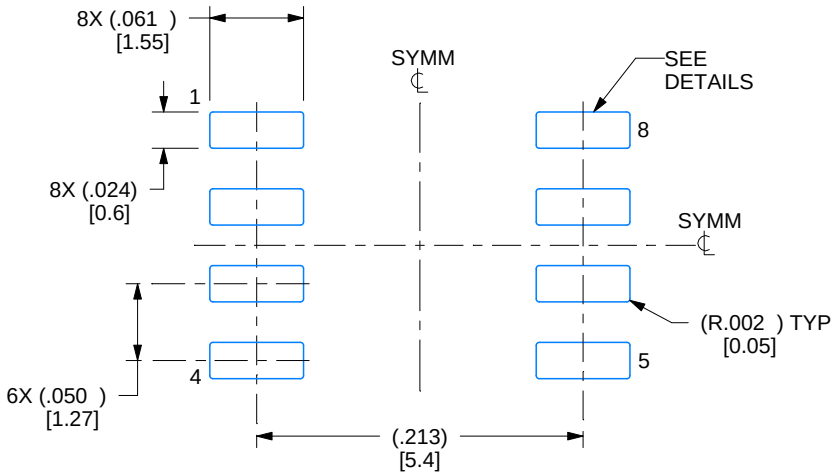
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

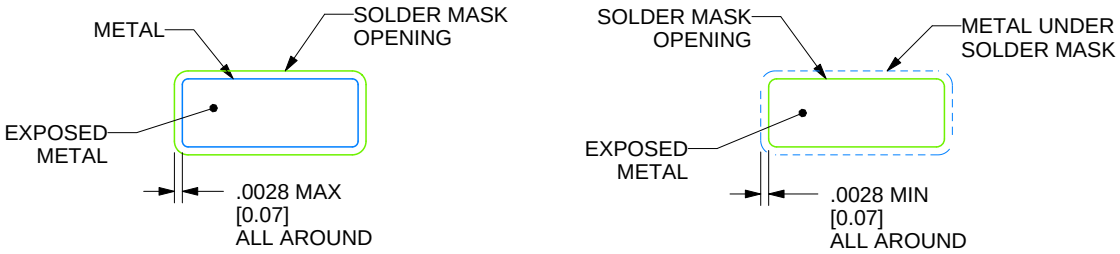


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

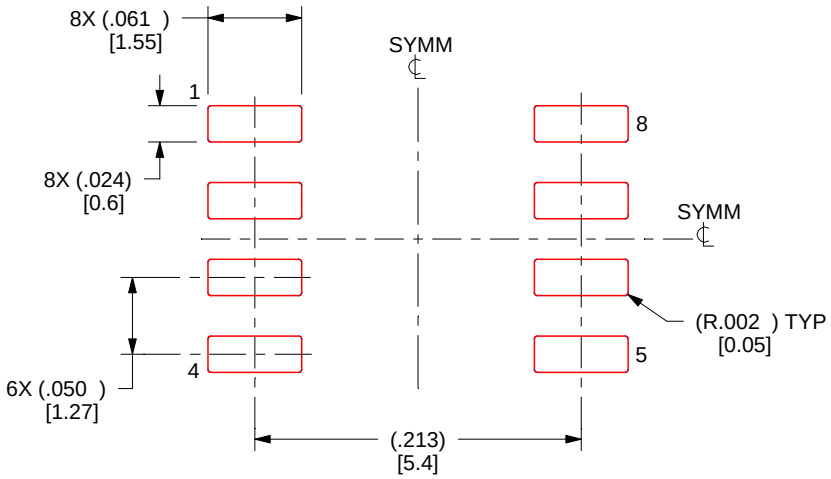
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



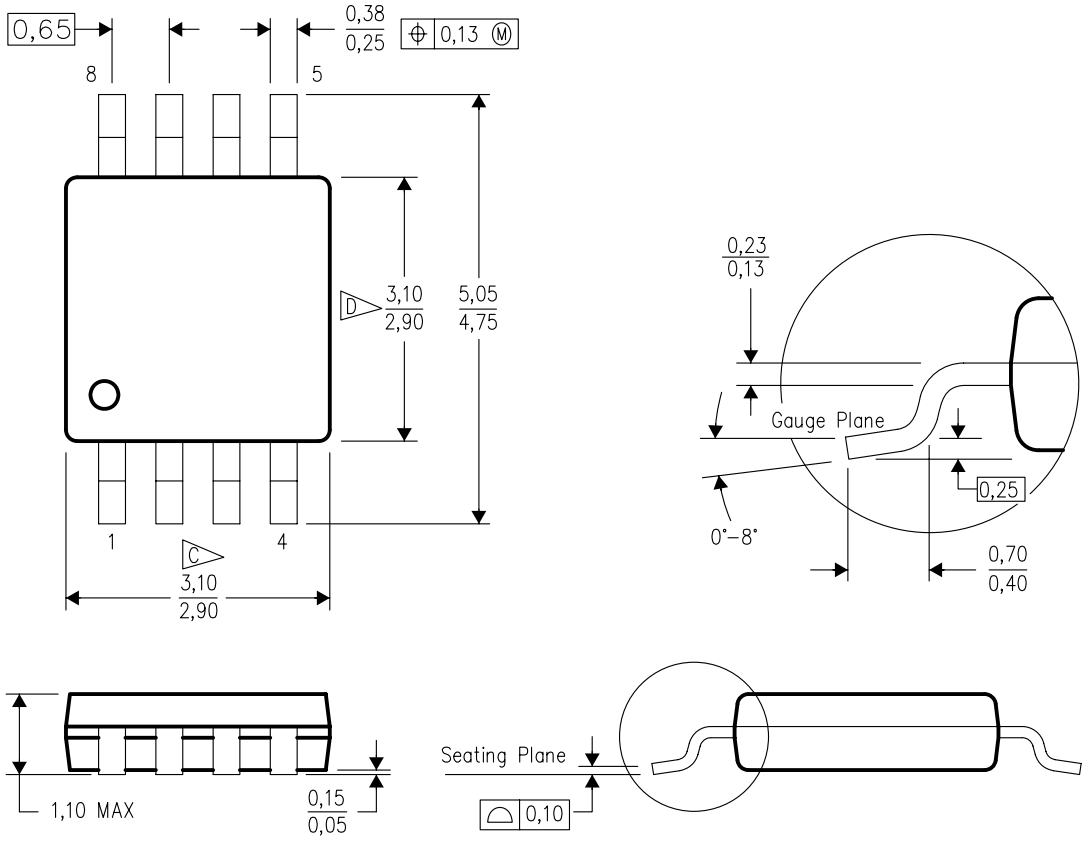
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

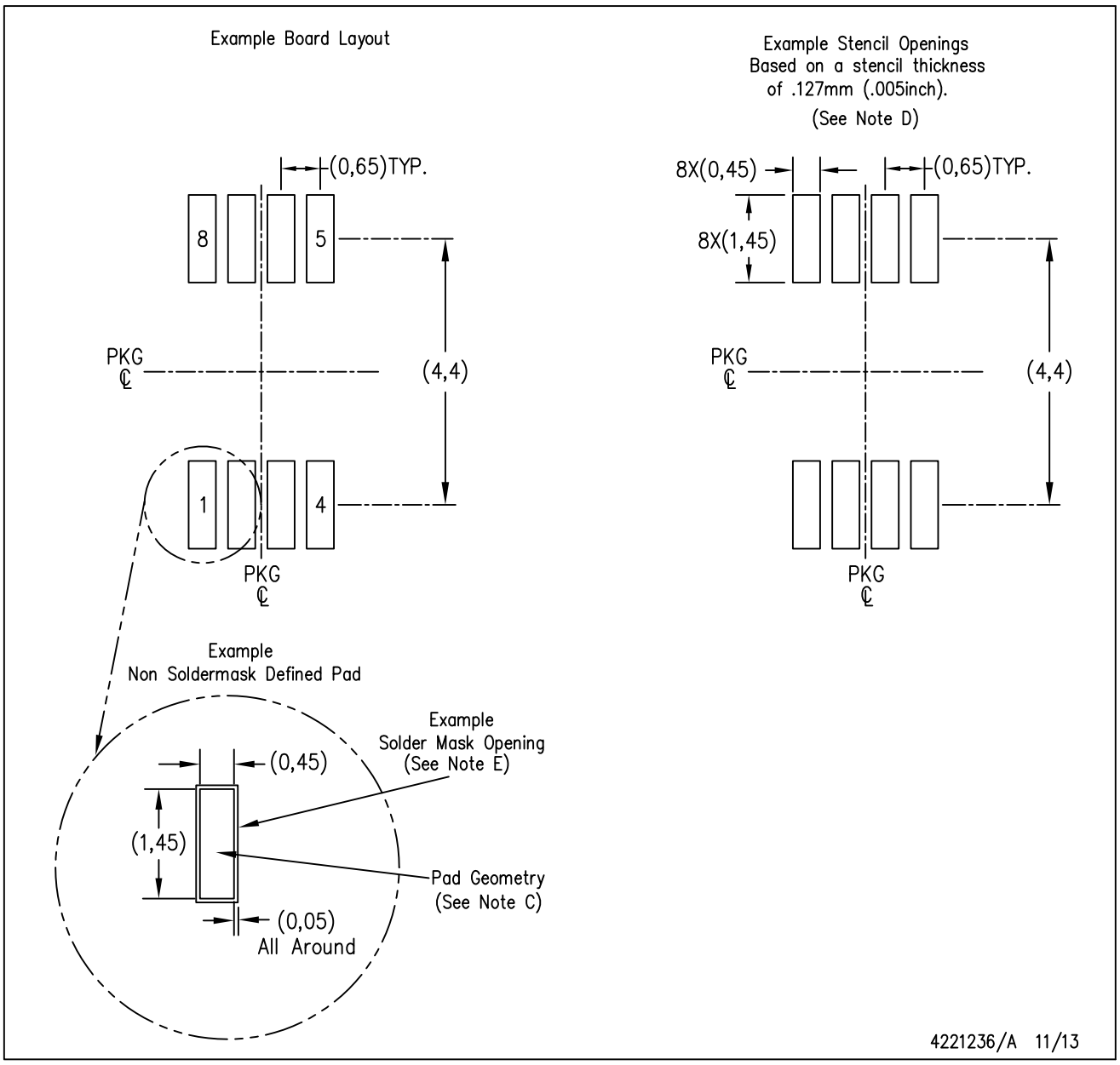
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

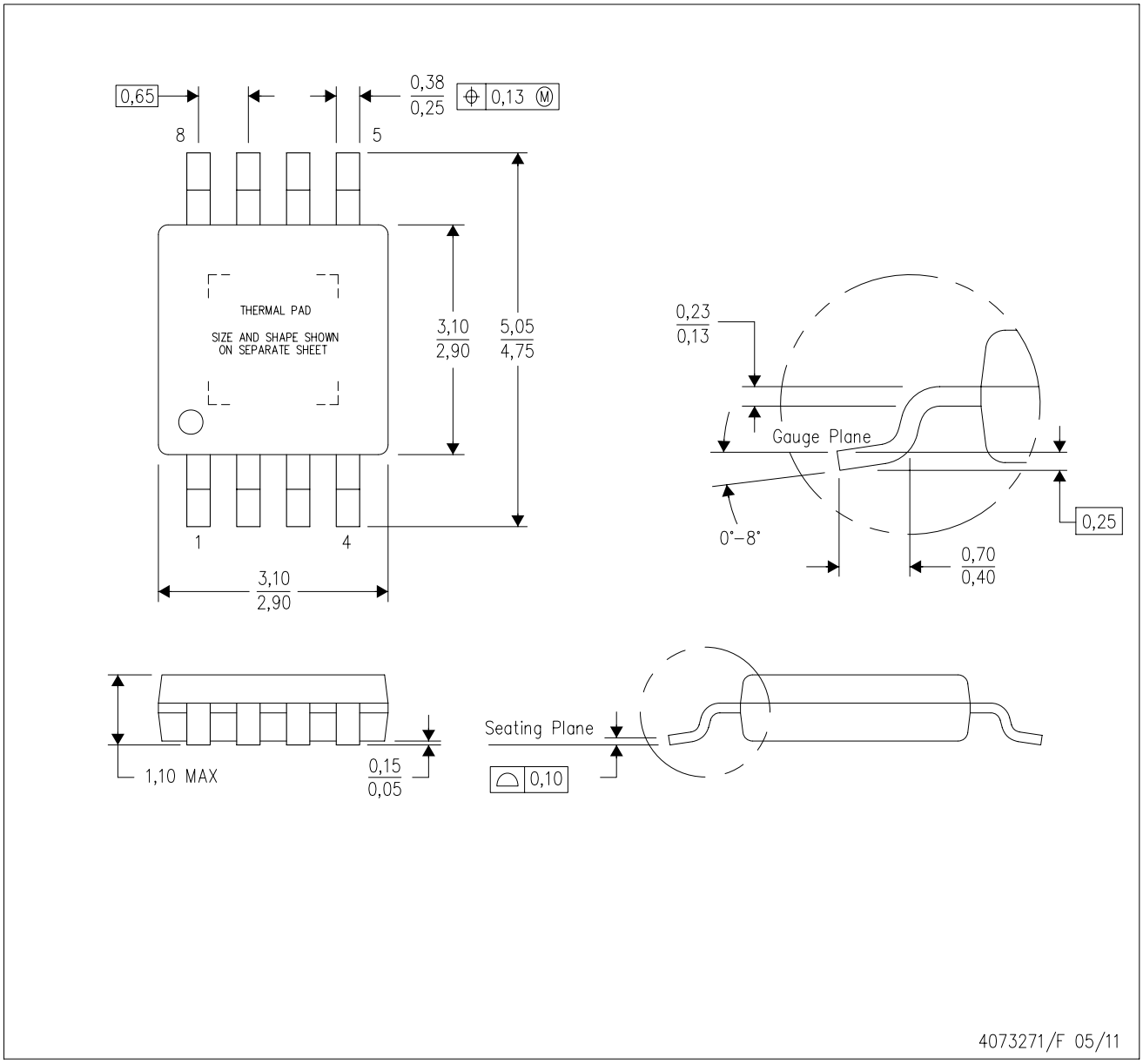
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

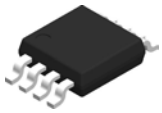


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

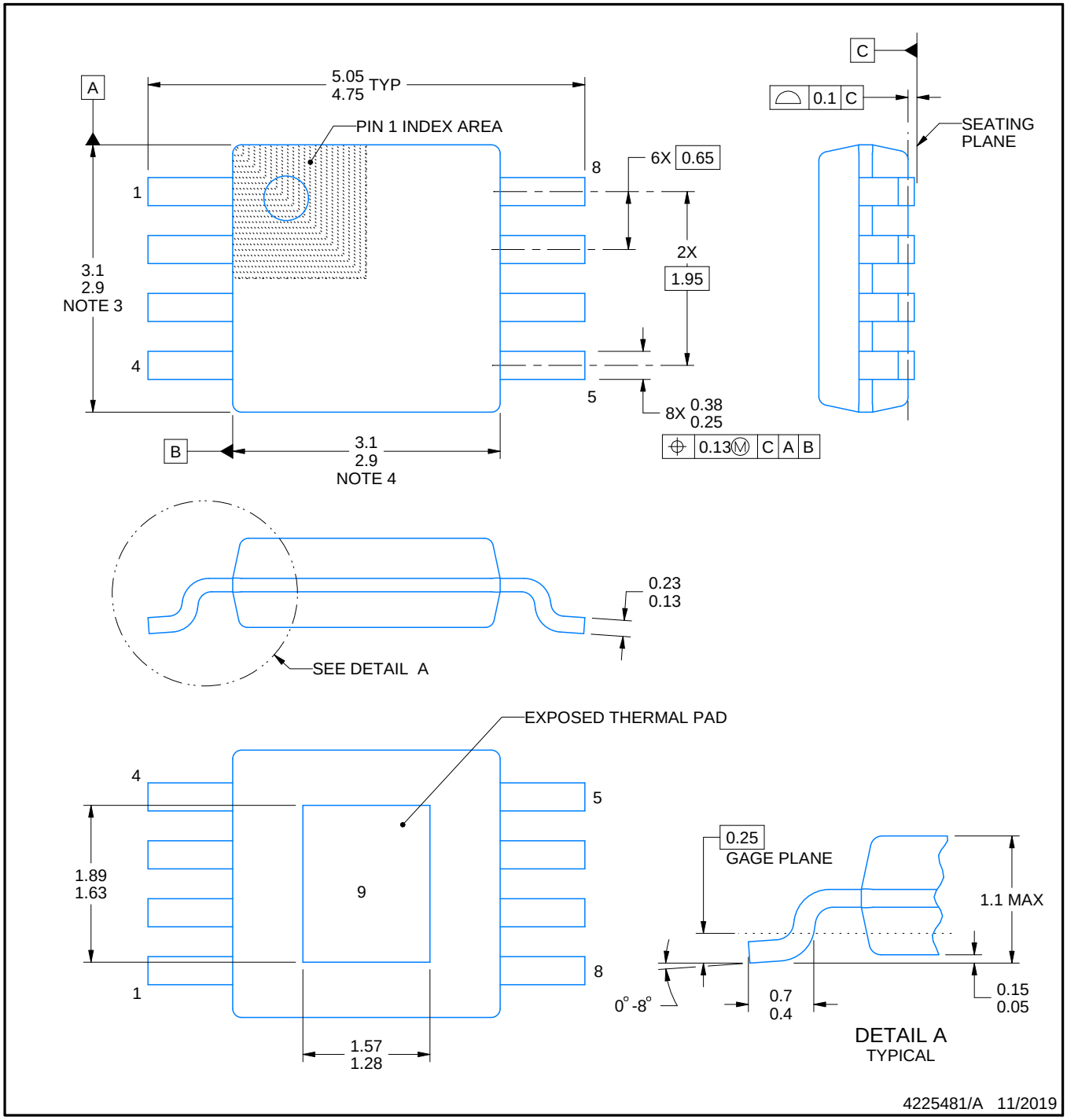
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

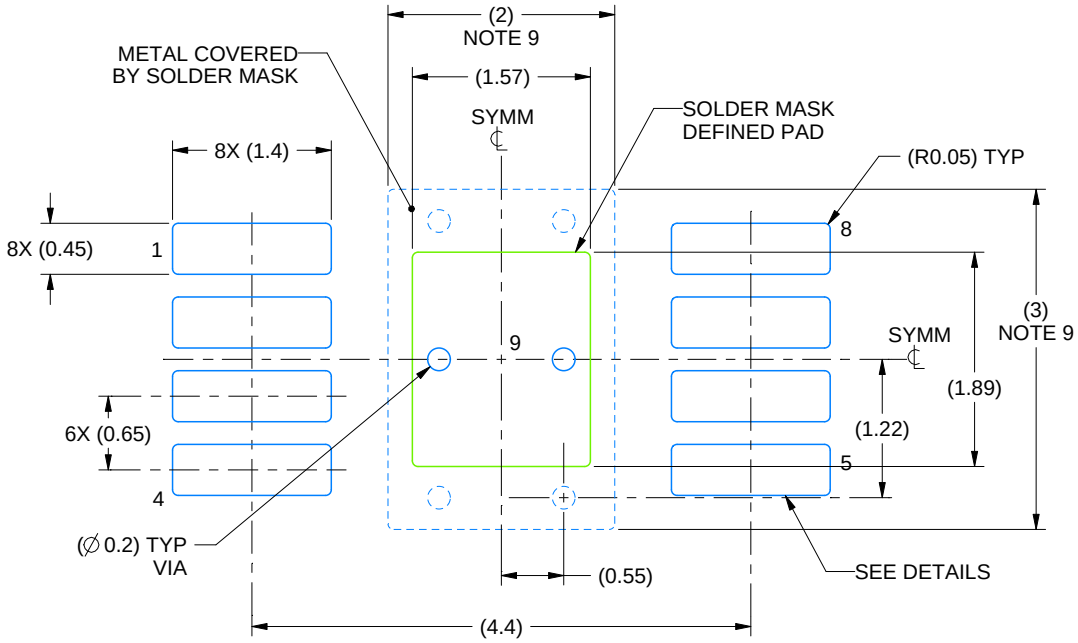
SMALL OUTLINE PACKAGE



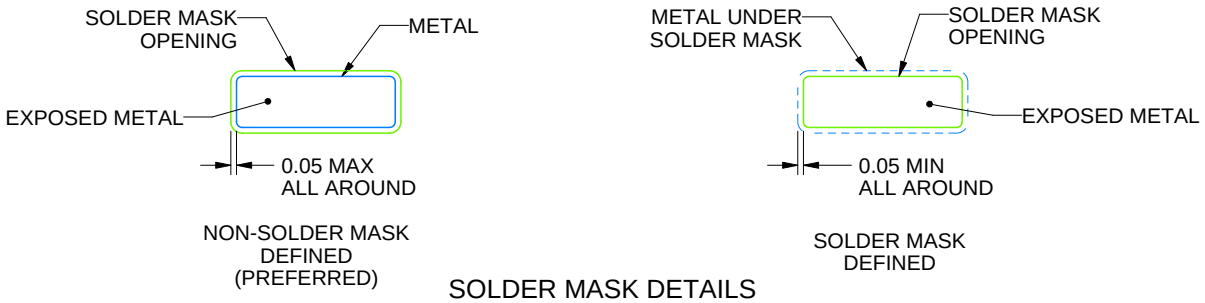
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

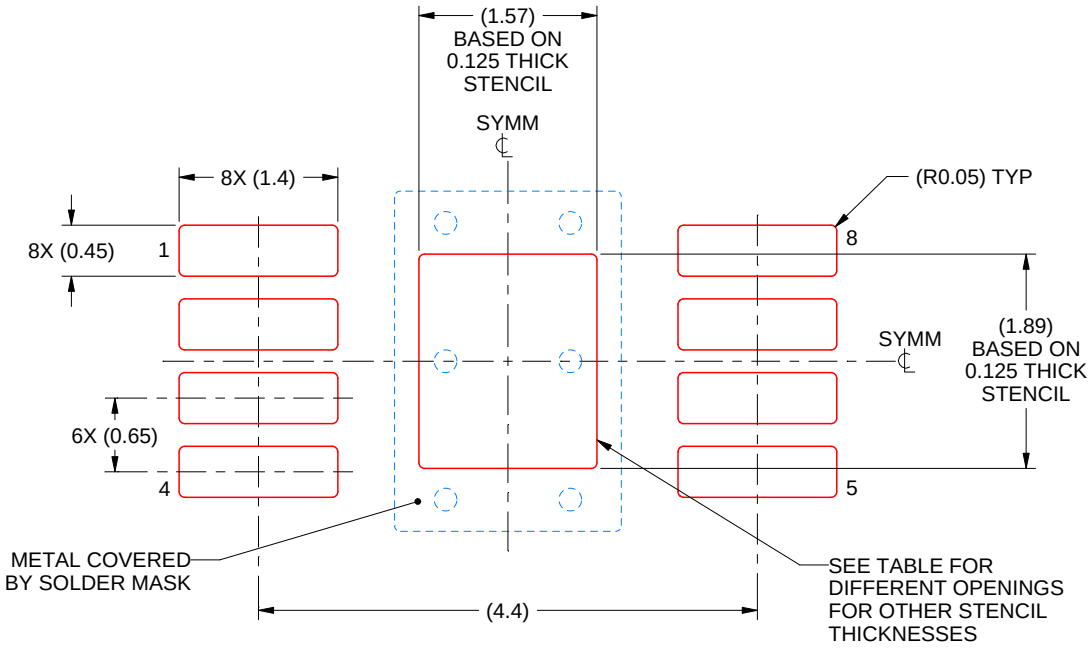


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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