

CD4001UB Types

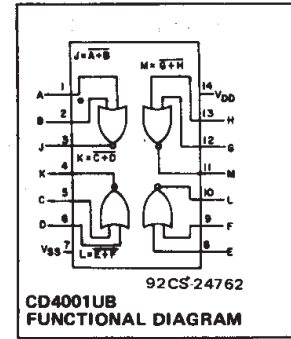
CMOS Quad 2-Input NOR Gate High-Voltage Types (20-Volt Rating)

■ CD4001UB quad 2-input NOR gate provides the system designer with direct implementation of the NOR function and supplements the existing family of CMOS gates.

The CD4001UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Propagation delay time = 30 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings



STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0.5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μ A
	—	0.10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0.15	15	1	1	30	30	—	0.01	1	
	—	0.20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0.5	5	0.05				—	0	0.05	V
	—	0.10	10	0.05				—	0	0.05	
	—	0.15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0.5	5	4.95				4.95	5	—	V
	—	0.10	10	9.95				9.95	10	—	
	—	0.15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1				—	—	1	V
	1, 9	—	10	2				—	—	2	
	1.5, 13.5	—	15	2.5				—	—	2.5	
Input High Voltage, V _{IH} Min.	0.5	—	5	4				4	—	—	V
	1	—	10	8				8	—	—	
	1.5	—	15	12.5				12.5	—	—	
Input Current I _{IN} Max.	—	0.18	18	± 0.1	± 0.1	± 1	± 1	—	$\pm 10^{-5}$	± 0.1	μ A

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4001UB Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max $+265^\circ\text{C}$

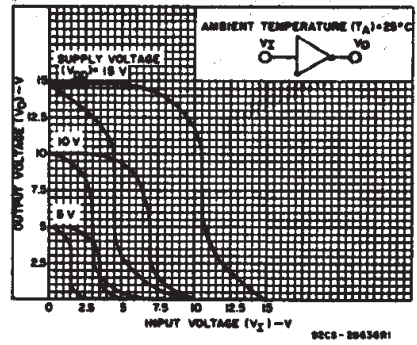


Fig. 1 - Minimum and maximum voltage transfer characteristics.

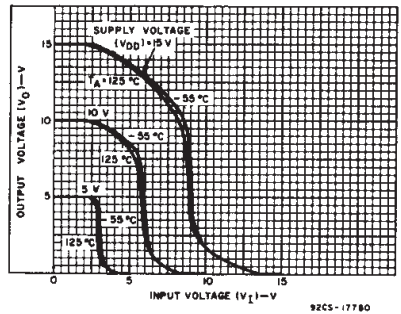


Fig. 2 - Typical voltage transfer characteristics as a function of temperature.

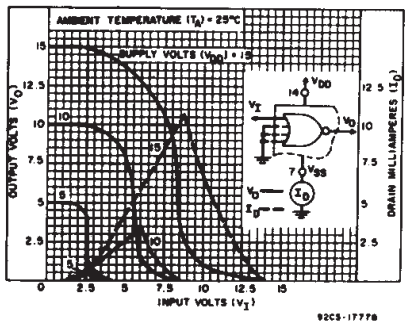


Fig. 3 - Typical current & voltage transfer characteristics.

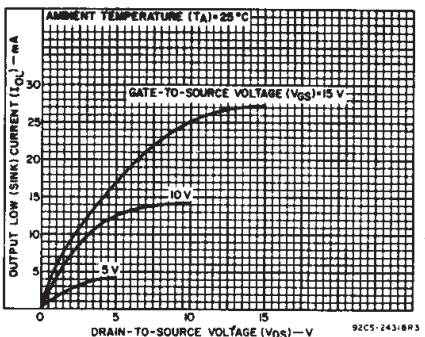


Fig. 5 - Typical output low (sink) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20$ ns, and $C_L = 50$ pF, $R_L = 200$ K Ω

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V_{DD} Volts	TYP.		MAX.
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{iN}	Any Input		10	15	pF

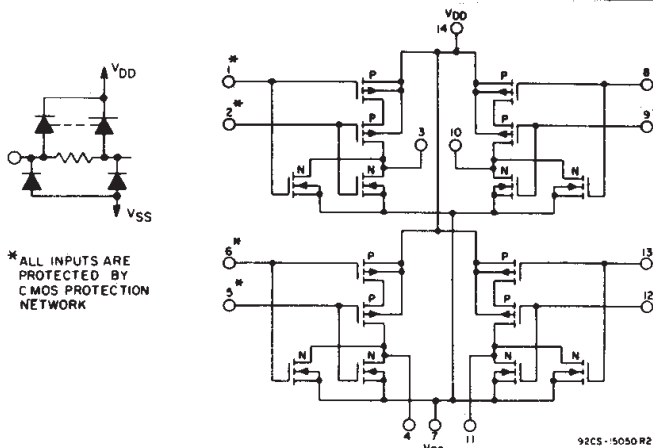


Fig. 4 - Schematic diagram for type CD4001UB.

CD4001UB Types

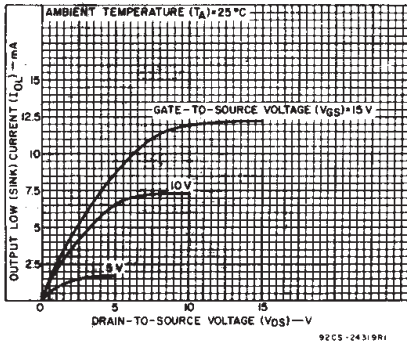


Fig. 6 - Minimum output low (sink) current characteristics.

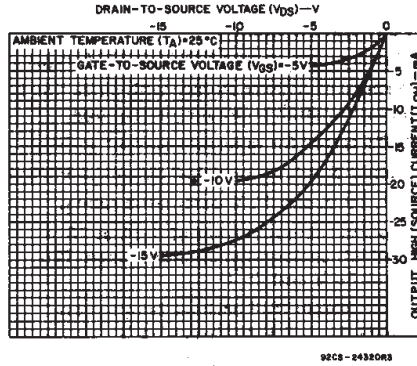


Fig. 7 - Typical output high (source) current characteristics.

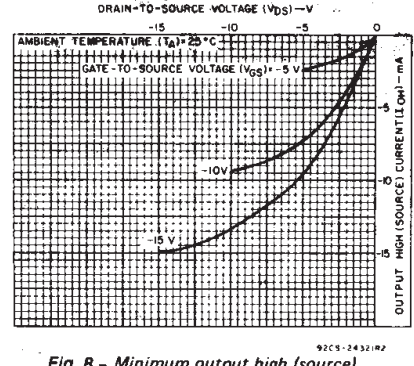


Fig. 8 - Minimum output high (source) current characteristics.

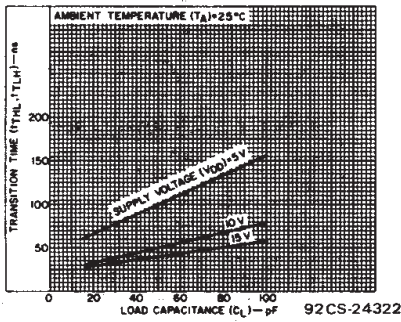


Fig. 9 - Typical transition time vs. load capacitance.

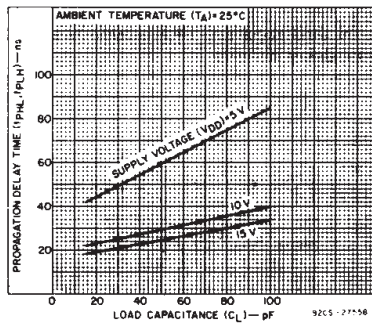


Fig. 10 - Typical propagation delay time vs. load capacitance.

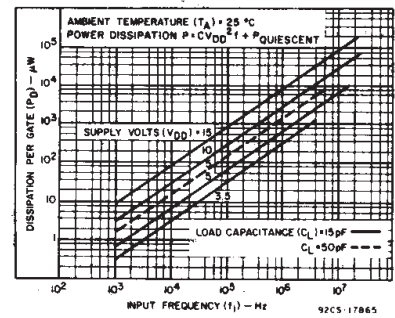


Fig. 11 - Typical power dissipation vs. frequency.

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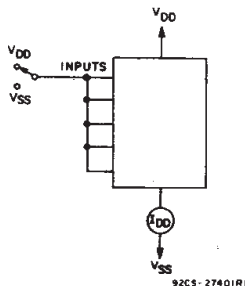


Fig. 12 - Quiescent device current test circuit.

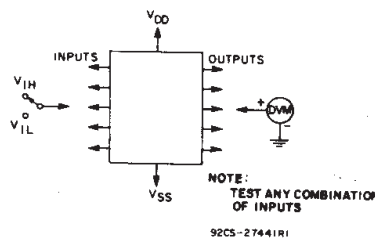


Fig. 13 - Input voltage test circuit.

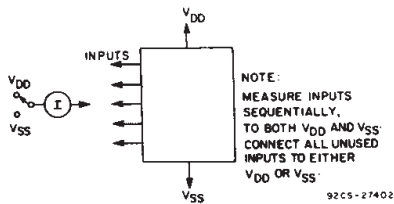
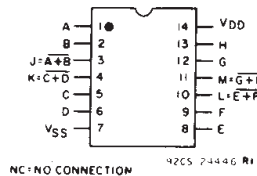


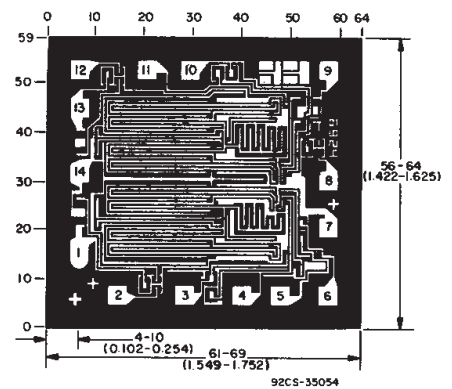
Fig. 14 - Input leakage current test circuit.

TERMINAL ASSIGNMENT



CD4001UB

CHIP Dimensions and Pad Layout



CD4001UB

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4001UBE	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4001UBE	Samples
CD4001UBEE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD4001UBE	Samples
CD4001UBF	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD4001UBF	Samples
CD4001UBF3A	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD4001UBF3A	Samples
CD4001UBM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001UBM	Samples
CD4001UBM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4001UBM	Samples
CD4001UBPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM001UB	Samples
CD4001UBPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM001UB	Samples
CD4001UBPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM001UB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4001UB, CD4001UB-MIL :

- Catalog: [CD4001UB](#)
- Military: [CD4001UB-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4001UBM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4001UBPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4001UBM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4001UBPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

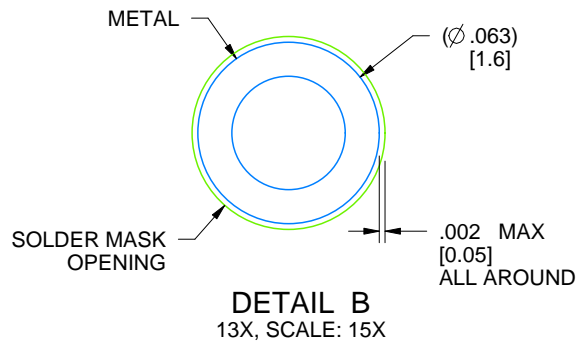
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



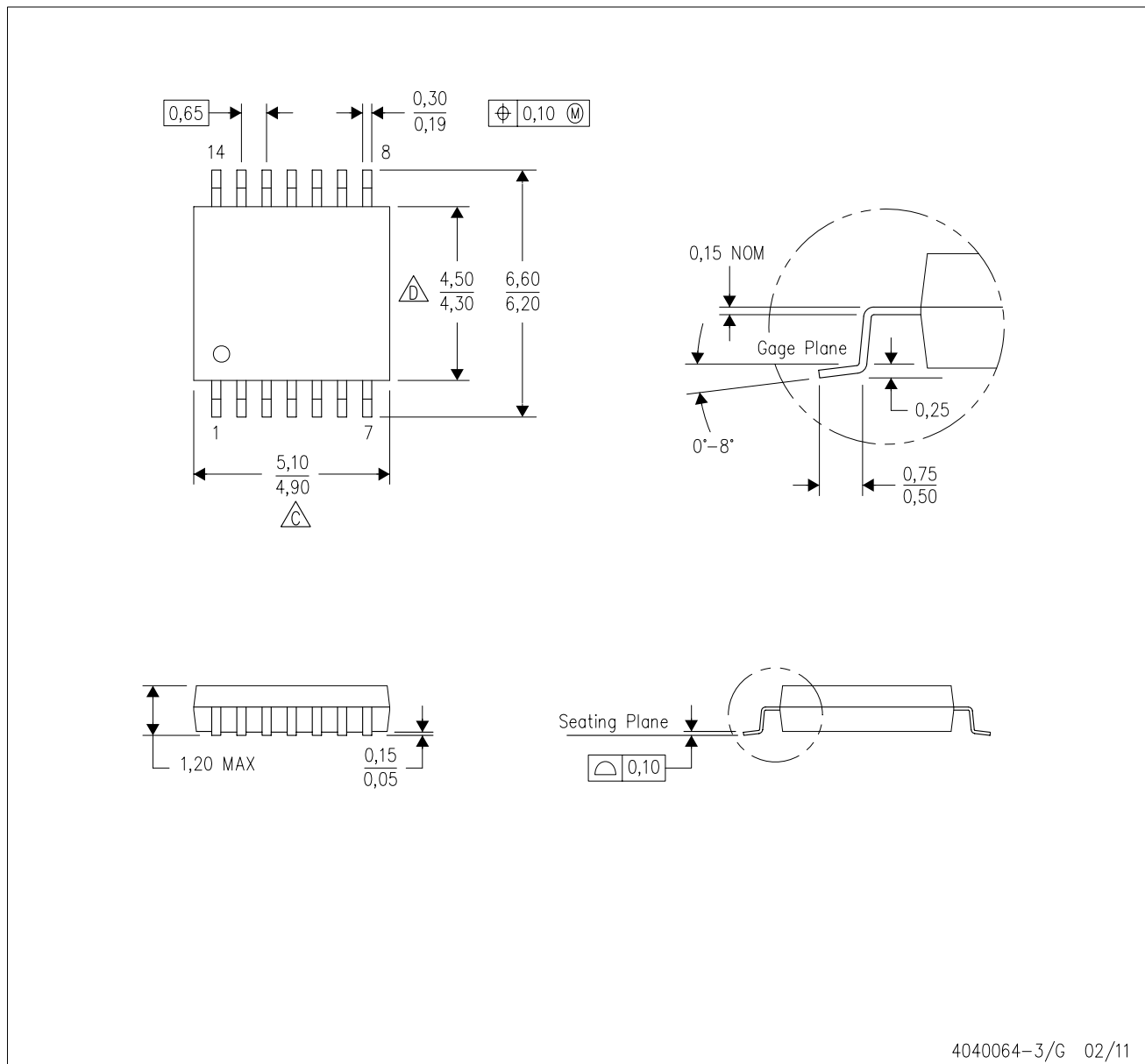
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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