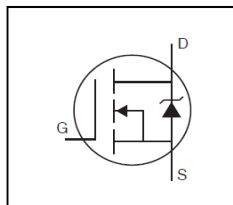


**Features**

- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

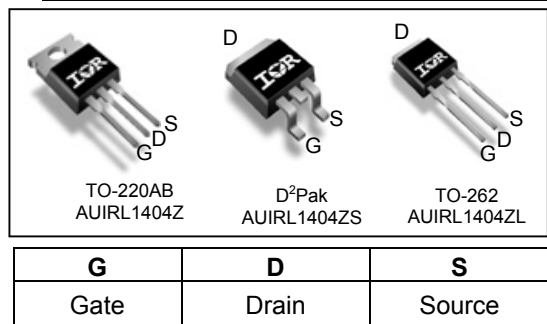


HEXFET® Power MOSFET

<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>2.5mΩ</b>
	<b>max.</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>180A<sup>Ⓢ</sup></b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>160A</b>

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRL1404Z	TO-220	Tube	50	AUIRL1404Z
AUIRL1404ZL	TO-262	Tube	50	AUIRL1404ZL
AUIRL1404ZS	D <sup>2</sup> -Pak	Tube	50	AUIRL1404ZS
		Tape and Reel Left	800	AUIRL1404ZSTRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	180 <sup>Ⓢ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	130	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	160	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup>	790	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 16	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) <sup>②</sup>	190	mJ
E <sub>AS</sub> (tested)	Single Pulse Avalanche Energy Tested Value <sup>⑥</sup>	490	
I <sub>AR</sub>	Avalanche Current <sup>①</sup>	See Fig.15,16, 12a, 12b	A
E <sub>AR</sub>	Repetitive Avalanche Energy <sup>⑤</sup>		mJ
T <sub>J</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T <sub>STG</sub>			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	0.75 <sup>Ⓢ</sup>	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface <sup>⑦</sup>	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient <sup>⑦</sup>	—	62	
R <sub>θJA</sub>	Junction-to-Ambient ( PCB Mount, steady state) <sup>⑦</sup>	—	40	

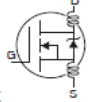
HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

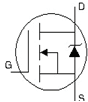
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.034	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.5	3.1	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A ③**
		—	—	4.7		V <sub>GS</sub> = 5.0V, I <sub>D</sub> = 40A ③
		—	—	5.9		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 40A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.4	—	2.7	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Trans conductance	120	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 75A**
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -16V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

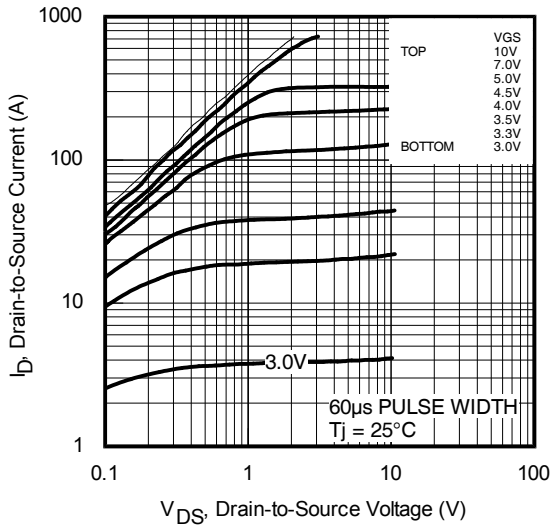
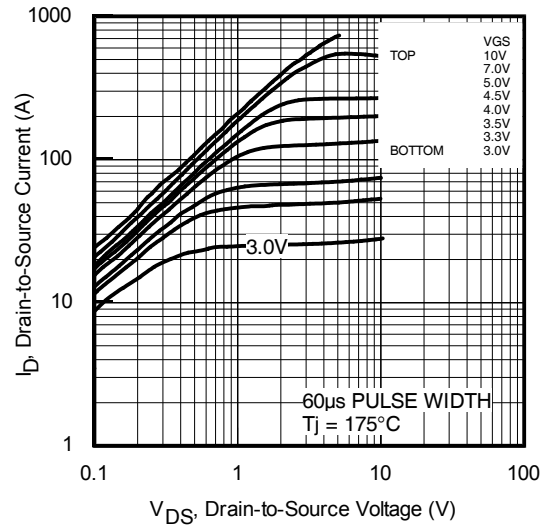
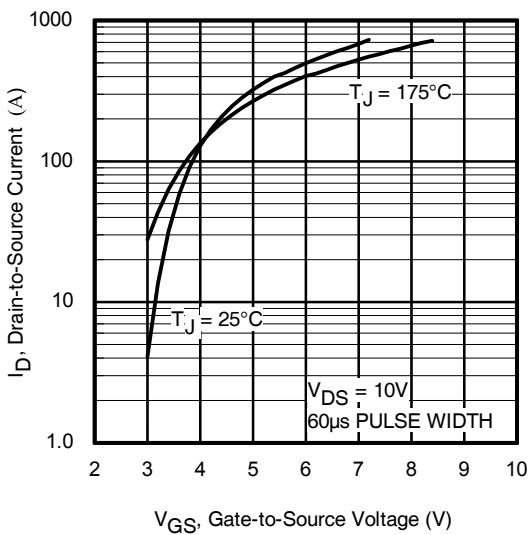
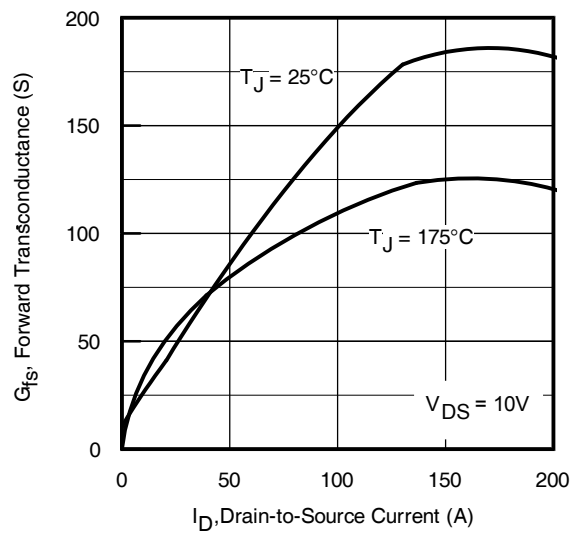
Q <sub>g</sub>	Total Gate Charge	—	75	110	nC	I <sub>D</sub> = 75A** V <sub>DS</sub> = 32V V <sub>GS</sub> = 5.0V ③
Q <sub>gs</sub>	Gate-to-Source Charge	—	28	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	40	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	19	—	ns	V <sub>DD</sub> = 20V I <sub>D</sub> = 75A** R <sub>G</sub> = 4.0Ω, V <sub>GS</sub> = 5.0V ③
t <sub>r</sub>	Rise Time	—	180	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	30	—		
t <sub>f</sub>	Fall Time	—	49	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	5080	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 32V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V ④
C <sub>oss</sub>	Output Capacitance	—	970	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	570	—		
C <sub>oss</sub>	Output Capacitance	—	3310	—		
C <sub>oss</sub>	Output Capacitance	—	870	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	1280	—		

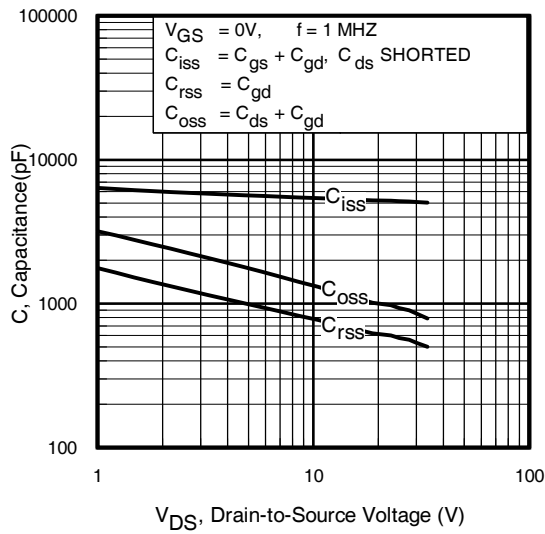
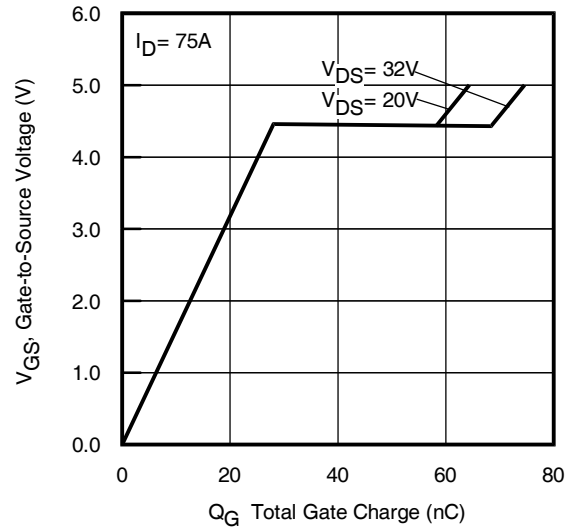
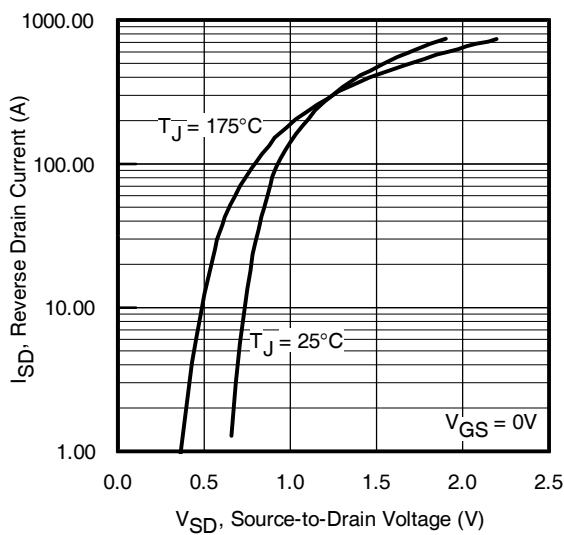
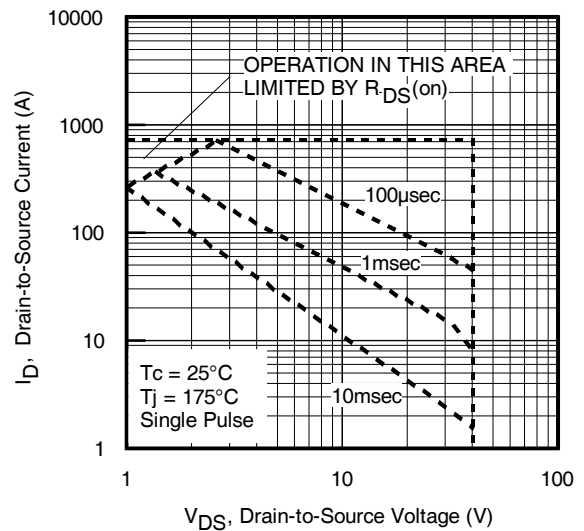
**Diode Characteristics**

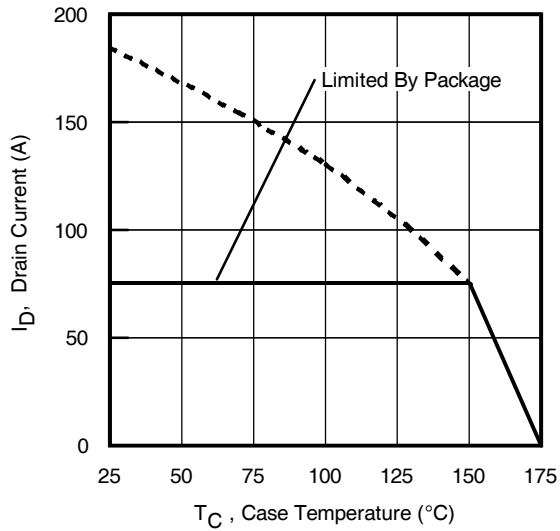
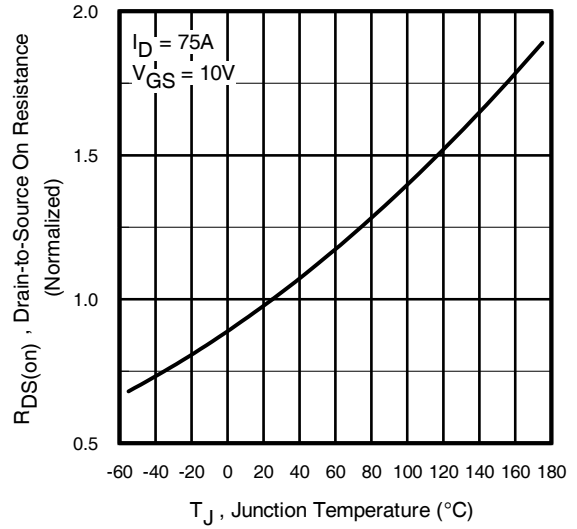
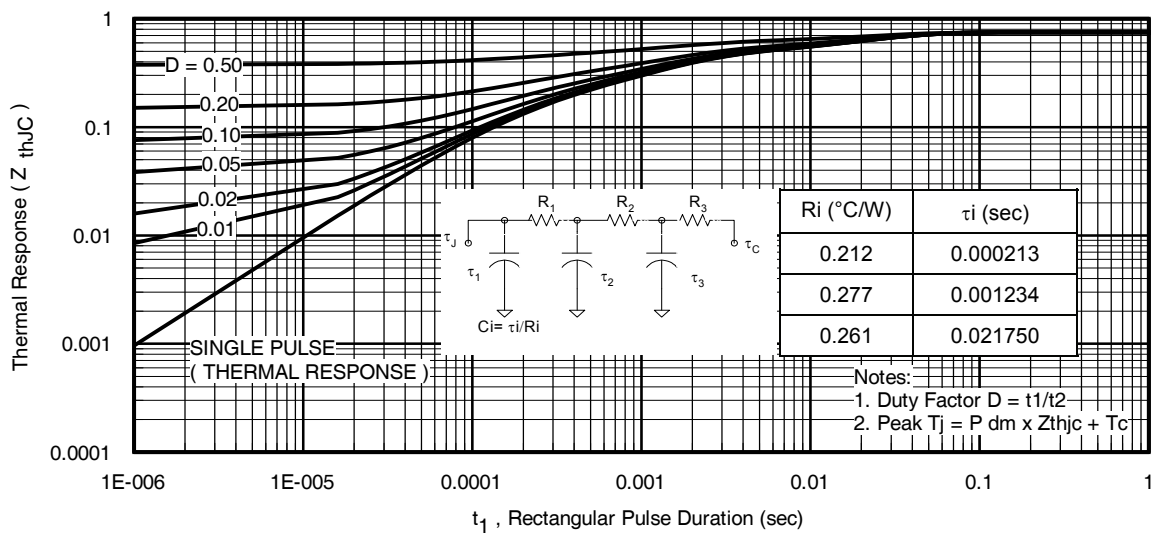
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	180	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	790		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A**, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	26	39	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 75A**, V <sub>DD</sub> = 20V
Q <sub>rr</sub>	Reverse Recovery Charge	—	18	27	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

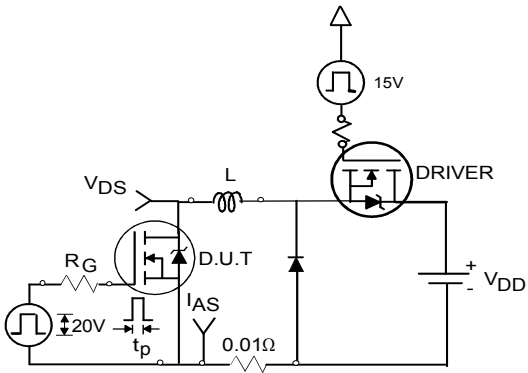
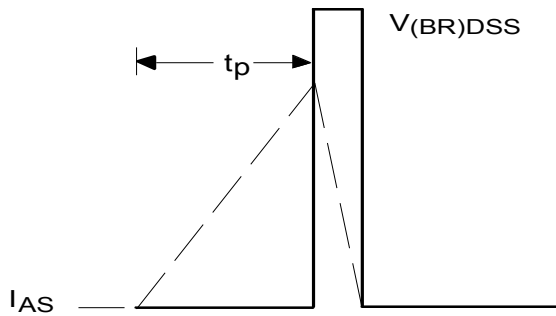
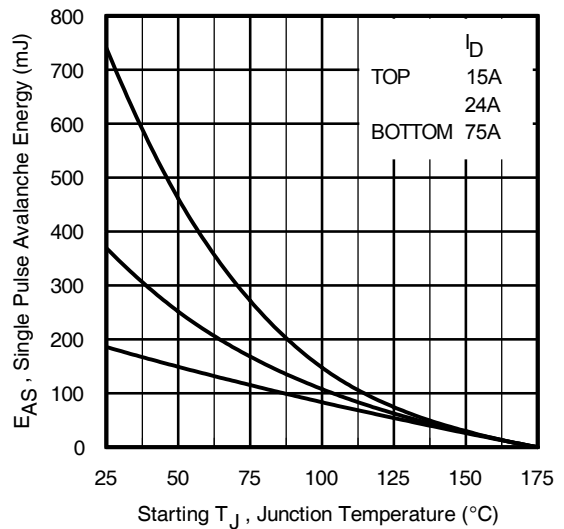
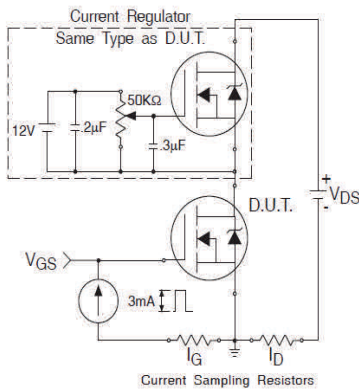
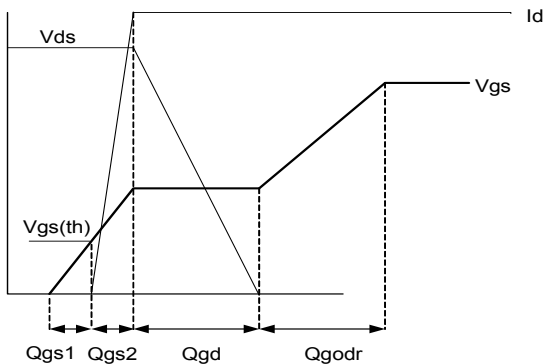
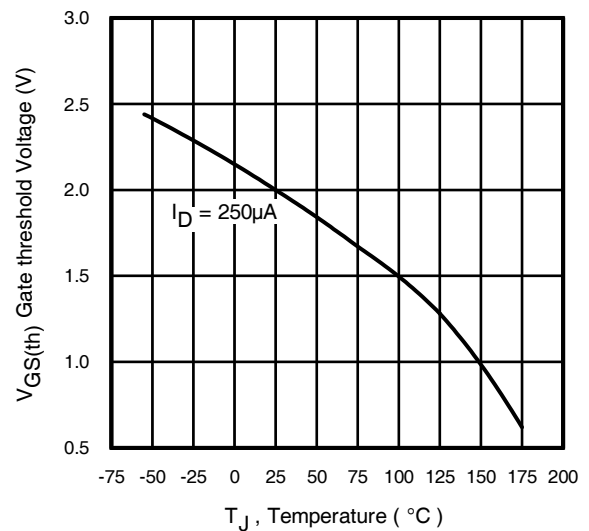
**Notes:**

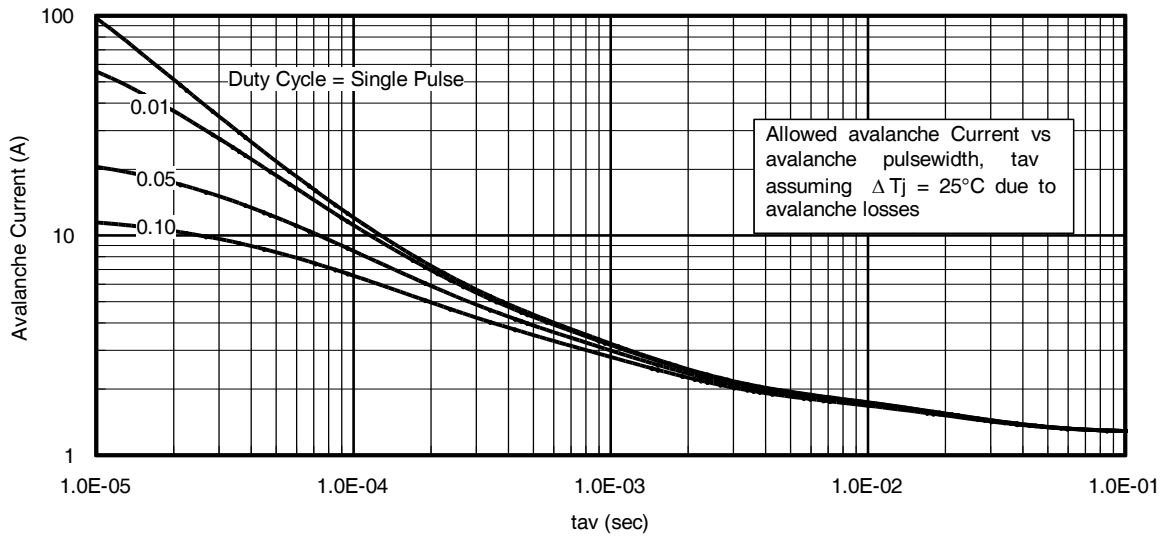
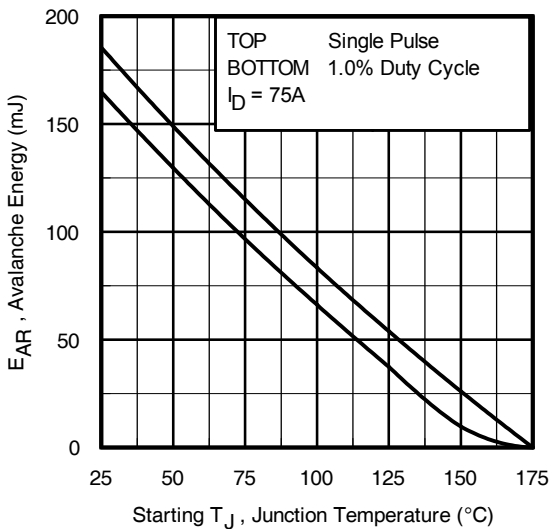
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig.11)
  - ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.066mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 75A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
  - ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
  - ④ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
  - ⑤ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
  - ⑥ This value determined from sample failure population 100% tested to this value in production.
  - ⑦ This is only applied to TO-220AB package.
  - ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
  - ⑨ TO-220Pak device will have an R<sub>th</sub> value of 0.65°C/W.
  - ⑩ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 160A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- \*\* All AC and DC test conditions based on former package limited current of 75A.


**Fig. 1 Typical Output Characteristics**

**Fig. 2 Typical Output Characteristics**

**Fig. 3 Typical Transfer Characteristics**

**Fig. 4 Typical Forward Transconductance vs. Drain Current**


**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area


**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Normalized On-Resistance vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 12c. Maximum Avalanche Energy vs. Drain Current**

**Fig 13a. Gate Charge Test Circuit**

**Fig 13b. Gate Charge Waveform**

**Fig 14. Threshold Voltage vs. Temperature**


**Fig 15. Avalanche Current vs. Pulse width**

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
**(For further info, see AN-1005 at www.infineon.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

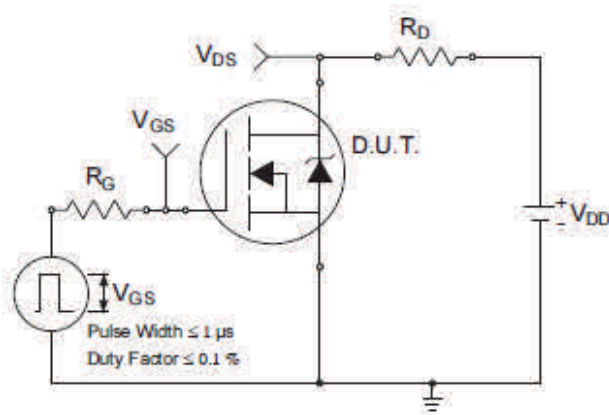
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

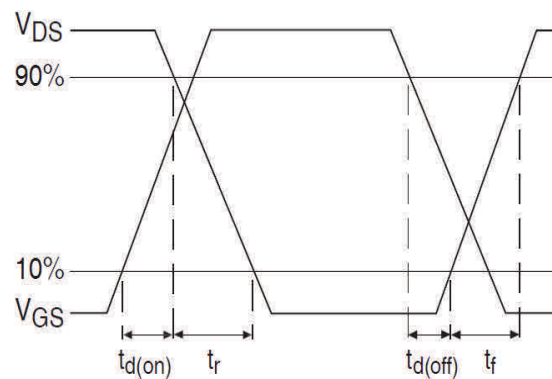
**Fig 16. Maximum Avalanche Energy vs. Temperature**



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms



**TO-220AB Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
phi P	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

**LEAD ASSIGNMENTS**
**HEXFET**

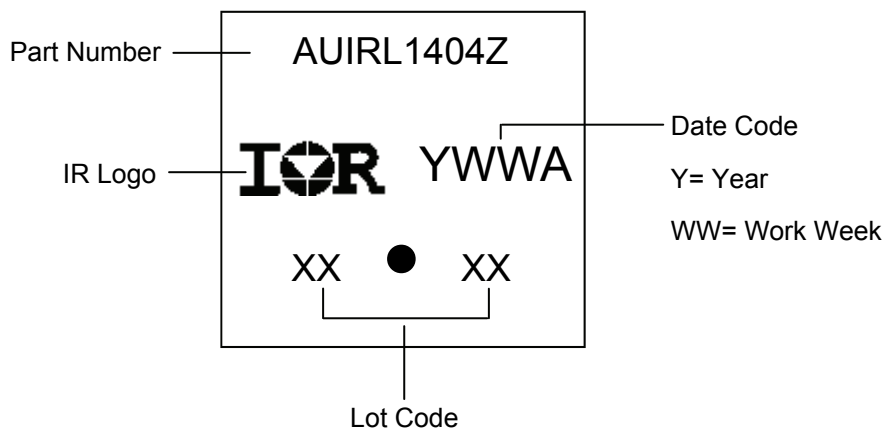
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

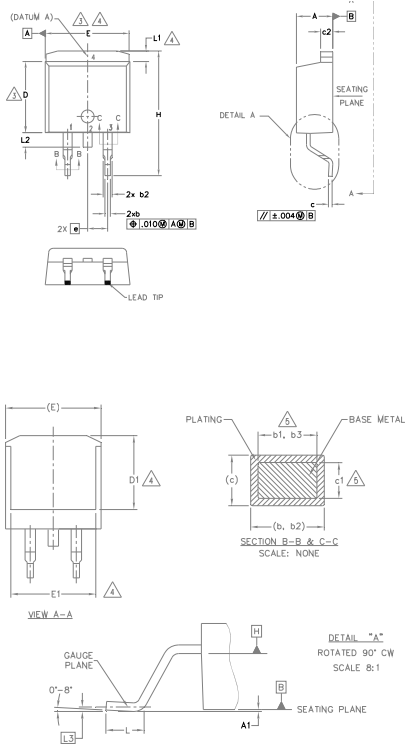
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

**DIODES**

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

**TO-220AB Part Marking Information**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))**


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
  6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  7. CONTROLLING DIMENSION: INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

**LEAD ASSIGNMENTS**
**DIODES**

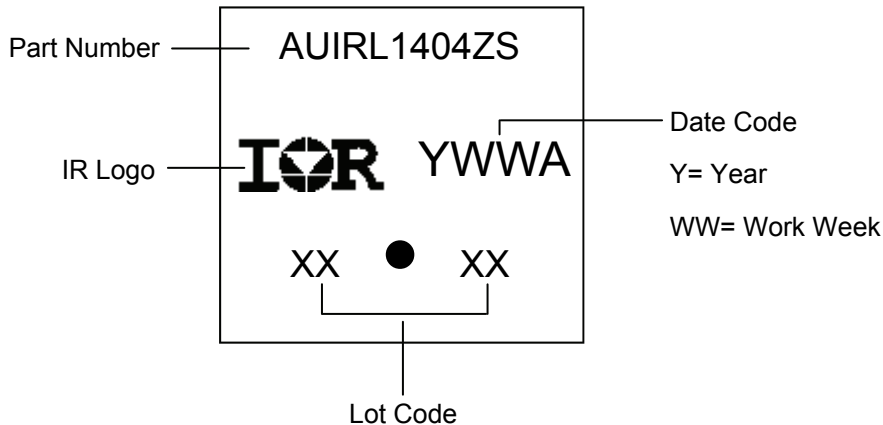
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- 2.- CATHODE
- 3.- ANODE

**HEXFET**

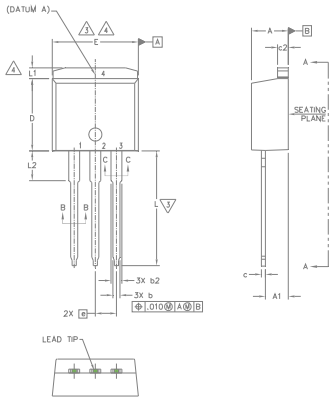
- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

**D<sup>2</sup>Pak (TO-263AB) Part Marking Information**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**TO-262 Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

**LEAD ASSIGNMENTS**
**IGBTs, CoPACK**

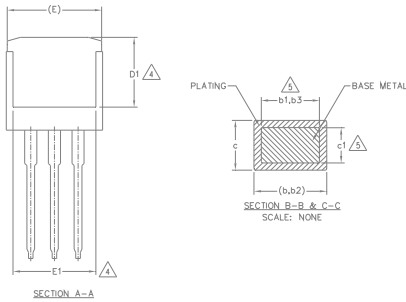
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**HEXFET**

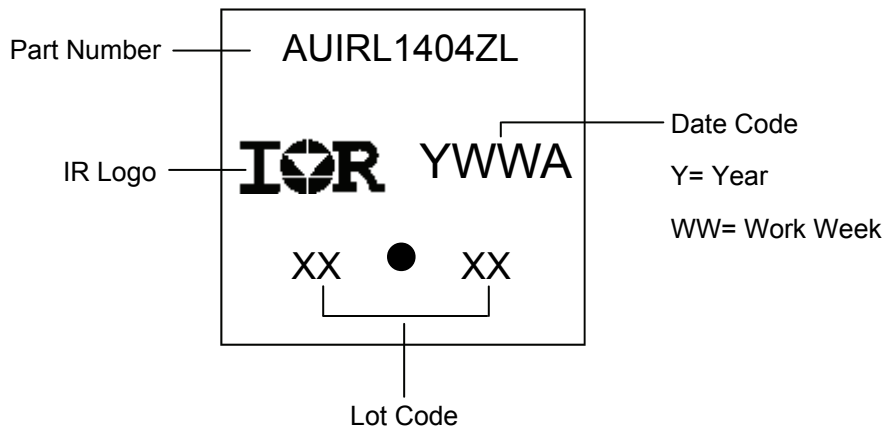
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**DIODES**

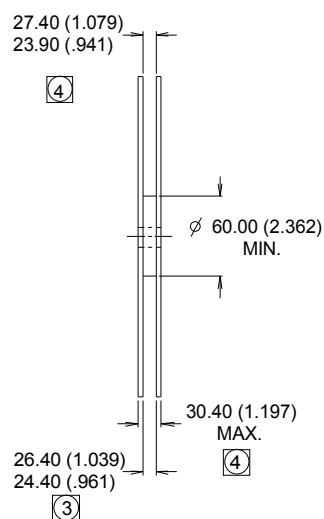
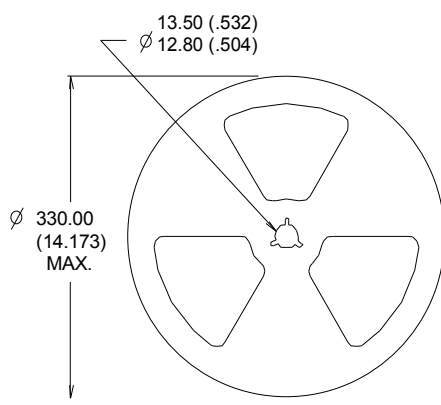
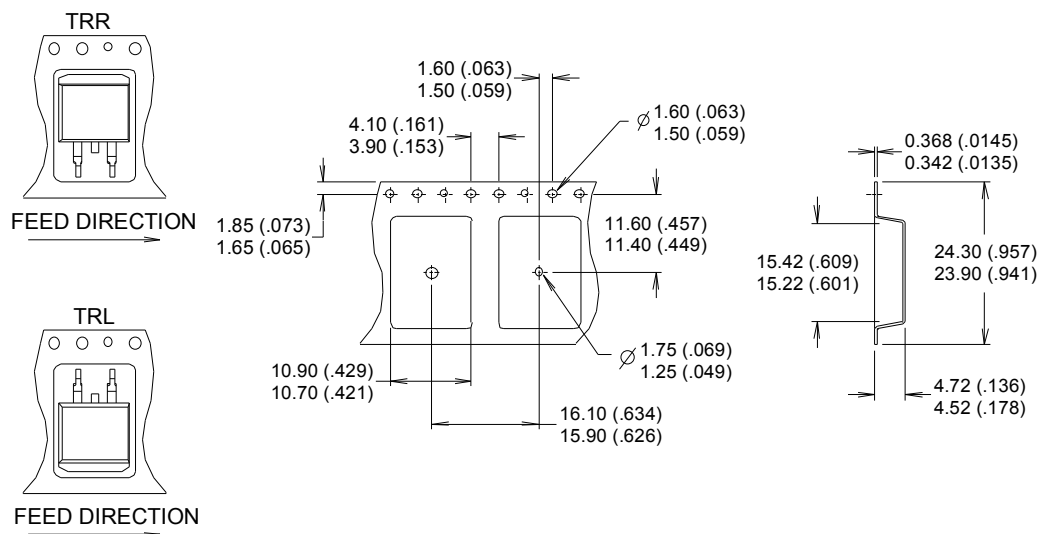
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

**TO-262 Part Marking Information**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))


- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		TO-220 Pak	N/A
		D <sup>2</sup> -Pak	MSL1
		TO-262	
<b>ESD</b>	Machine Model	Class M4 (+/- 425V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

**Revision History**

Date	Comments
10/27/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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