GENERAL DESCRIPTION

The XRP7725 is a quad channel Digital Pulse Width Modulated (DPWM) Step down (buck) controller. A wide 4.75V to 5.5V and 5.5V to 25V input voltage dual range allows for single supply operation from standard power rails.

With integrated FET gate drivers, two LDOs for standby power and a 105kHz to 1.23MHz independent channel to channel programmable constant operating frequency, the XRP7725 reduces overall component count and solution footprint and optimizes conversion efficiencies. A selectable digital Pulse Frequency Mode (DPFM) and low operating current result in better than 80% efficiency down to 10mA load provides support for portable and Energy Star compliant applications. Each XRP7725 output channel is individually programmable down to a minimum 0.6V with a resolution of 2.5mV, and configurable for precise soft start and soft stop sequencing, including delay and ramp control.

The XRP7725 operation is fully controlled via an SMBus-compliant I^2C interface allowing for advanced local and/or remote reconfiguration, full performance monitoring and reporting as well as fault handling.

Built-in independent output over voltage, over temperature, over-current and under voltage lockout protections insure safe operation under abnormal operating conditions.

The XRP7725 is offered in a RoHS compliant, "green"/halogen free 44-pin TQFN package.

FEATURES

- **Quad Channel Step-down Controller**
  - Digital PWM 105kHz-1.23MHz Operation
  - Individual Channel Frequency Selection
  - Patented digital PFM with Ultrasonic mode
  - Patented Over Sampling Feedback
- **Instantaneous current monitoring – Intel® Node Manager Compatible**
- **4.75V to 25V Input Voltage**
  - 4.75V to 5.5V and 5.5V to 25V Input Ranges
  - 0.6V to 5.5V Output Voltage
- **SMBus Compliant - I^2C Interface**
  - Full Power Monitoring and Reporting
- **3 x 15V Capable PSIO + 2 x GPIOs**
- **Full Start/Stop Sequencing Support**
- **Built-in Thermal, Over-Current, UVLO and Output Over-Voltage Protections**
- **On Board 5V and 3.3V Standby LDOs**
- **On Board Non-volatile Memory**
- **Supported by PowerArchitect™ 5**

APPLICATIONS

- **Blade Servers**
- **Micro Servers**
- **Network Adapter Cards**
- **Base Stations**
- **Switches/Routers**
- **Broadcast Equipment**
- **Industrial Control Systems**
- **Automatic Test Equipment**

TYPICAL APPLICATION DIAGRAM

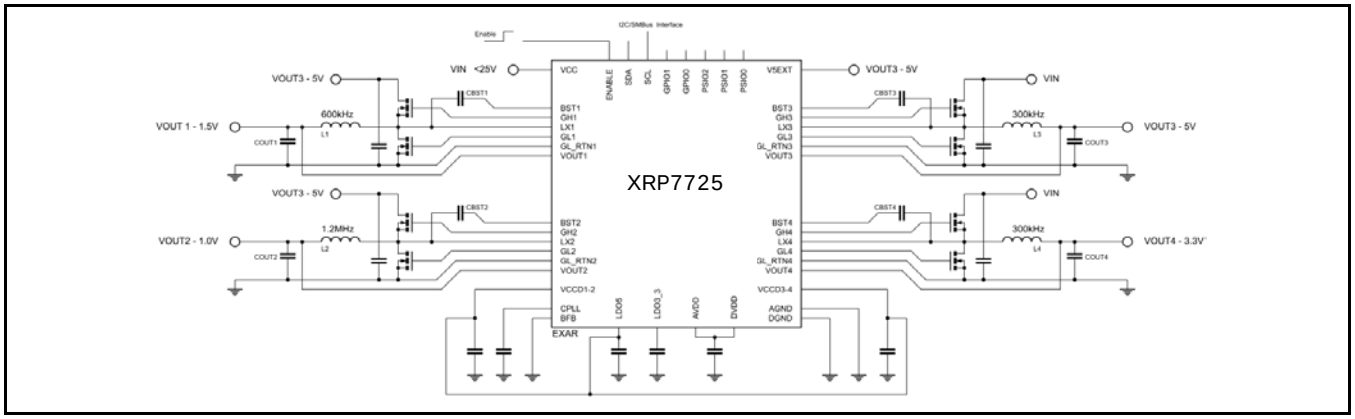


Figure 1: XRP7725 Application Diagram

FEATURES AND BENEFITS

Programmable Power Benefits

- **Fully Configurable**
  - Output set point
  - Feedback compensation
  - Frequency set point
  - Under voltage lock out
  - Input voltage measurement
  - Gate drive dead time
- **Reduced Development Time**
  - Configurable and re-configurable for different Vout, Iout, Cout, and Inductor values
  - No need to change external passives for a new output specification.
- **Higher integration and Reliability**
  - Many external components used in the past can be eliminated thereby significantly improving reliability.

PowerArchitect™ 5.1 Design and Configuration Software

- Wizard quickly generates a base design
- Calculates all configuration registers
- Projects can be saved and/or recalled
- GPIOs can be configured easily and intuitively
- Dashboard interface can be used for real-time monitoring and debug

System Benefits

- Intel Node Manager Compatible current monitoring.
- Ability to perform remote configuration updates.
- Ability to analyze operating history, perform diagnostics and if required, take the supply off-line after making other system adjustments.

System Integration Capabilities

- **Single supply operation**
- **I^2C interface allows:**
  - Intel Node Manager Compatible as well as other Power Management systems
  - Modification or reading of internal registers that control or monitor:
    - Output Current
    - Input and Output Voltage
    - Soft-Start/Soft-Stop Time
    - Power Good
    - Part Temperature
    - Enable/Disable Outputs
    - Over Current
    - Over Voltage
    - Temperature Faults
    - Adjusting fault limits and disabling/enabling faults
  - Packet Error Checking (PEC) on I^2C communication
- **5 GPIO pins with a wide range of configurability**
  - Fault reporting (including UVLO Warn/Fault, OCP Warn/Fault, OVP, Temperature, Soft-Start in progress, Power Good, System Reset)
  - Allows a Logic Level interface with other non-digital IC's or as logic inputs to other devices
- **Frequency and Synchronization Capability**
  - Selectable switching frequency between 105kHz and 1.2MHz
  - Main oscillator clock and DPWM clock can be synchronized to external sources
  - 'Master', 'Slave' and 'Stand-alone' configurations are possible
- **Internal MOSFET Drivers**
  - Internal FET drivers (4Ω/2Ω) per channel
  - Built-In Automatic Dead-time adjustment
  - 30ns Rise and Fall times
- **4 Independent SMPS channels and 2 LDOs in a 7x7mm TQFN**

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

VCCD, LDO5, LDO3_3, GLx, VOUTx ..... -0.3V to 7.0V
ENABLE, 5V_EXT ..... -0.3V to 7.0V
GPIO0/1, SCL, SDA 6.0V
PSIOs Inputs, BFB 18V
DVDD, AVDD 2.0V
V_{CC} 28V
LX# ..... -1V to 28V
BSTx, GHx ..... VLXx + 6V
Storage Temperature ..... -65°C to 150°C
Junction Temperature ..... 150°C
Power Dissipation ..... Internally Limited
Lead Temperature (Soldering, 10 sec) ..... 300°C
ESD Rating (HBM - Human Body Model) 2kV

OPERATING RATINGS

Input Voltage Range V_{CC} ..... 5.5V to 25V
Input Voltage Range V_{CC} = LDO5 ..... 4.75V to 5.5V
VOUT1, 2, 3, 4 ..... 5.5V
Junction Temperature Range ..... -40°C to 125°C
JEDEC Thermal Resistance θ_{JA} ..... 30.2°C/W

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{CC} = 5.5V to 25V, 5V EXT open.

QUIESCENT CURRENT

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{CC} Supply Current in SHUTDOWN		10	20	µA		EN = 0V, V_{CC} = 12V
ENABLE Turn On Threshold	0.82		0.95	V		V_{CC} = 12V Enable Rising
ENABLE Pin Leakage Current			10	uA		EN=5V
	-10			uA		EN=0V
V_{CC} Supply Current in STANDBY		440	600	µA		LDO3_3 disabled, all channels disabled GPIOs programmed as inputs V_{CC} =12V,EN = 5V
V_{CC} Supply Current 2ch PFM		3.1		mA		2 channels on and set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, V_{CC} =12 V, No I^2C activity.
V_{CC} Supply Current 4ch PFM		4.0		mA		4 channels on and set at 5V, VOUT forced to 5.1V, no load, non-switching, Ultra-sonic off, V_{CC} =12V, No I^2C activity.
V_{CC} Supply Current ON		18		mA		All channels enabled, Fsw=600kHz, gate drivers unloaded, No I^2C activity.

INPUT VOLTAGE RANGE AND UNDERVOLTAGE LOCKOUT

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{CC} Range	5.5		25	V	•	
	4.75		5.5	V	•	With V_{CC} connected to LDO5

VOLTAGE FEEDBACK ACCURACY AND OUTPUT VOLTAGE SET POINT RESOLUTION

Parameter	Min.	Typ.	Max.	Units		Conditions
VOUT Regulation Accuracy Low Output Range 0.6V to 1.6V PWM Operation	-5		5	mV		0.6 ≤ VOUT ≤ 1.6V
	-20		20	mV	•	
	-7.5		7.5	mV		0.6 ≤ VOUT ≤ 1.6V V_{CC} =LDO5
	-22.5		22.5	mV	•	
VOUT Regulation Accuracy Mid Output Range 0.6V to 3.2V PWM Operation	-15		15	mV		0.6 ≤ VOUT ≤ 3.2V
	-45		45	mV	•	
	-20		20	mV		0.6 ≤ VOUT ≤ 3.2V V_{CC} =LDO5
	-50		50	mV	•	
VOUT Regulation Accuracy High Output Range 0.6V to 5.5V PWM Operation	-30		30	mV		0.6 ≤ VOUT ≤ 5.5V
	-90		90	mV	•	
	-40		40	mV		0.6 ≤ VOUT ≤ 4.2V V_{CC} =LDO5
	-100		100	mV	•	
VOUT Regulation Range	0.6		5.5	V	•	Without external divider network
VOUT Native Set Point Resolution		12.5 25 50		mV		Low Range Mid Range High Range
VOUT Fine Set Point Resolution[1]		2.5 5 10		mV		Low Range Mid Range High Range
VOUT Input Resistance		120 90 75		kΩ		Low Range Mid Range High Range
VOUT Input Resistance in PFM Operation		10 1 0.67		MΩ		Low Range Mid Range High Range
Power Good and OVP Set Point Range (from set point)	-155 -310 -620		157.5 315 630	mV		Low Range Mid Range High Range
Power Good and OVP Set Point Accuracy	-5 -10 -20		5 10 20	mV		Low Range Mid Range High Range
BFB Set Point Range	9		16	V		
BFB Set Point Resolution		1		V		
BFB Accuracy	-0.5		0.5	V		

Note 1: Fine Set Point Resolution not available in PFM

CURRENT AND AUX ADC (MONITORING ADCS)

Parameter	Min.	Typ.	Max.	Units		Conditions
Current Sense Accuracy	-3.75	±1.25	3.75	mV		Low Range (≤120mV) -60mV applied
	-10		10	mV	•	
	-5	±2.5	5	mV		High Range (≤280mV) -150mV
	-12.5		+12.5	mV	•	
Current Sense ADC INL		±0.4		LSB		
DNL		0.27				
Current Limit Set Point Resolution and Current Sense ADC Resolution		1.25		mV		Low Range (≤120mV)
		2.5		mV		High Range (≤280mV)
Current Sense ADC Range	-120		20	mV		Low Range (≤120mV)
	-280		40			High Range (≤280mV)
VOUT ADC Resolution		15 30 60		mV		Low Range Mid Range High Range
VOUT ADC Accuracy	-1		1	LSB		
V_{CC} ADC Range	4.6		25	V		Note 2
UVLO WARN SET	4.4		4.72	V		UVLO WARN set point 4.6V, V_{CC} =LDO5
UVLO WARN CLEAR	4.4		4.72	V		UVLO WARN set point 4.6V, V_{CC} =LDO5
UVLO FAULT SET (Note 3)	4.2		4.55	V		UVLO FAULT set point 4.4V, V_{CC} =LDO5
V_{CC} ADC Resolution		200		mV		
V_{CC} ADC Accuracy	-1		1	LSB		Vin <= 20V
Die Temp ADC Resolution		5		°C		
Die Temp ADC Range	-44		156	°C		Output value is in Kelvin

Note 2: Although Range of V_{CC} ADC is 0V to 25V, operation below 4.55 is not supported.
Note 3: This test ensures an UVLO FAULT flag will be given before the LDO5 hardware UVLO trips.

LINEAR REGULATORS

Parameter	Min.	Typ.	Max.	Units		Conditions
LDO5 Output Voltage	4.85	5.0	5.15	V	•	5.5V ≤ V_{CC} ≤ 25V 0mA < $I_{LDO5OUT}$ < 130mA, LDO3_3 Off
LDO5 Current Limit	135	155	180	mA	•	LDO5 Fault Set
LDO5 UVLO	4.74			V	•	V_{CC} Rising
LDO5 PGOOD Hysteresis		375		mV		V_{CC} Falling
LDO5 Bypass Switch Resistance		1.1	1.5	Ω		
Bypass Switch Activation Threshold	2.5		2.5	%	•	V5EXT Rising, % of threshold setting
Bypass Switch Activation Hysteresis		150		mV		V5EXT Falling
LDO3_3 Output Voltage	3.15	3.3	3.45	V	•	4.6V ≤ LDO5 ≤ 5.5V 0mA < I_{LDO3_3OUT} < 50mA
LDO3_3 Current Limit	53		85	mA	•	LDO3_3 Fault Set
Maximum total LDO loading during ENABLE start-up			30	mA		ENABLE transition from logic low to high. Once LDO5 in regulation above limits apply.

PWM GENERATORS AND OSCILLATOR

Parameter	Min.	Typ.	Max.	Units		Conditions
Switching Frequency (fsw) Range	105		1230	kHz		Steps defined in Table 1
fsw Accuracy	–5		5	%		
CLOCK IN Synchronization Frequency	20	25.7	31	MHz		When synchronizing to an external clock (Range 1)
CLOCK IN Synchronization Frequency	10	12.8	15.5	MHz		When synchronizing to an external clock (Range 2)

GPIOs[4]

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V		
Input Pin High Level	2.0			V		
Input Pin Leakage Current			1	µA		
Output Pin Low Level			0.4	V		I_{SINK} = 1mA
Output Pin High Level	2.4			V		I_{SOURCE} = 1mA
Output Pin High Level		3.3	3.6	V		I_{SOURCE} = 0mA
Output Pin High-Z leakage Current (GPIO pins only)			10	µA		
Maximum Sink Current			1	mA		Open Drain Mode
I/O Frequency			30	MHz		

Note 4: 3.3V CMOS logic compatible, 5V tolerant.

PSIOs[5]

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level			0.8	V		
Input Pin High Level	2.0			V		
Input Pin Leakage Current			1	µA		
Output Pin Low Level			0.4	V		I_{SINK} = 3mA
Output Pin High Level			15	V		Open Drain. External pull-up resistor to user supply
Output Pin High-Z leakage Current (PSIO pins only)			10	µA		
I/O Frequency			5	MHz		

Note 5: 3.3V/5.0V CMOS logic compatible, maximum rating of 15.0V

SMBUS (I2C) INTERFACE

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Pin Low Level, V_{IL}			0.3 VIO	V		VIO = 3.3 V ±10%
Input Pin High Level, V_{IH}	0.7 VIO			V		VIO = 3.3 V±10%
Hysteresis of Schmitt Trigger inputs, V_{hys}	0.05 VIO			V		VIO = 3.3 V±10%
Output Pin Low Level (open drain or collector), V_{OL}			0.4	V		I_{SINK} = 3mA
Input leakage current	-10		10	µA		Input is between 0.1 VIO and 0.9 VIO
Output fall time from V_{IHmin} to V_{ILmax}	20 + 0.1 Cb		250	Ns		With a bus capacitance (Cb) from 10 pF to 400 pF
Internal Pin Capacitance			1	pF		

GATE DRIVERS

Parameter	Min.	Typ.	Max.	Units		Conditions
GH, GL Rise Time		17		Ns		At 10-90% of full scale, 1nF C_{load}
GH, GL Fall Time		11		Ns		
GH, GL Pull-Up On-State Output Resistance		4	5	Ω		
GH, GL Pull-Down On-State Output Resistance		2	2.5	Ω		
GH, GL Pull-Down Resistance in Off-Mode		50		kΩ		V_{CC} = VCCD = 0V.
Bootstrap diode forward resistance		9		Ω		@ 10mA
Minimum On Time		50		ns		1nF of gate capacitance.
Minimum Off Time		125		ns		1nF of gate capacitance
Minimum Programmable Dead Time		20		ns		Does not include dead time variation from driver output stage Tsw=switching period
Maximum Programmable Dead Time		Tsw		us		
Programmable Dead Time Adjustment Step		607		ps		

BLOCK DIAGRAM

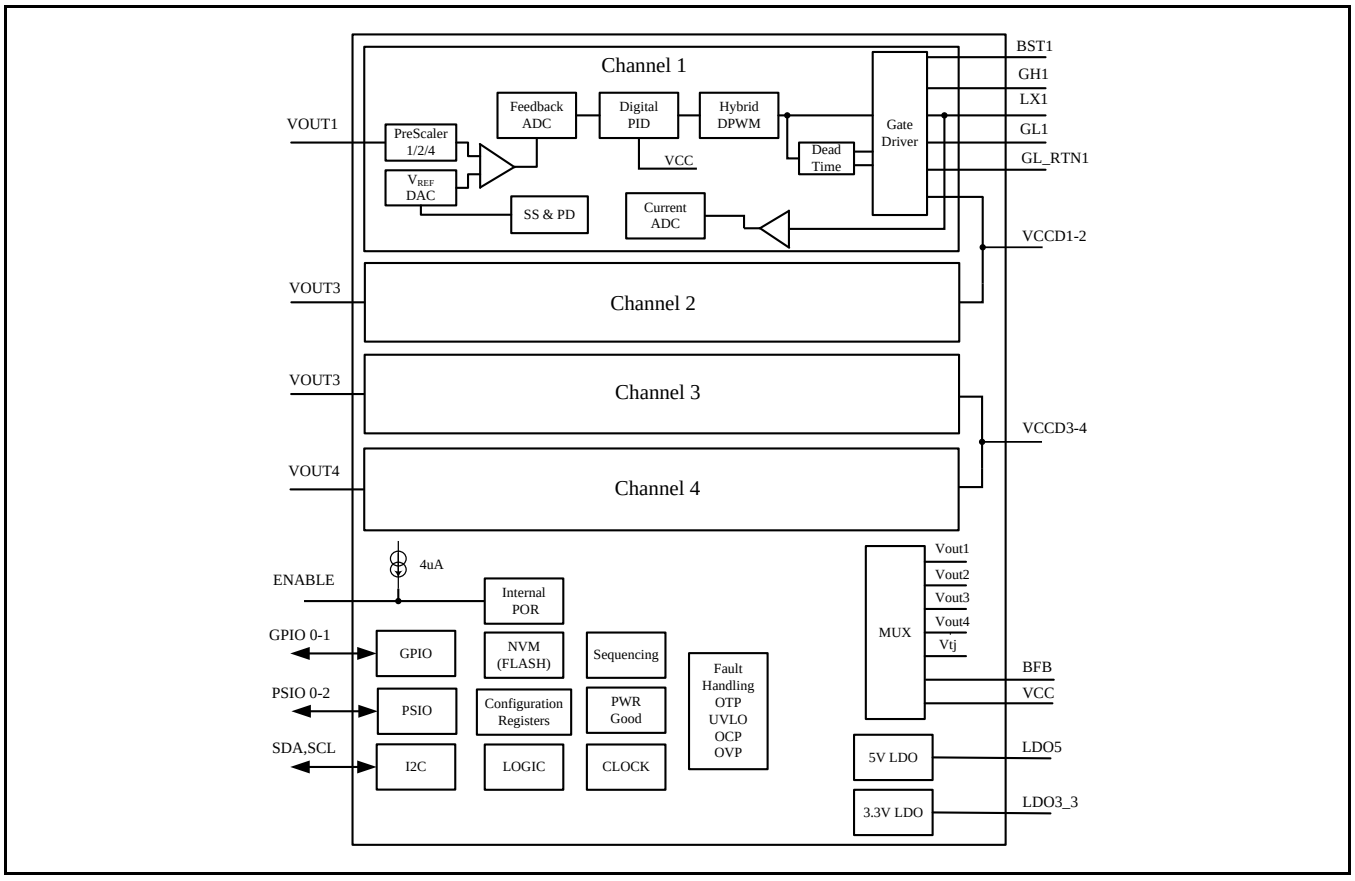


Figure 2: XRP7725 Block Diagram

LDO BLOCK DIAGRAM

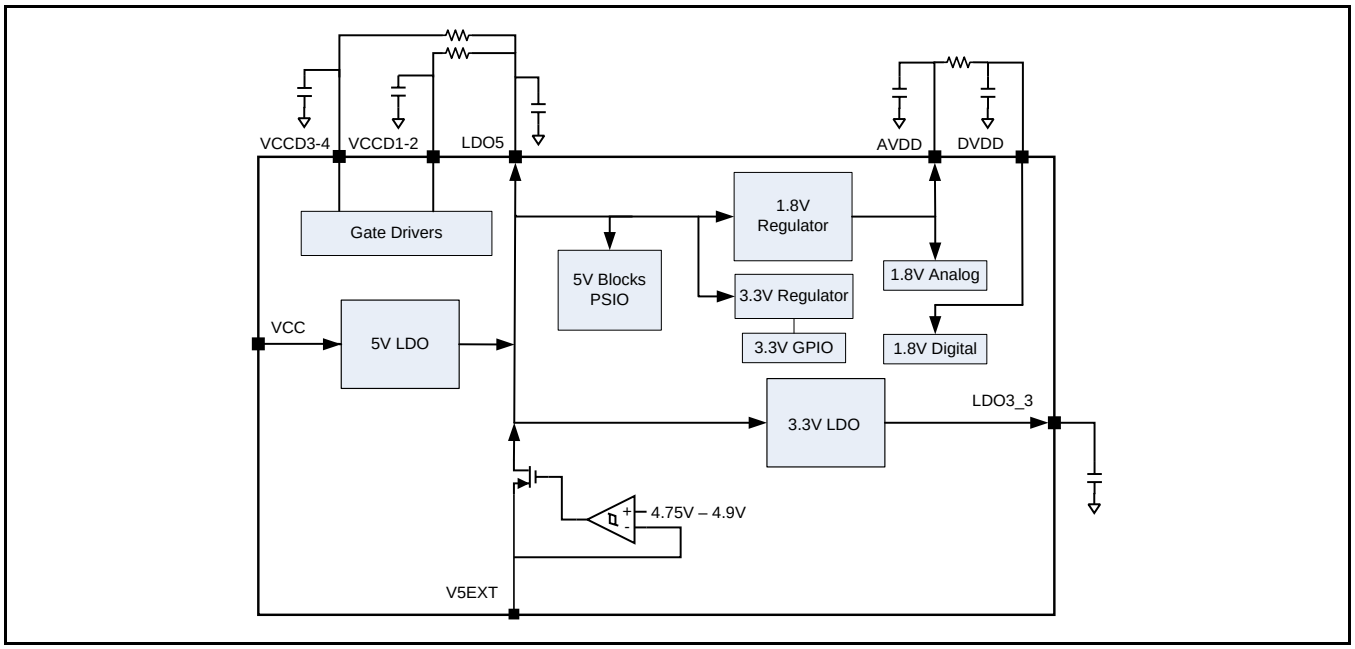


Figure 3: XRP7725 LDO Block Diagram

PIN ASSIGNMENT

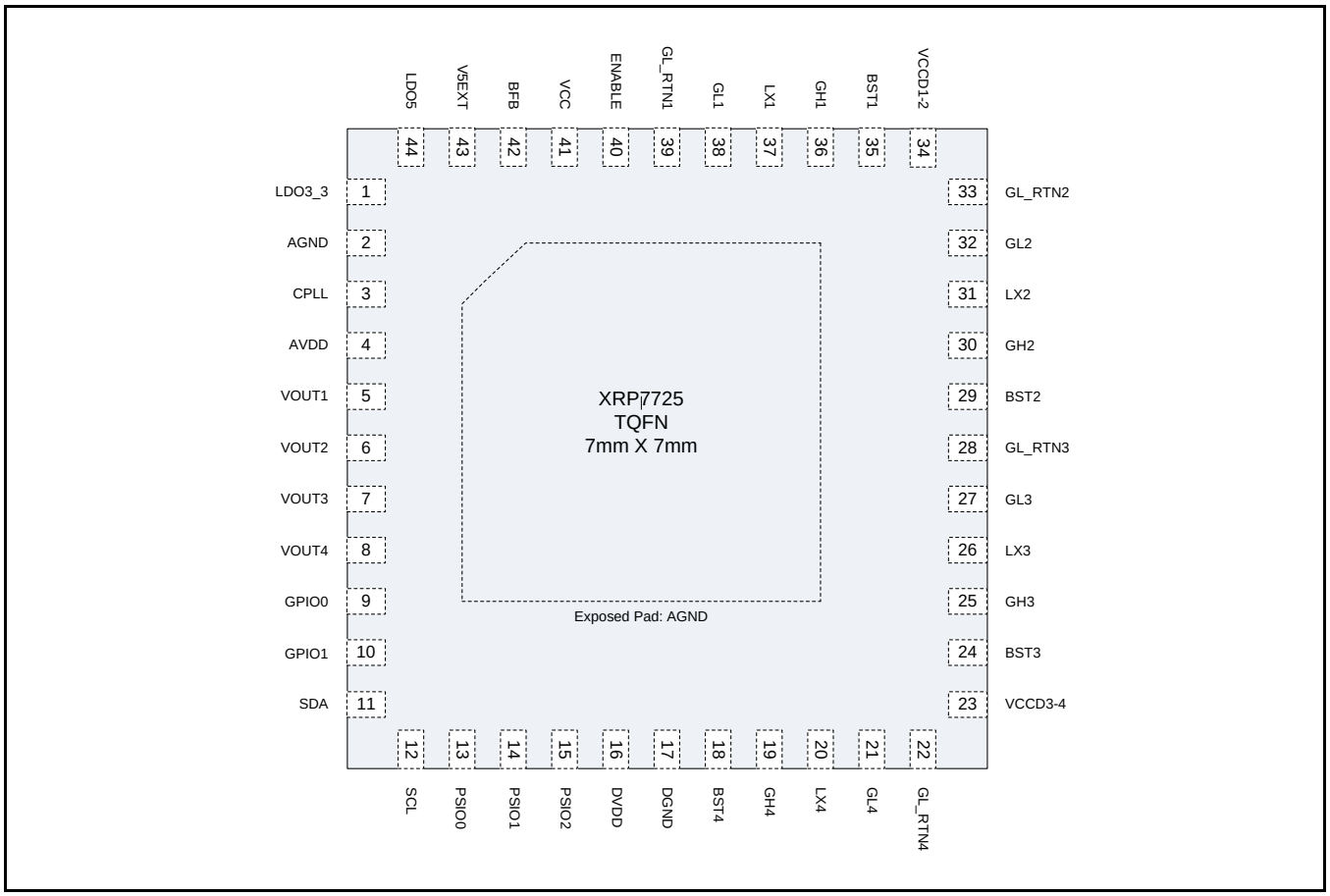


Figure 4: XRP7725 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
V_{CC}	41	Input voltage. Place a decoupling capacitor close to the pin. This input is used in UVLO fault generation.
DVDD	16	1.8V supply input for digital circuitry. Connect pin to AVDD. Place a decoupling capacitor close to the pin.
VCCD1-2 VCCD3-4	23,34	Gate Drive supply. Two independent gate drive supply pins where pin 34 supplies drivers 1 and 2 and pin 23 supplies drivers 3 & 5. One of the two pins must be connected to the LDO5 pin to enable two power rails initially. It is recommended that the other VCCD pin be connected to the output of a 5V switching rail (for improved efficiency or for driving larger external FETs), if available, otherwise this pin may also be connected to the LDO5 pin. A bypass capacitor (>1uF) to PAD is recommended for each VCCD pin with the pin(s) connected to LDO5 with shortest possible etch.
AGND	2	Analog ground pin. This is the small signal ground connection.
GL_RTN1-4	39,33, 28,22	Ground connection for the low side gate driver. This should be routed as a signal trace with GL. Connect to the source of the low side MOSFET.
GL1-GL4	38,32, 27,21	Output pin of the low side gate driver. Connect directly to the gate of an external N-channel MOSFET.
GH1-GH4	36,30, 25,19	Output pin of the high side gate driver. Connect directly to the gate of an external N-channel MOSFET.

Name	Pin Number	Description
LX1-LX4	37,31, 26,20	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFETs and the inductor. These pins are also used to measure voltage drop across bottom MOSFETs in order to provide output current information to the control engine.
BST1-BST4	35,29, 24,18	High side driver supply pin(s). Connect BST to the external capacitor as shown in the Typical Application Circuit on page 2. The high side driver is connected between the BST pin and LX pin and delivers the BST pin voltage to the high side FET gate each cycle.
GPI0-GPIO1	9,10	These pins can be configured as inputs or outputs to implement custom flags, power good signals, enable/disable controls and synchronization to an external clock.
PSIO0-PSIO2	13,14,15	Open drain, these pins can be used to control external power MOSFETs to switch loads on and off, shedding the load for fine grained power management. They can also be configures as standard logic outputs or inputs just as any of the GPIOs can be configured, but as open drains require an external pull-up when configured as outputs.
SDA, SCL	11,12	SMBus/I^2C serial interface communication pins.
VOUT1-VOUT4	5,6,7,8	Connect to the output of the corresponding power stage. The output is sampled at least once every switching cycle.
LDO5	44	Output of a 5V LDO. This is a micro power LDO that can remain active while the rest of the IC is in the stand-by mode. This LDO is also used to power the internal Analog Blocks.
LDO3_3	1	Output of the 3.3V standby LDO. This is a micro power LDO that can remain active while the rest of the IC is in shutdown.
ENABLE	40	If ENABLE is pulled high or allowed to float high, the chip is powered up (logic is reset, registers configuration loaded, etc.). The pin must be held low for the XRP7725 to be placed into shutdown.
BFB	42	Input from the 15V output created by the external boost supply. When this pin goes below a pre-defined threshold, a pulse is created on the low side drive to charge this output back to the original level. If not used, this pin should be connected to GND.
DGND	17	Digital ground pin. This is the logic ground connection, and should be connected to the ground plane close to the PAD.
CPLL	3	Connect to a 2.2nF capacitor to GND.
V5EXT	43	External 5V that can be provided. If one of the output channels is configured for 5V, then this voltage can be fed back to this pin for reduced operating current of the chip and improved efficiency.
AVDD	4	Output of the internal 1.8V LDO. A decoupling capacitor should be placed between AVDD and AGND close to the chip.
PAD	45	This is the die attach paddle, which is exposed on the bottom of the part. Connect externally to the ground plane.

ORDERING INFORMATION(1)

Part Number	Operating Temperature Range	Lead-Free	Package	Packing Method	I^2C Default Address
XRP7725ILB-F	-40°C ≤ T_J ≤ +125°C	Yes(2)	44-pin TQFN	Tray	0x28 (7Bit)
XRP7725EVB-DEMO-2-KITA	Evaluation kit includes XRP7725EVB-DEMO-1 Evaluation Board with Power Architect software and XRP77XXEVB-XCM (USB to I^2C MaxLinear Configuration Module)				
XRP7725EVB-DEMO-2	XRP7725 Evaluation Board				

Notes:

1. Refer to www.exar.com/XRP7725 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{CC} = 12V, T_J = T_A = 25°C, unless otherwise specified - Schematic and BOM from XRP7725EVB. See XRP7725EVB-DEMO-1 Manual.

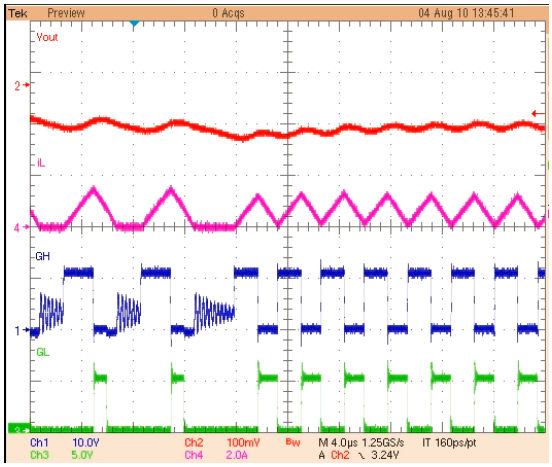


Figure 5: PFM to PWM Transition

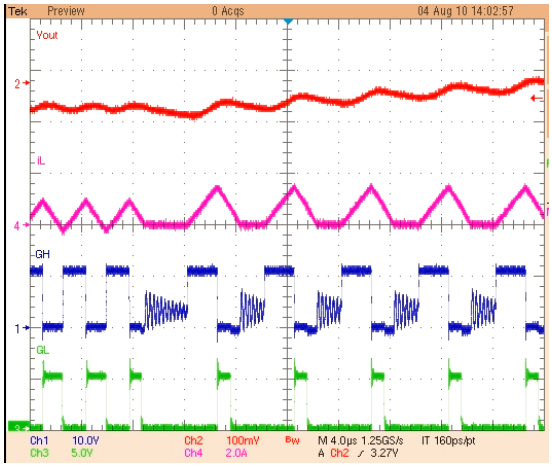


Figure 6: PWM to PFM Transition

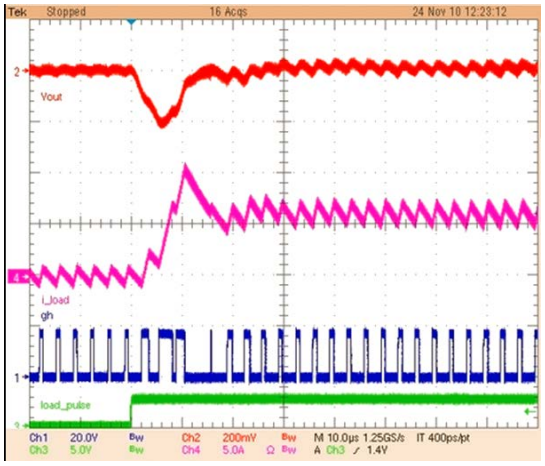


Figure 7: 0-6A Transient 300kHz PWM only

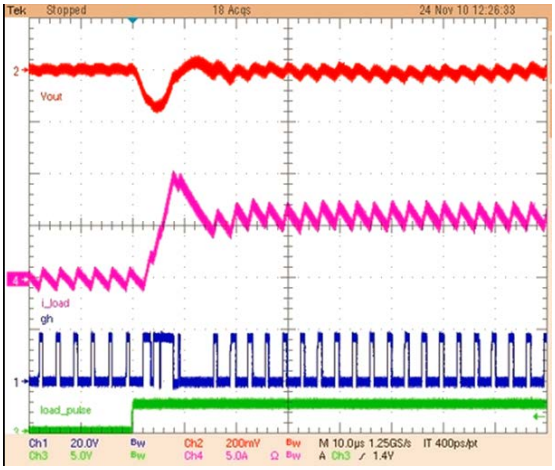


Figure 8: 0-6A Transient 300kHz with OVS ±5.5%

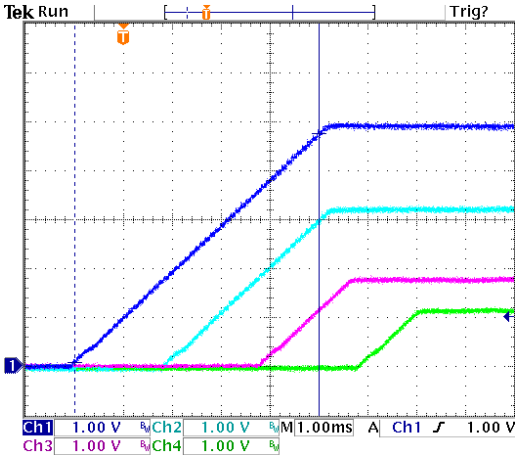


Figure 9: Sequential Start-up

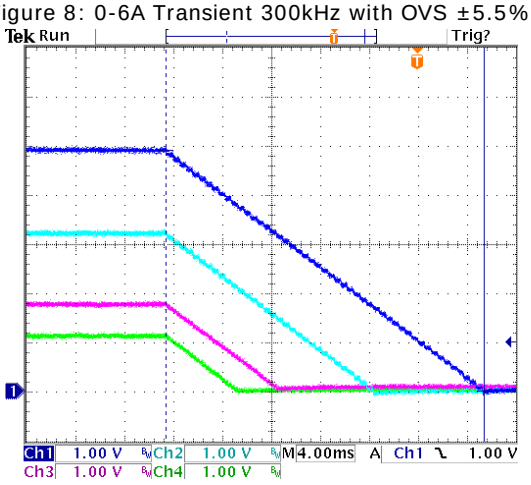


Figure 10: Sequential Shut Down

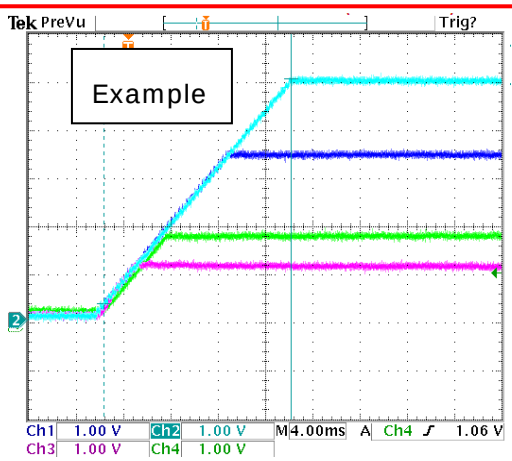


Figure 11: Simultaneous Start-up

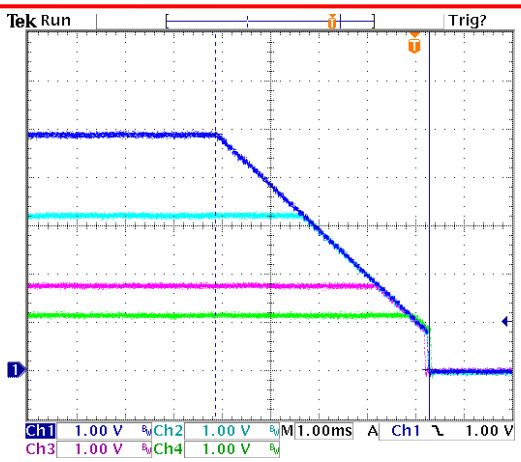


Figure 12: Simultaneous Shut Down

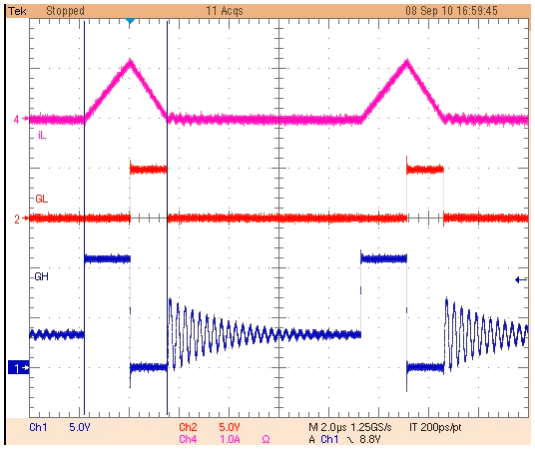


Figure 13: PFM Zero Current Accuracy

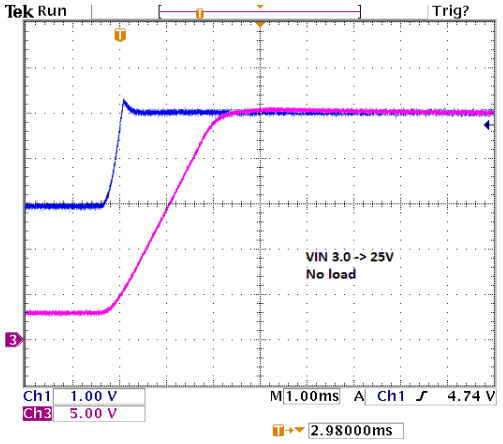


Figure 14: LDO5 Brown Out Recovery, No Load

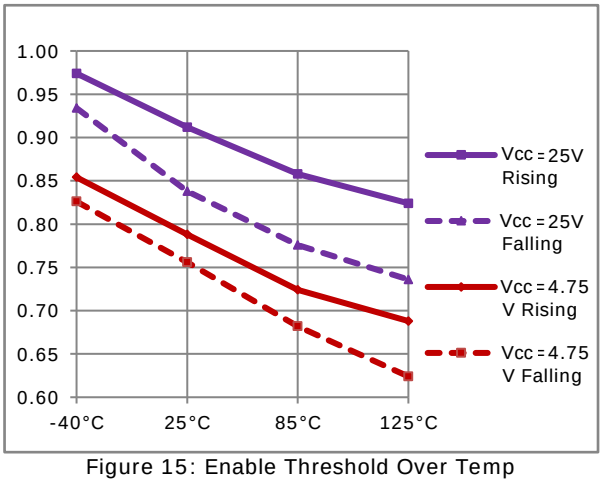


Figure 15: Enable Threshold Over Temp

FUNCTIONAL OVERVIEW

The XRP7725 is a quad-output digital pulse width modulation (DPWM) controller with integrated gate drivers for use with synchronous buck switching regulators. Each output voltage can be programmed from 0.6V to 5.5V without the need for an external voltage divider. The wide range of programmable DPWM switching frequency (from 105 kHz to 1.2 MHz) enables the user to optimize for efficiency or component sizes. Since the digital regulation loop requires no external passive components, loop performance is not compromised due to external component variation or operating condition.

The XRP7725 provides a number of critical safety features, such as Over-Current Protection (OCP), Over-Voltage Protection (OVP), Over Temperature Protection (OTP) plus input Under Voltage Lockout (UVLO). In addition, a number of key health monitoring features such as warning level flags for the safety functions, Power Goods (PGOOD), etc., plus full monitoring of system voltages and currents. The above are all programmable and/or readable from the SMBus and many are steerable to the GPIOs for hardware monitoring.

For hardware communication, the XRP7725 has two logic level General Purpose Input-Output (GPIO) pins and three, 15V, open drain, Power System Input-Output (PSIO) pins. Two pins are dedicated to the SMBus data (SDA) and clock (SCL). Additional pins include Chip Enable (Enable), Aux Boost Feedback (BFB) and External PLL Capacitor (CPLL).

In addition to providing four switching outputs, the XRP7725 also provides control for an Aux boost supply, and two stand-by linear regulators that produce 5V and 3.3V for a total of seven customer usable supplies in a single device.

The 5V LDO is used for internal power and is also available for customer use to power external circuitry. The 3.3V LDO is solely for customer use and is not used by the chip. There is also a 1.8V linear regulator which is for internal use only and should not be used externally.

A key feature of the XRP7725 is its advinced power management capabilities. All four outputs are independently programmable and provide the user full control of the delay, ramp, and sequence during power up and power down. The user may also control how the outputs interact and power down in the event of a fault. This includes active ramp down of the output voltages to remove an output voltage as quickly as possible. Another useful feature is that the outputs can be defined and controlled as groups.

The XRP7725 has two main types of programmable memory. The first type is runtime registers that contain configuration, control and monitoring information for the chip. The second type is rewritable Non-Volatile Flash Memory (NVFM) that is used for permanent storage of the configuration data along with various chip internal functions. During power up, the run time registers are loaded from the NVFM allowing for standalone operation.

The XRP7725 brings an extremely high level of functionality and performance to a programmable power system. Ever decreasing product budgets require the designer to quickly make good cost/performance tradeoffs to be truly successful. By incorporating four switching channels, two user LDOs, a charge pump boost controller, along with internal gate drivers, all in a single package, the XRP7725 allows for extremely cost effective power system designs. Another key cost factor that is often overlooked is the unanticipated Engineering Change Order (ECO). The programmable versatility of the XRP7725, along with the lack of hard wired configuration components, allows for minor and major changes to be made in circuit by simple reprogramming.

THEORY OF OPERATION

CHIP ARCHITECTURE

REGULATION LOOPS

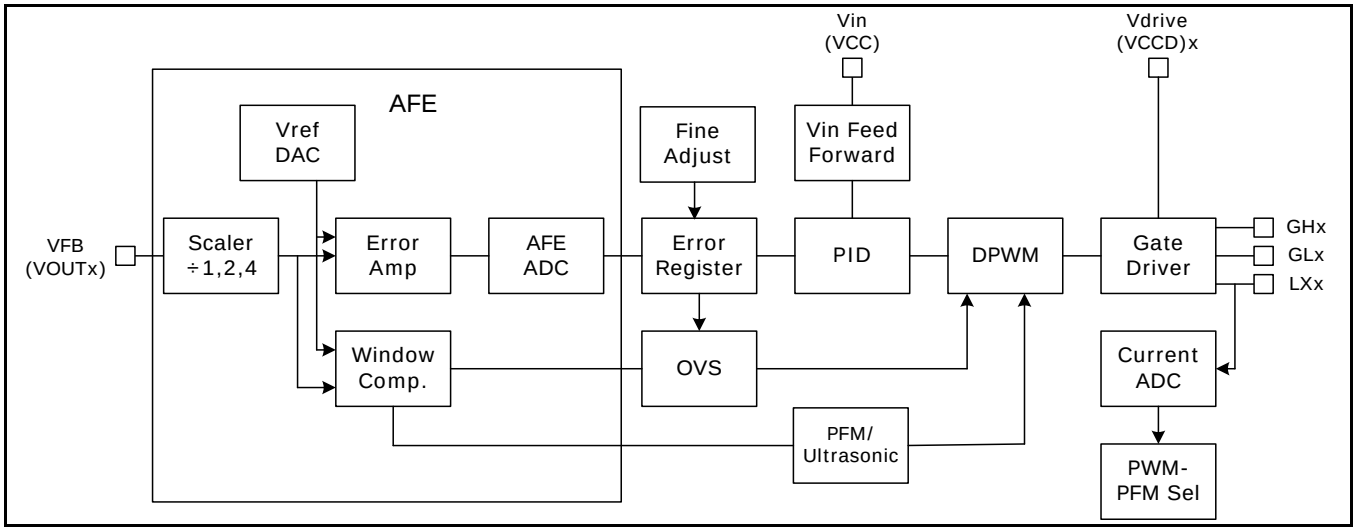


Figure 16: XRP7725 Regulation Loops

Figure 16 shows a simplified functional block diagram of the regulation loops for one output channel of the XRP7725. There are four separate parallel control loops; Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), Ultrasonic, and Over Sampling (OVS). Each of these loops is fed by the Analog Front End (AFE) as shown at the left of the diagram. The AFE consist of an input voltage scaler, a programmable Voltage Reference (Vref) DAC, Error Amplifier, and a window comparator. Some of the functional blocks are common and shared by each channel by means of a multiplexer.

PWM Loop

The PWM loop operates in Voltage Control Mode (VCM) with optional V_{IN} feed forward based on the voltage at the V_{CC} pin. The reference voltage (Vref) for the error amp is generated by a 0.15V to 1.6V DAC that has 12.5mV resolution. In order to provide a 0.6V to 5.5V output voltage range, an input scaler is used to reduce feedback voltages for higher output voltages to bring them within the 0.15V to 1.6V control range. So for output voltages up to 1.6V (low range) the scaler has a gain of 1. For output voltages from 1.6V to 3.2V (mid range) the scaler gain is 1/2 and for voltages greater than 3.2V (high range) the gain is 1/4. This results in the low range having an output voltage resolution of 12.5mV, the mid range having a resolution of 25mV and the high range having a resolution of 50mV. The error amp has a gain of 4 and compares the output voltage of the scaler to Vref to create an error voltage on its output. This is converted to a digital error term by the AFE ADC and is stored in the error register. The error register has a fine adjust function that can be used to improve the output voltage set point resolution by a factor of 5 resulting in a low range resolution of 2.5mV, a mid range resolution of 5mV and a high range resolution of 10mV. The output of the error register is then used by the Proportional Integral Derivative (PID) controller to manage the loop dynamics.

The XRP7725 PID is a 17-bit five-coefficient control engine that calculates the required duty cycle under the various operating conditions and feeds it to the Digital Pulse Width Modulator (DPWM). Besides the normal

coefficients the PID also uses the V_{CC} voltage to provide a feed forward function.

The XRP7725 DPWM includes a special delay timing loop that provides a timing resolution that is 16 times the master oscillator frequency (103MHz) for a timing resolution of 607ps for both the driver pulse width and dead time delays. The DWPM produces the Gate High (GH) and Gate Low (GL) signals for the driver. The maximum and minimum on-times and dead time delays are programmable by configuration resisters.

To provide current information, the output inductor current is measured by a differential amplifier that reads the voltage drop across the R_{DS} of the lower FET during its on time. There are two selectable ranges, a low range with a gain of 8 for a +20mV to -120 mV range, and a high range with a gain of 4 for a +40mV to -280mV range. The optimum range to use will depend on the maximum output current and the R_{DS} of the lower FET. The measured voltage is then converted to a digital value by the current ADC block. The resulting current value is stored in a readable register, and also used to determine when PWM to PFM transitions should occur.

PFM mode loop

The XRP7725 has a PFM loop that can be enabled to improve efficiency at light loads. By reducing switching frequency and operating in the discontinuous conduction mode (DCM), both switching and conduction losses are minimized.

Figure 17 shows a functional diagram of the PFM logic.

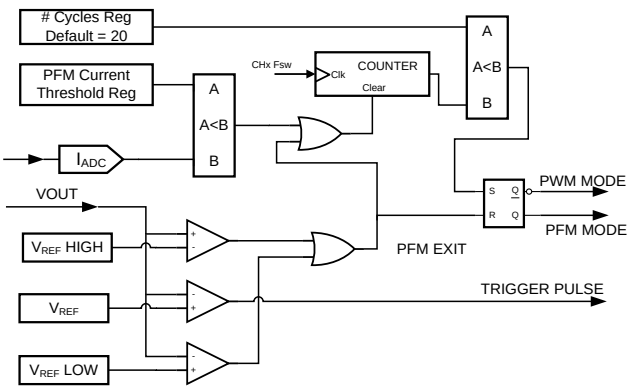


Figure 17: PFM Enter/Exit Functional Diagram

The PFM loop works in conjunction with the PWM loop and is entered when the output current falls below a programmed threshold level for a programmed number of cycles. When PFM mode is entered, the PWM loop is disabled and instead, the scaled output voltage is compared to Vref with a window comparator. The window comparator has three thresholds; normal (Vref), high (Vref + %high) and low (Vref - %low). The %high and %low values are programmable and track Vref.

In PFM mode, the normal comparator is used to regulate the output voltage. If the output voltage falls below the Vref level, the comparator is activated and triggers the DPWM to start a switching cycle. When the high side FET is turned on, the inductor current ramps up which charges up the output capacitors and increases their voltage. After the completion of the high side and low side on-times, the lower FET is turned off to inhibit any inductor reverse current flow. The load current then discharges the output capacitors until the output voltage falls below Vref and the normal comparator is activated. This triggers the DPWM to start the next switching cycle. The time from the end of the switching cycle to the next trigger is referred to as the dead zone. When PFM mode is initially entered the switching duty cycle is equal to the steady-state PWM duty cycle. This will cause the inductor ripple current to be at the same level that it was in PWM mode. During operation the PFM duty cycle is calculated based on the ratio of the output voltage to V_{CC}. This method ensures that the output

voltage ripple is well controlled and is much lower than in other architectures which use a "burst" methodology.

If the output voltage goes outside the high/low windows, PFM mode is exited and the PWM loop is reactivated.

Although the PFM mode is effective at improving efficiency at light load, at very light loads the dead zone time can increase to the point where the switching frequency can enter the audio hearing range. When this happens some components, like the output inductor and ceramic capacitors, can emit audible noise. The amplitude of the noise depends mainly on the board design and on the manufacturer and construction details of the components. Proper selection of components can reduce the sound to very low levels. In general Ultrasonic Mode is not used unless required as it reduces light load efficiency.

Ultrasonic Mode

Ultrasonic mode is an extension of PFM to ensure that the switching frequency never enters the audible range. When this mode is entered, the switching frequency is set to 30kHz and the duty cycle of the upper and lower FETs, which are fixed in PFM mode, are decreased as required to keep the output voltage in regulation while maintaining the 30kHz switching frequency.

Under extremely light or zero load currents, the GH on time pulse width can decrease to its minimum width. When this happens, the lower FET on time is increased slightly to allow a small amount of reverse inductor current to flow back into V_{IN} to keep the output voltage in regulation while maintaining the switching frequency above the audio range.

Oversampling OVS Mode

Oversampling (OVS) mode is a feature added to the XRP7725 to improve transient responses. This mode can only be enabled when the channel switching frequency is operating in 1x frequency mode. In OVS mode the output voltage is sampled four times per switching cycle and is monitored by the AFE window comparators. If the voltage goes outside the set high or low limits, the OVS control electronics can immediately modify the pulse width of the GH or GL drivers to respond accordingly, without having to wait for the next cycle to start. OVS has two types of response depending on whether the high limit is exceeded during an unloading transient (Over Voltage), or the low limit is exceeded during a loading transient (Under Voltage).

Under Voltage OVS: If there is an increasing current load step, the output voltage will drop until the regulator loop adapts to the new conditions to return the voltage to the correct level. Depending on where in the switching cycle the load step happens there can be a delay of up to one switching cycle before the control loop can respond. With OVS enabled if the output voltage drops below the lower level, an immediate GH pulse will be generated and sent to the driver to increase the output inductor current toward the new load level without having to wait for the next cycle to begin. If the output voltage is still below the lower limit at the beginning of the next cycle, OVS will work in conjunction with the PID to insert additional GH pulses to quickly return the output voltage back within its regulation band. The result of this system is transient response capabilities on par or exceeding those of a constant on-time control loop.

Over Voltage OVS: When there is a step load current decrease, the output voltage will increase (bump up) as the excess inductor current that is no longer used by the load flows into the output capacitors causing the output voltage to rise. The voltage will continue to rise until the inductor current decreases to the new load current. With OVS enabled, if the output voltage exceeds the high limit of the window comparator, a blanking pulse is generated to truncate the GH signal. This causes inductor current to immediately begin decreasing to the new load level. The GH signal will continue to be blanked until the output voltage falls below the high limit. Again, since the output voltage is sampled at four times the switching frequency, over shoot will be decreased and the time required to get back into the regulation band is also decreased.

OVS can be used in conjunction with both the PWM and PFM operating modes. When it is activated it can noticeably decrease output voltage excursions when transitioning between PWM and PFM modes.

INTERNAL DRIVERS

The internal high and low gate drivers use totem pole FETs for high drive capability. They are powered by two external 5V power pins (VCCD1-2) and (VCCD3-4), VCCD1-2 powers the drivers for channels 1 and 2 and VCCD3-4 powers channels 3 and 4. The drivers can be powered by the internal 5V LDO by connecting their power pins to the LDO5 output through an RC filter to avoid conducted noise back into the analog circuitry.

To minimize power dissipation in the 5V LDO it is recommended to power the drivers from an external 5V power source either directly or by using the V5EXT input. Good quality 1uF to 4.7uF capacitors should be connected directly between the power pins to ground to optimize driver performance and minimize noise coupling to the 5V LDO supply.

The driver outputs should be connected directly to their corresponding output switching FETs, with the Lx output connected to the drain of the lower FET for the best current monitoring accuracy.

See ANP-32 “Practical Layout Guidelines for Power^{XR} Designs.”

LDOs

The XRP7725 has two internal Low Drop Out (LDO) linear regulators that generate 5.0V (LDO5) and 3.3V (LDO3_3) for both internal and external use. Additionally it also has a 1.8V regulator that supplies power for the XRP7725 internal circuits. Figure 3 shows a block diagram of the linear power supplies. LDO5 is the main power input to the device and is supplied by an external 5.5V to 25V (V_{CC}) supply. The output of LDO5 should be bypassed by a good quality capacitor connected between the pin and ground close to the device. The 5V output is used by the XRP7725 as a standby power supply and is also used to power the 3.3V and 1.8V linear regulators inside the chip and can also supply power to the 5V gate drivers. The total output current that the 5V LDO can provide is 130mA. The XRP7725 consumes approximately 20mA and the rest is shared between LDO3_3 and the gate drive currents. *During initial power up, the maximum external load should be limited to 30mA.*

The 3.3V LDO output available on the LDO3_3 pin is solely for customer use and is not used internally. This supply may be turned on or off by the configuration registers. Again a good bypass capacitor should be used.

The AVDD pin is the 1.8V regulator output and needs to be connected externally to the DVDD pin on the device. A good quality capacitor should be connected between this pin and ground close to the package.

For operation with a V_{CC} of 4.75V to 5.5V, the LDO5 output needs to be connected directly to V_{CC} on the board.

CLOCKS AND TIMING

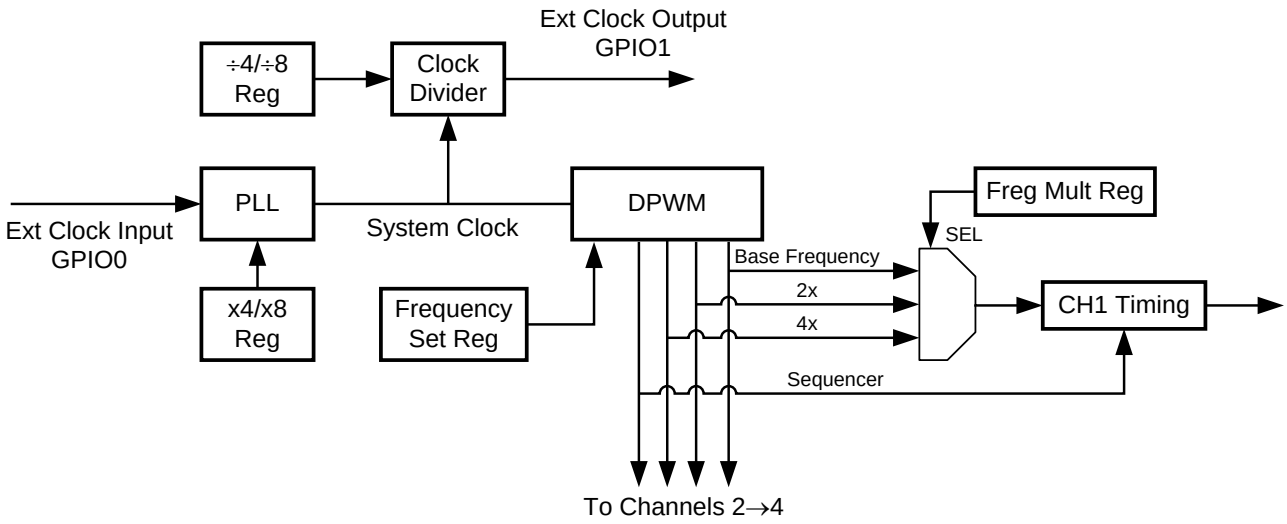


Figure 18: XRP7725 Timing Block Diagram

Figure 18 shows a simplified block diagram of the XRP7725 timing. Again, please note that the function blocks and signal names used are chosen for ease of understanding and do not necessarily reflect the actual design.

The system timing is generated by a 103MHz internal system clock (Sys_Clk). There are two ways that the 103MHz system clock can be generated. These include an internal oscillator and a Phase Locked Loop (PLL) that is synchronized to an external clock input. The basic timing architecture is to divide the Sys_Clk down to create a fundamental switching frequency (Fsw_Fund) for all the output channels that is settable from 105kHz to 306kHz. The switching frequency for a channel (Fsw_CHx) can then be selected as 1 time, 2 times or 4 times the fundamental switching frequency.

To set the base frequency for the output channels, an “Fsw_Set” value representing the base frequency shown in Table 1, is entered into the switching frequency configuration register. Note that Fsw_Set value is basically equal to the Sys_Clk divided by the base frequency. The system timing is then created by dividing down Sys_Clk to produce a base frequency clock, 2X and 4X times the base frequency clocks, and sequencing timing to position the output channels relative to each other. Each output channel then has its own frequency multiplier register that is used to select its final output switching frequency.

Table 1 shows the available channel switching frequencies for the XRP7725 device. In practice the PowerArchitect™ 5.1 (PA 5.1) design tool handles all the details and the user only has to enter the fundamental switching frequency and the 1x, 2x, 4x frequency multiplier for each channel.

If an external clock is used, the frequencies in this table will shift accordingly.

Base Frequency kHz	Available 2x Frequencies kHz	Available 4x Frequencies kHz
105.5	211.1	422.1
107.3	214.6	429.2
109.1	218.2	436.4
111.0	222.0	444.0
112.9	225.9	451.8
115.0	229.9	459.8
117.0	234.1	468.2
119.2	238.4	476.9
121.5	242.9	485.8
123.8	247.6	495.2
126.2	252.5	504.9
128.8	257.5	515.0
131.4	262.8	525.5
134.1	268.2	536.5
137.0	273.9	547.9
139.9	279.9	559.8
143.1	286.1	572.2
146.3	292.6	585.2
149.7	299.4	598.8
153.3	306.5	613.1
157.0	314.0	628.0
160.9	321.9	643.8
165.1	330.1	660.3
169.4	338.8	677.6
174.0	348.0	695.9
178.8	357.6	715.3
183.9	367.9	735.7
189.3	378.7	757.4
195.1	390.2	780.3
201.2	402.3	804.7
207.7	415.3	830.6
214.6	429.2	858.3
222.0	444.0	887.9
229.9	459.8	919.6
238.4	476.9	953.7
247.6	495.2	990.4
257.5	515.0	1030.0
268.2	536.5	1072.9
279.9	559.8	1119.6
292.6	585.2	1170.5
306.5	613.1	1226.2

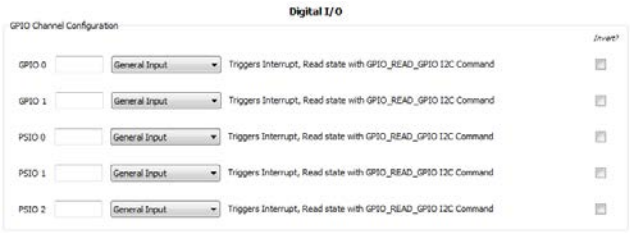
Table 1

SUPERVISORY AND CONTROL

Power system design with XRP7725 is accomplished using PA 5.1 design tool. All figures referenced in the following sections are taken from PA 5.1. Furthermore, the following sections reference I²C commands. For more information on these commands, refer to ANP-38.

DIGITAL I/O

XRP7725 has two General Purpose Input Output (GPIO) and three Power System Input Output (PSIO) user configurable pins.

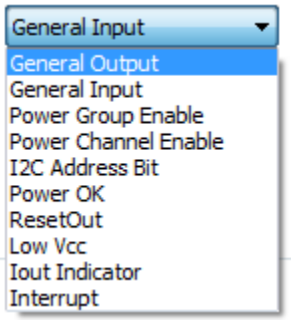


- GPIOs are 3.3V CMOS logic compatible and 5V tolerant.
- PSIOs which configured as outputs are open drain and require external pull-up resistors. These I/Os are 3.3V and 5V CMOS logic compatible, and up to 15V capable.

The polarity of the GPIO/PSIO pins is set in PA 5.1 or with an I²C command.

Configuring GPIO/PSIOs

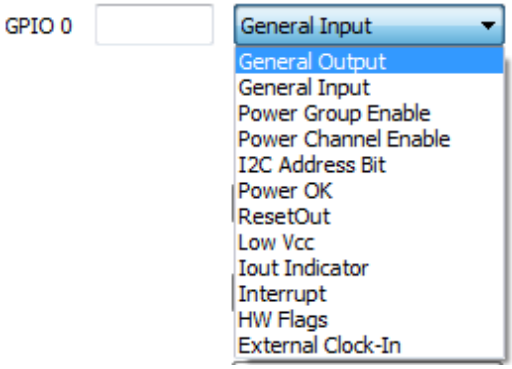
The following functions can be controlled from or forwarded to any GPIO/PSIO:



- **General Output** – set with an I²C command
- **General Input** – triggers an interrupt; state read with an I²C command
- **Power Group Enable** – controls enabling and disabling of Group 1 and Group 2
- **Power Channel Enable** – controls enabling and disabling of a individual channel including LDO3.3
- **I²C Address Bit** – controls an I²C address bit
- **Power OK** – indicates that selected channels have reached their target levels and have not faulted. Multiple channel selection is available, in which case the resulting signal is the AND logic function of all channels selected
- **ResetOut** – is delayed Power OK. Delay is programmable in 1msec increments with the range of 0 to 255 msecs
- **Low V_{CC}** – indicates when V_{CC} has fallen below the UVLO fault threshold and when the UVLO condition clears (V_{CC} voltage rises above the UVLO warning level)
- **Interrupt** – the controller generated interrupt selection and clearing is done through I²C commands

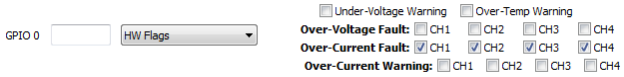
Interrupt, Low V_{CC}, Power OK and ResetOut signals can only be forwarded to a single GPIO/PSIO.

In addition, the following are functions that are unique to GPIO0 and GPIO1.

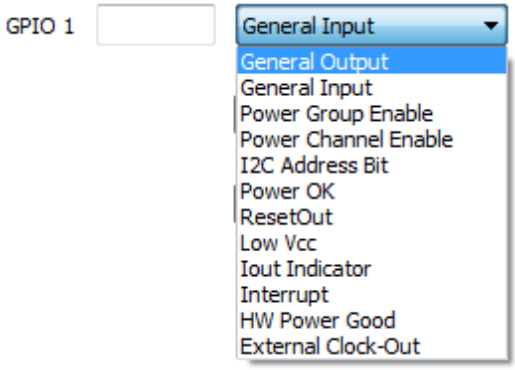


- **HW Flags** – these are hardware monitoring functions forwarded to GPIO0 only. The functions include Under-Voltage Warning, Over-Temperature Warning, Over-Voltage Fault, Over-Current Fault and Over-Current Warning for every channel.

Multiple selections will be combined using the OR logic function.

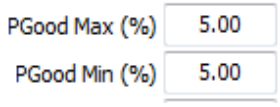


- **External Clock-in** – enables the controller to lock to an external clock including one from another XRP7725 applied to the GPIO0 pin. There are two ranges of clock frequencies the controller accepts, selectable by a user.



- **HW Power Good** – the Power Good hardware monitoring function. It can only be forwarded to GPIO1. This is an output voltage monitoring function that is a hardware comparison of channel output voltage against its user defined Power Good threshold limits (Power Good minimum and maximum levels). It has no hysteresis. Multiple channel selections will be combined using the AND logic function of all channels selected.

The Power Good minimum and maximum levels are expressed as percentages of the target voltage.



"PGood Max" is the upper window and "PGood Min" is the lower window. The minimum and maximum for each of these values can be calculated with the following equation:

$$PGOOD(\%) = \frac{N * LSB(mV) * 10^5}{Vtarget\ (V)}$$

Where N=1 to 63 for the PGOOD Max value and N=1 to 62 for the PGOOD Min value. For example, with the target voltage of 1.5V and set point resolution of 2.5mV (LSB), the Power Good min and max values can range from 0.17% to 10.3% and 0.17% to 10.5% respectively. A user can effectively double the range by changing to the next higher output voltage range setting, but at the expense of reduced set point resolution.

- **External Clock-out** – clock sent out through GPIO1 for synchronizing with another XRP7725 (see the clock out section for more information).

FAULT HANDLING

There are seven different types of fault handling:

- **Under Voltage Lockout (UVLO)** monitors voltage supplied to the V_{CC} pin and will cause the controller to shut down all channels if the supply drops to critical levels.
- **Over Temperature Protection (OTP)** monitors temperature of the chip and will cause the controller to shut down all channels if temperature rises to critical levels.
- **Over Voltage Protection (OVP)** monitors regulated voltage of a channel and will cause the controller to react in a user specified way if the regulated voltage surpasses threshold level.
- **Over Current Protection (OCP)** monitors current of a channel and will cause the controller to react in a user specified way if the current level surpasses threshold level.
- **Start-up Time-out Fault** monitors whether a channel gets into regulation in a user defined time period
- **LDO5 Over Current Protection (LDO5 OCP)** monitors current drawn from the

regulator and will cause the controller to be reset if the current exceeds LDO5 limit

- **LDO3.3 Over Current Protection (LDO3.3 OCP)** monitors current drawn from the regulator and will cause the controller to shut down the regulator if the current exceeds LDO3.3 limit

UVLO

Both UVLO warning and fault levels are user programmable and set at 200mV increments in PA 5.1.

When the warning level is reached the controller will generate the UVLO_WARNING_EVENT interrupt. In addition, the host can be informed about the event through HW Flags on GPIO0 (see the Digital I/O section).

When an under voltage fault condition occurs, the XRP7725 outputs are shut down and the UVLO_FAULT_ACTIVE_EVENT interrupt is generated. In addition, the host can be informed by forwarding the Low V_{CC} signal to any GPIO/PSIO (see the Digital I/O section). This signal transitions when the UVLO fault occurs. When coming out of the fault, rising V_{CC} crossing the UVLO fault level will trigger the UVLO_FAULT_INACTIVE_EVENT interrupt.

Once the UVLO condition clears (V_{CC} voltage rises above or to the user-defined UVLO warning level), the Low V_{CC} signal will transition and the controller will be reset.

Special attention needs to be paid in the case when V_{CC} = LDO5 = 4.75V to 5.5V. Since the input voltage ADC resolution is 200mV, the UVLO warning and fault set points are coarse for a 5V input. Therefore, setting the warning level at 4.8V and the fault level at 4.6V may result in the outputs not being re-enabled until a full 5.0V is reached on V_{CC}. Setting the warning level to 4.6V and the fault level at 4.4V would likely make UVLO handling as desired; however, at a fault level below 4.6V the device has hardware UVLO on LDO5 to ensure proper shutdown of the internal circuitry of the controller. This means the 4.4V UVLO fault level may never occur.

OTP

User defined OTP warning, fault and restart levels are set at 5°C increments in PA 5.1.

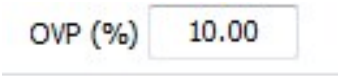
When the warning level is reached the controller will generate the TEMP_WARNING_EVENT interrupt. In addition, the host can be informed about the event through HW Flags on GPIO0 (see the Digital I/O section).

When an OTP fault condition occurs, the XRP7725 outputs are shut down and the TEMP_OVER_EVENT interrupt is generated.

Once temperature reaches a user defined OTP Restart Threshold level, the TEMP_UNDER_EVENT interrupt will be generated and the controller will reset.

OVP

A user defined OVP fault level is set in PA 5.1 and is expressed in percentages of a regulated target voltage.



Resolution is the same as for the target voltage (expressed in percentages). The OVP minimum and maximum values are calculated by the following equation where the range for N is 1 to 63:

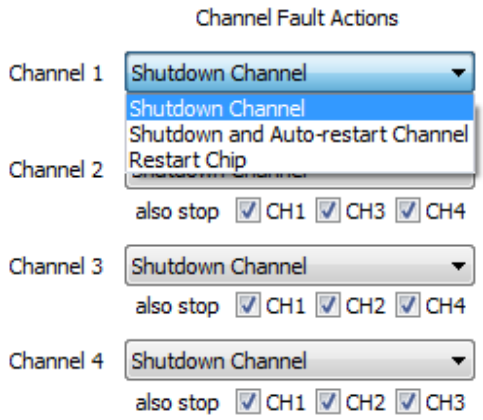
$$OVP(\%) = \frac{N * LSB(mV) * 10^5}{Vtarget\ (V)}$$

When the OVP level is reached and the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I^2C command to check which channel is at fault.

In addition, OVP fault can be monitored through GPIO0.

A user can choose one of three options in response to an OVP event: shut down the faulting channel, shut down faulting channel and perform auto-restart of the channel, or restart the chip.

WARNING: Choosing the "Restart Chip" option during development is NOT recommended as it makes debug efforts difficult.



In the case of shutting down the faulting channel and auto-restarting, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 msec increments with a maximum value of 255 msec.

Note: The Channel Fault Action response is the same for an OVP or OCP event.

OCP

A user defined OCP fault level is set with 10 mA increments in PA 5.1. PA 5.1 uses calculations to give the user the approximate DC output current entered in the current limit field. However the actual current limit trip value programmed into the part is limited to 280mV as defined in the electrical characteristics. The maximum value the user can program is limited by R_{DSON} of the synchronous Power FET and current monitoring ADC range. For example, using a synchronous FET with R_{DSON} of 30mΩ, and the wider ADC range, the maximum current limit programmed would be:

$$OCP\ Max(A) = \frac{280mV}{30m\Omega} = 9.33A$$

The current is sampled approximately 30ns before the low side MOSFET turns off, so the actual measured DC output current in this example would be 9.33A plus approximately half the inductor ripple.

An OCP Fault is considered to have occurred only if the fault threshold has been tripped in four consecutive switching cycles. When the switching frequency is set to the 4x multiplier, the current is sampled only every other cycle. As a result it can take as many as eight switching cycles for an over current event to be detected. When operating in 4x mode an inductor with a soft saturation characteristic is recommended.

When the OCP level is reached and the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I^2C command to check which channel is at fault.

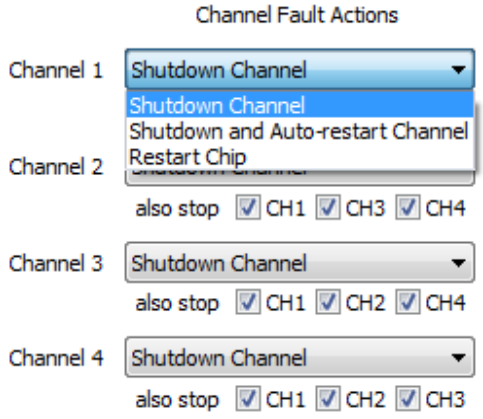
In addition, OCP faults can be monitored through HW Flags on GPIO0. The host can also monitor the OCP warning flag through HW Flags on GPIO0. The OCP warning level is calculated by PA 5.1 as 85% of the OCP fault level.

A user can choose one of three options in response to an OCP event: shut down the

faulting channel, shut down faulting channel and perform auto-restart of the channel, or restart the chip.

WARNING: Choosing the "Restart Chip" option during development is NOT recommended as it makes debug efforts difficult.

The output current reported by the XRP7725 is processed through a seven sample median filter in order to reduce noise. The OCP limit is compared against unfiltered ADC output.



For the case of Shutdown and Auto-restart Channel, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 msec increments with a maximum value of 255 msec.

Note: The Channel Fault Action response is the same for an OVP or OCP event.

Start-up Time-out Fault

A channel will be at Startup Timeout Fault if it does not come-up in the time period specified in the "Startup Timeout" box. In addition, a channel is at Startup Timeout Fault if its pre-bias configuration voltage is within a defined value too close to the target.

When the fault is generated, the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can use an I^2C command to check which channel is at fault.

LDO5 OCP

When current is drawn from the LDO5 that exceeds the LDO5 current limit the controller will be reset.

LDO3.3 OCP

When current drawn from LDO3.3 exceeds LDO3.3 current limit the regulator gets shut down, a fault is generated, and the host will be notified by the SUPPLY_FAULT_EVENT interrupt generated by the controller. The host then can through an I^2C command check which channel/regulator is at fault. Once the fault condition is removed, the host needs to turn the regulator on again.

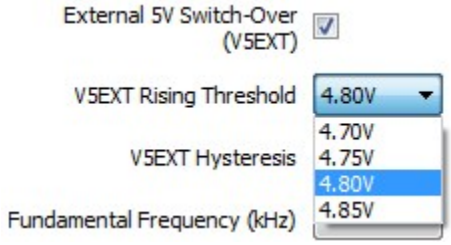
V5EXT SWITCHOVER

The V5EXT gives a user an opportunity to supply an external 5 Volt rail to the controller in order to reduce the controller's power dissipation. The 5 Volt rail can be an independent power rail present in a system or any of 7725 channels regulated to 5 Volts (in the PFM mode in particular) and routed back to the V5EXT pin. It is important to mention that voltage to V_{CC} must be applied all the time even after the switchover in which case the current drawn from V_{CC} supply will be minimal.

If the function not used, we recommend the pin to be either grounded or left floating in conjunction with making sure the function gets disabled through register settings.

V5EXT switchover control

The function is enabled in PA 5.1. The switchover thresholds are programmable in 50mV steps with a total range of 200mV. Hysteresis to switch the external 5 Volt supply in-out is 150mV. LDO5 automatically turns off when the external voltage is switched in and turns on when the external voltage drops below the lower threshold.



When the controller switches over to the V5EXT rail, the V5EXT_RISE interrupt is generated to inform the host. Similarly, when the controller switches out, the V5EXT_FALL interrupt gets generated.

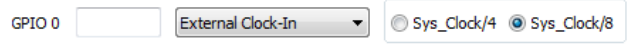
External Clock Synchronization

XRP7725 can be run off an external clock available in the system or another XRP7725. The external clock must be in the ranges of 10.9MHz to 14.7MHz or 21.8MHz to 29.6MHz. Locking to the external clock is done through an internal Phase Lock Loop (PLL) which requires an external loop capacitor of 2.2nF to be connected between the CPLL pin and AGND.

In applications where this functionality is not desired, the CPLL capacitor is not necessary and can be omitted, and the pin shall be left floating. In addition, the user needs to make sure the function gets disabled through register settings.

The external clock must be routed to GPIO0. The GPIO0 setting must reflect the range of the external clock applied to it: Sys_Clock/8 corresponds to the range of 10.9MHz to 14.7MHz while Sys_Clock/4 setting corresponds to the range of 21.8Mhz to 29.6MHz.

The functionality is enabled in PA 5.1 by selecting External Clock-in function under GPIO0.

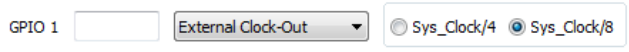


For more details on how to monitor PLL lock in-out, please contact MaxLinear or your local MaxLinear representative.

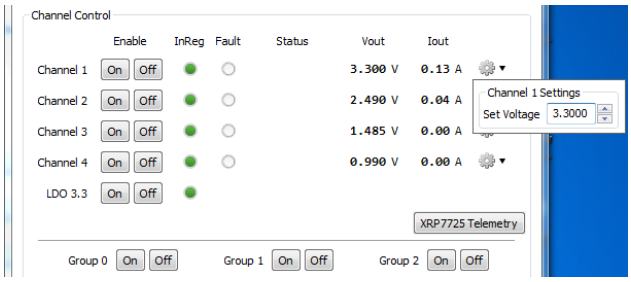
Clock Out

XRP7725 can supply clock out to be used by another XRP7725 controller. The clock is routed out through GPIO1 and can be set to system clock divided by 8 (Sys_Clock/8) or system clock divided by 4 (Sys_Clock/4) frequencies.

The functionality is enabled in PA 5.1 by selecting External Clock-Out function under GPIO1.



Channel Control



Channels including LDO3.3 can be controlled independently by any GPIO/PSIO or I²C command. Channels will start-up or shut-down following transitions of signals applied to GPIO/PSIOs set to control the channels. The control can always be overridden with an I²C command.

Regardless of whether the channels are controlled independently or are in a group, the ramp rates will be followed as specified (see the Power Sequencing section).

Regulated voltages and voltage drops across the synchronous FET on each switching channel can be read back using I²C commands. The regulated voltage read back resolution is 15mV, 30mV and 60mV per LSB depending on the target voltage range. The voltage drop across synchronous FET read back resolution is 1.25mV and 2.5mV per LSB depending on the range.

Through an I²C command the host can check the status of the channels; whether they are in regulation or at fault.

Regulated voltages can be dynamically changed on switching channels using I²C

commands with resolution of 2.5mV, 5mV and 10mV depending on the target voltage range (in PWM mode only).

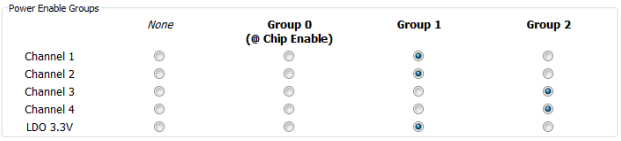
For more information on I²C commands please refer to ANP-38 or contact MaxLinear or your local MaxLinear representative.

POWER SEQUENCING

All four channels and LDO3.3 can be grouped together and will start-up and shut-down in a user defined sequence.

Selecting none means channel(s) will not be assigned to any group and therefore will be controlled independently.

Group Selection



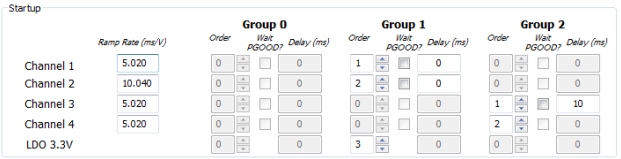
There are three groups:

- **Group 0** – is controlled by the chip ENABLE or an I²C command. Channels assigned to this group will come up with the ENABLE signal being high (plus additional delay needed to load configuration from Flash to run-time registers), and will go down with the ENABLE signal being low. The control can always be overridden with an I²C command

  Since it is recommended to leave the ENABLE pin floating in the applications when V_{CC} = LDO5 = 4.75V to 5.5V, please contact MaxLinear for how to configure the channels to come up at the power up in this scenario

- **Group 1** – can be controlled by any GPIO/PSIO or I²C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I²C command
- **Group 2** – can be controlled by any GPIO/PSIO or I²C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I²C command

Start-up

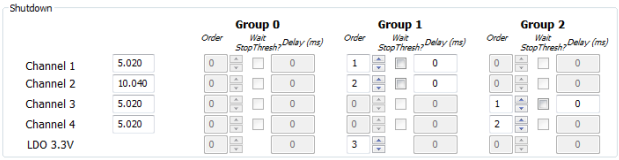


For each channel within a group, a user can specify the following start-up characteristics:

- **Ramp Rate** – expressed in milliseconds per volt. It does not apply to LDO3.3

- **Order** – position of a channel to come-up within the group
- **Wait PGOOD?** – selecting this option for a channel means the next channel in the order will not start ramping-up until this channel reaches the target level and its Power Good flag is asserted
- **Delay** – an additional time delay a user can specify to postpone a channel start-up with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0msec to 255msec

Shut-down



For each channel within a group a user can specify the following shut-down characteristics:

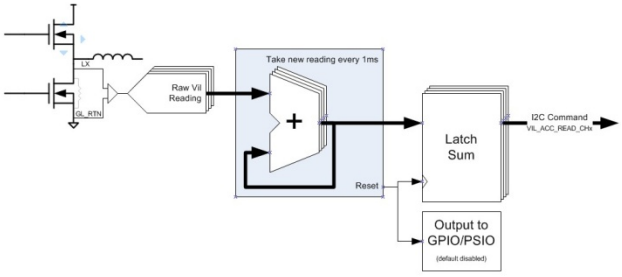
- **Ramp Rate** – expressed in milliseconds per volt. It does not apply to LDO3.3
- **Order** – position of a channel to come-down within the group
- **Wait Stop Thresh?** – selecting this option for a channel means the next channel in the order will not start ramping-down until this channel reaches the Stop Threshold level. The stop threshold level is fixed at 600mV
- **Delay** – additional time delay a user can specify to postpone a channel shut-down with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0msec to 255msec

MONITORING V_{CC} AND TEMPERATURE

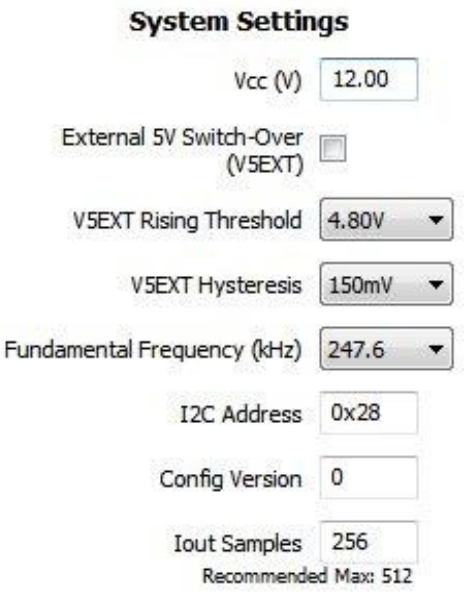
Through I^2C commands, the host can read back the voltage applied to the V_{CC} pin and the die temperature respectively. The V_{CC} read back resolution is 200mV per LSB; the die temperature read back resolution is 5C° per LSB. For more on I^2C commands please refer to ANP-38.

INSTANTANEOUS CURRENT MONITORING

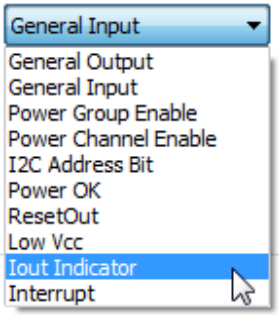
XRP7725 will capture V_{IL} readings every 1msec on all channels until a user defined sample threshold is reached. Then, the sum is latched into a separate register to be read from an I^2C command.



The sample size is selected in Power Architect 5.1 (PA 5.1). The recommended maximum sample size is 512. Going over this limit could potentially cause overflow. In certain designs it would be possible to increase sample size above this limit without problems, but this will depend on the design parameters. If there is such a need please contact MaxLinear representatives who will determine if your design is suitable.



The host should time its reading frequency to match the sample window size. A GPIO/PSIO can be configured in PA 5.1 to indicate to the host each time a new accumulated sum has been latched.



The IO will be asserted after all samples have been taken and held while the accumulated values are being latched.

Reading of the accumulated sum is done using following I²C commands:

0x71 (VIL_ACC_READ_CH1) – CH1 Accumulator

0x72 (VIL_ACC_READ_CH2) – CH2 Accumulator

0x73 (VIL_ACC_READ_CH3) – CH3 Accumulator

0x74 (VIL_ACC_READ_CH4) – CH4 Accumulator

The internal counter can be reinitialized by reading from the following I²C command:

0x70 (VIL_ACC_INIT) – Accumulator Initialization

These I²C commands follow the same command structure as the commands described in ANP-38.

Once the host reads the accumulated sum, it will need to do some post data processing in order to get an average load current.

First, the host has to divide the read sum by a number of samples to obtain an average V_{IL} register value.

Secondly, the average V_{IL} register value needs to be translated into a load current.

Translating average V_{IL} register value into a load current

To adjust for the gain and offset of the sense circuit the average V_{IL} register value needs to be converted to V_{IL}. That can be done with the following equation:

$$V_{GL\_RTN} - V_{LX} = V_{IL} = \frac{DEC(R\_Value) * 0.01}{IFE\_Gain} - 0.04$$

Equation 1

where IFE_Gain is a gain setting of the sense circuit. The IFE_Gain equals to 8 if Gain 8 of the sense circuit is enabled, else IFE_Gain is 4.

PA 5.1 sets the gain based on R_{DSON}, I_{OUTMAX} values entered, and current sense ADC range. The IFE_Gain value can be obtained by reading register 0xD016 via the PA 5.1 Peek Poke function. This is a four bit register with following bit description:

Bit 0 – IFE_Gain 8 setting for channel 1

Bit 1 – IFE_Gain 8 setting for channel 2

Bit 2 – IFE_Gain 8 setting for channel 3

Bit 3 – IFE_Gain 8 setting for channel 4

Value 1 indicates gain 8 setting while value 0 indicates gain 4.

Reading this register from customer software requires implementation of I²C register read command structure described in ANP-39.

The flash equivalent of this register is 0x156 if obtaining the value from flash HEX image is preferred.

Since V_{IL} is a voltage sensed across synchronous Power FET during its on time, the current through will be:

$$I = \frac{V_{IL}}{R_{DSON}}$$

Equation 2

where R_{DSON} is channel resistance of the synchronous Power FET entered as a channel parameter in PA 5.1.

In addition, XRP7725 samples V_{IL} at valley of the inductor current which means one half of the inductor ripple current has to be added to current in equation 2 in order to get an average inductor current (load current). Inductor ripple current is calculated as:

$$I_{Peak-Peak-Ripple} = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{(V_{IN} * f_{SW} * L)}$$

Equation 3

where V_{IN}, V_{OUT}, f_{SW} and L are channel parameters entered in PA 5.1.

Finally, the load current is a sum of the valley current (equation 2) and one half of the inductor ripple current (equation 3).

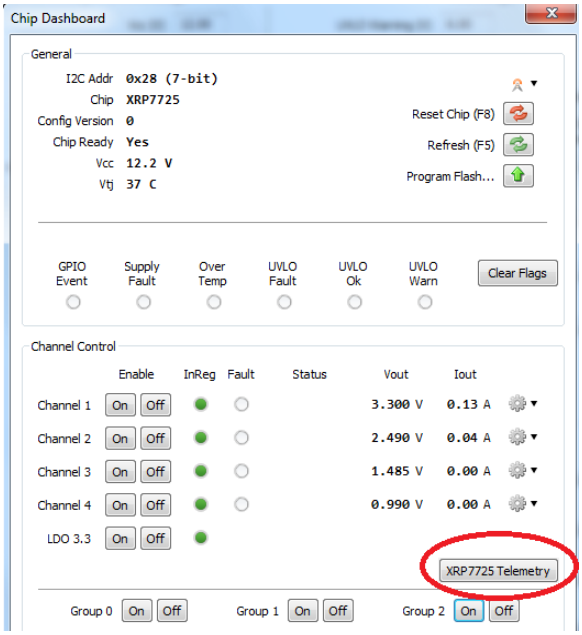
$$I_{Load} = I_{LValley} + \frac{I_{Peak-Peak-Ripple}}{2}$$

Equation 4

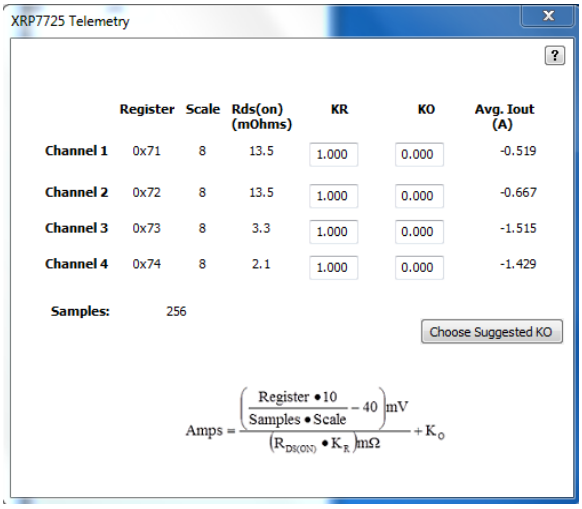
Note: the calculated load current is dependent on parameters entered in PA 5.1. R_{DSON} and L are the most significant since they will change noticeably depending on operating conditions. Because of this, calibrating R_{DSON} and L can greatly improve accuracy. For more on R_{DSON} and L calibration techniques refer to ANP-43.

XRP7725 Telemetry in PA 5.1

PA 5.1 adds a new function under the dashboard called XRP7725 Telemetry.



The function displays load currents calculated as described in the section above. In addition, it gives a user an opportunity to make adjustments to R_{DSON} (K_R) and ripple current offset (K_O).



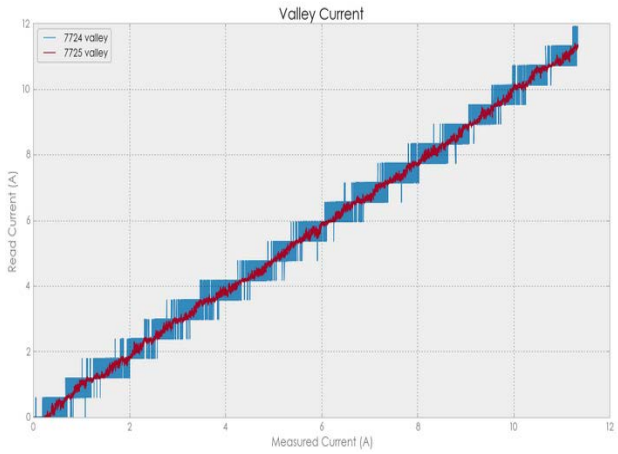
The default value of K_R is 1. PA 5.1 will calculate K_O based on entered design parameters such as V_{IN}, V_{OUT}, f_{SW} and L. The calculated K_O can be recalled by clicking on "Choose Suggested K_O."

Once the design has been calibrated, saving the project file (.pwrxr) will save K_R and K_O for later use as well.

The scale and sample values will always reflect what is saved in a project file. PA 5.1 will also read actual register values and report discrepancies highlighted in red if there exist during design development.

CURRENT READING ACCURACY

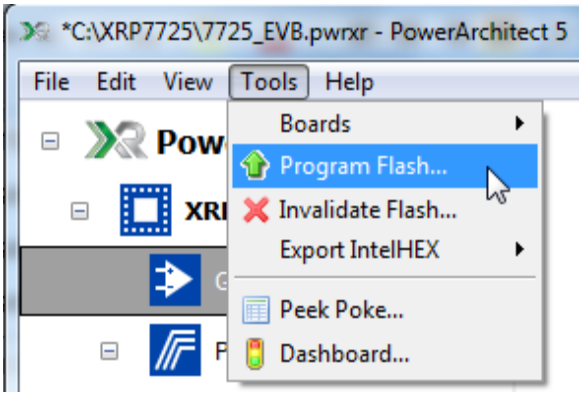
An important advantage of averaging current readings across a large sample size is that a distribution gets much tighter compared to current reading through I^2C bus in XRP7724. The accuracy specification in the electrical table includes quantization noise. Quantization noise is divided down by the square root of the number of samples taken by the accumulator. For example, if 400 samples are taken, the quantization noise is reduced by a factor of 20. The result below shows how the current reading is much improved whether the noise is from the board or quantization noise.

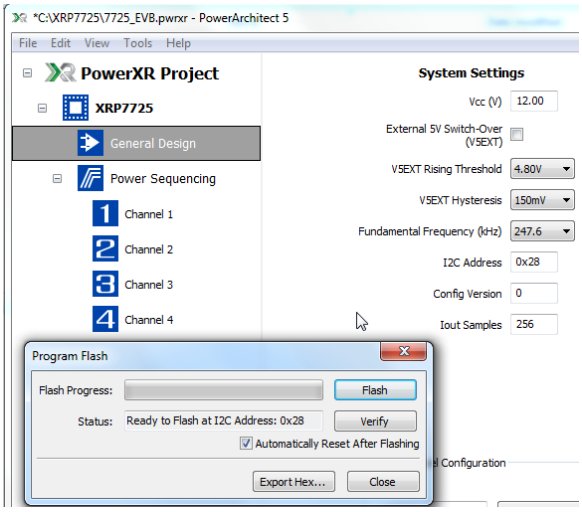


PROGRAMMING XRP7725

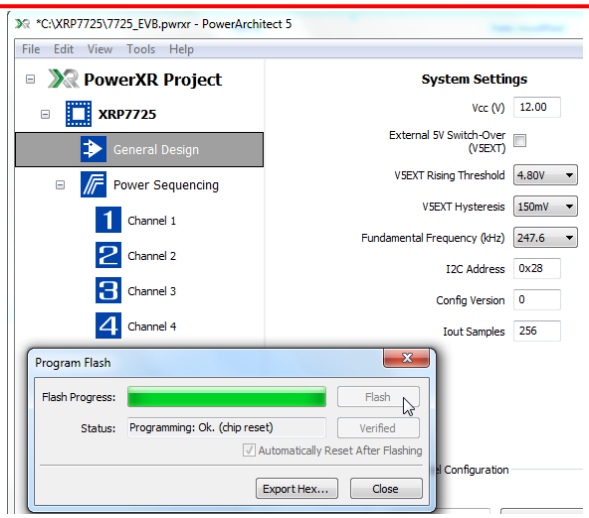
XRP7725 is a FLASH based device which means its configuration can be programmed into FLASH NVM and re-programmed a number of times.

Programming of FLASH NVM is done through PA 5.1.





By clicking on the Flash button, user will start programming sequence of the design configuration into the Flash NVM. After the programming sequence completes, the chip will reset (if automatically reset After Flashing box is checked), and boot the design configuration from the Flash.



For users that wish to create their own programming procedure so they can re-program Flash in-circuit using their system software, please contact MaxLinear for a list of I²C Flash Commands needed.

ENABLING XRP7725

XRP7725 has a weak internal pull-up ensuring it gets enabled as soon as internal voltage supplies have ramped up and are in regulation.

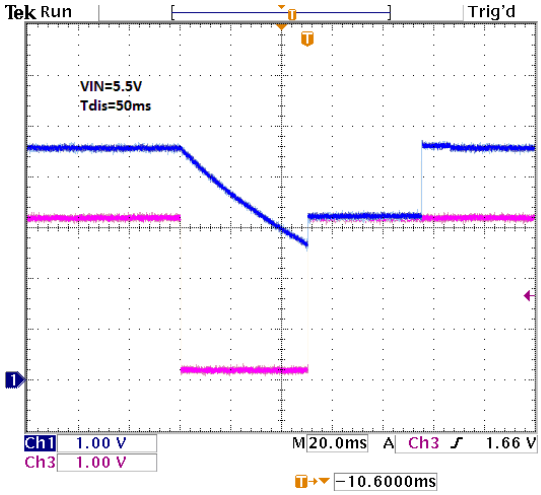
Driving the Enable pin low externally will keep the controller in the shut-down mode. A simple open drain pull down is the recommended way to shut XRP7725 down.

If the Enable pin is driven high externally to control XRP7725 coming out of the shut-down mode, care must be taken in such a scenario to ensure the Enable pin is driven high after V_{CC} gets supplied to the controller.

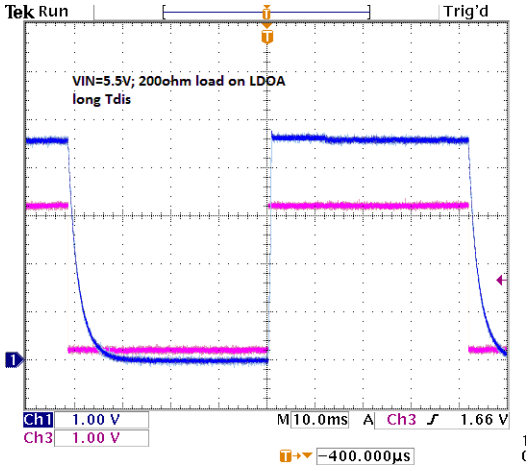
In the configuration when V_{CC} = LDO5 = 4.75V to 5.5V, disabling the device by grounding the Enable pin is not recommended. At this time we recommend leaving the Enable pin floating and placing the controller in the "Standby Mode" instead in this scenario. The standby mode is defined as the state when all switching channels and LDO3.3 are disabled, all GPIO/PSIOs are programmed as inputs, and system clock is disabled. In this state chip consumes 440uA typical.

Short duration Enable pin toggled low

Short duration shutdown pulses to the ENABLE pin of the XRP7725, which do not provide sufficient time for the LDO5 voltage to fall below 3.5V, can result in significant delay in re-enabling of the device. Some examples below show LDO5 and ENABLE pins:



No load on LDO5, blue trace. Recovery time after ENABLE logic high is approximately 40ms.



Adding a 200 ohm load on LDO5 pulls voltage below 3.5V and restart is short.

Note that as V_{CC} increases, the restart time falls as well. 5.5V input is shown as the worst case.

Since the ENABLE pin has an internal current source, a simple open drain pull down is the

recommended way to shut down the XRP7725. A diode in series with a resistor between the LDO5 and ENABLE pins may offer a way to more quickly pull down the LDO5 output when the ENABLE pin is pulled low.

APPLICATION INFORMATION

THERMAL DESIGN

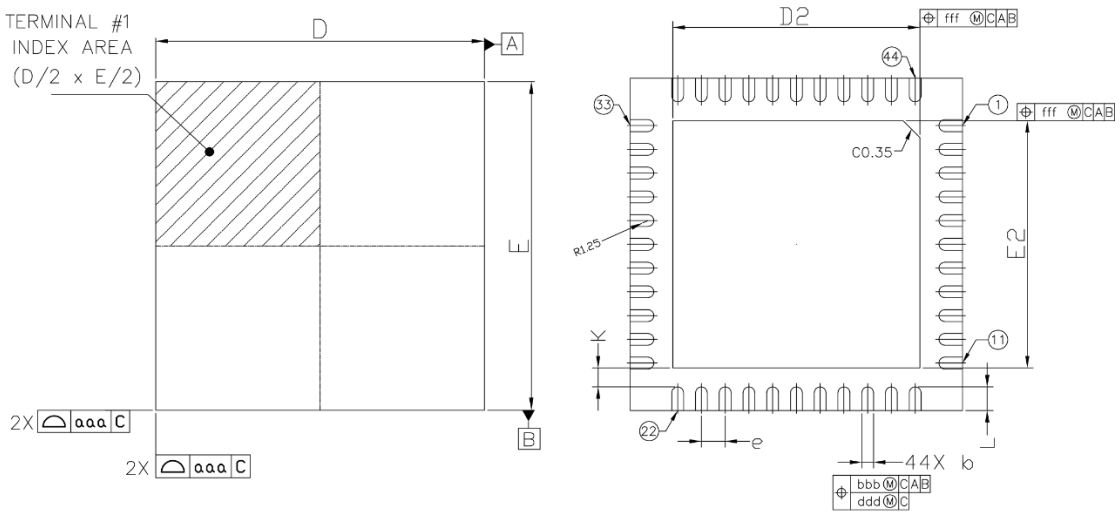
As a four channel controller with internal MOSFET drivers and 5V gate drive supply all in one 7x7mm 44pin TQFN package, there is the potential for the power dissipation to exceed the package thermal limitations. The XRP7725 has an internal LDO which supplies 5V to the internal circuitry and MOSFET drivers during startup. It is generally expected that either one of the switching regulator outputs is 5V or another 5V rail is available in the system and connected to the 5 Volt EXT pin. If there is no 5V available in the system, then the power loss will increase significantly and proper thermal design becomes critical. For lower power levels using properly sized MOSFETs, the use of the internal 5V regulator as a gate drive supply is considered appropriate.

LAYOUT GUIDELINES

Refer to application note ANP-32 “Practical Layout Guidelines for Power^{XR} Designs and ANP-35 “XRP77XX: Extending the MOSFET Gate Drive Conductors”.

MECHANICAL DIMENSIONS

44-PIN 7X7MM TQFN



DIM / SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20Ref	
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	5.00	5.15	5.30
E2	5.00	5.15	5.30
L	0.40	0.50	0.60
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		44	

TERMINAL DETAILS

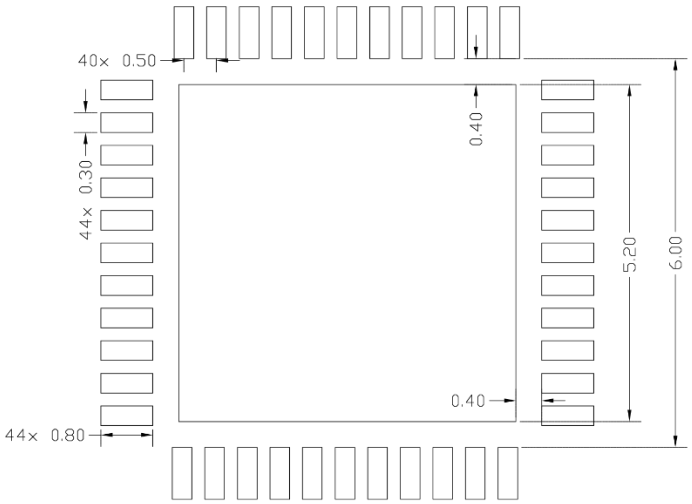
NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000049

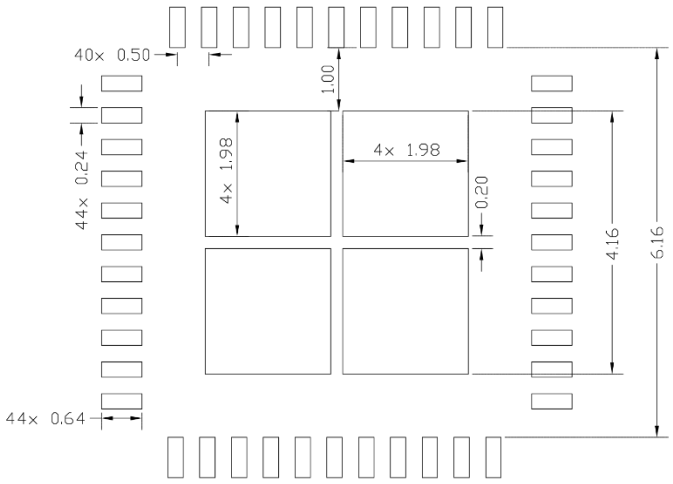
Revision: B

RECOMMENDED LAND PATTERN AND STENCIL

44-PIN 7X7MM TQFN



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000049

Revision: B

REVISION HISTORY

Revision	Date	Description
1.0.0	01/27/2014	Initial Release [ECN# 14xx-xx]
1.0.1	06/07/2018	Update to MaxLinear logo. Update format and Ordering Information. Corrected figure numbers.

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

High Performance Analog:
1060 Rincon Circle
San Jose, CA 95131
Tel.: +1 (669) 265-6100
Fax: +1 (669) 265-6101
www.exar.com

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