CY7C1018CV33



Features

- Pin- and function-compatible with CY7C1018BV33
- High speed

—t_{AA} = 10 ns

- CMOS for optimum speed/power
- Center power/ground pinout
- Data retention at 2.0V
- Automatic power-down when deselected
- Easy memory expansion with \overline{CE} and \overline{OE} options
- Available in Pb-free and non Pb-free 300-mil-wide 32-pin SOJ

Functional Description^[1]

The CY7C1018CV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tri-state drivers. This

Logic Block Diagram

128K x 8 Static RAM

device has an automatic power-down feature that significantly reduces power consumption when deselected.

<u>Writing</u> to the device is <u>accomplished</u> by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins $(I/O_0 \text{ through } I/O_7)$ is then written into the location specified on the address pins $(A_0 \text{ through } A_{16})$.

Reading from the device is accomplished by taking Chip Enable (\underline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in <u>a</u> high-impedance state when the <u>device</u> is deselected (CE HIGH), the <u>outputs</u> are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1018CV33 is available in a standard 300-mil-wide SOJ.

Pin Configurations





Note:
1. For guidelines on SRAM system designs, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

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Selection Guide

		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Comm'l	90	85	80	mA
	Ind'l		85		mA
Maximum Standby Current	•	5	5	5	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage on V_{CC} Relative to G	SND ^[2] –0.5V to + 4.6V
DC Voltage Applied to Outputs ^[6]	
in High-Z State	–0.5V to V _{CC} + 0.5V
DC Input Voltage ^[2]	–0.5V to V _{CC} + 0.5V

Electrical Characteristics Over the Operating Range

Current into Outputs (LOW)...... 20 mA Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015) Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	V _{cc}
Commercial	0°C to +70°C	$3.3V\pm10\%$
Industrial	–40°C to +85°C	$3.3V\pm10\%$

					–10		–12		–15	
Parameter	Description	Test Conditio	ns	Min.	Max.	Min.	Max.	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = – 4.0 mA		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA			0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage			2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V _{IL}	Input LOW Voltage ^[2]			-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND <u><</u> V _I ≤ V _{CC} , Output Disabled		-1	+1	-1	+1	-1	+1	μΑ
I _{CC}	V _{CC} Operating		Comm'l		90		85		80	mA
	Supply Current	$I_{OUT} = 0 \text{ mA},$ f = f _{MAX} = 1/t _{RC}	Ind'l				85			mA
I _{SB1}	Automatic CE	Max. V _{CC} , <u>CE</u> ≥ V _{IH}	Comm'l		15		15		15	mA
	Power-down Current —TTL Inputs	V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Ind'l				15			mA
I _{SB2}	Automatic CE		Comm'l		5		5		5	mA
	Power-down Current —CMOS Inputs	$CE \ge V_{CC} - 0.3V,$ $V_{IN} \ge V_{CC} - 0.3V,$ or $V_{IN} \le 0.3V, f = 0$	Ind'l				5			mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	8	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.3V$	8	pF

Notes:

 $[\]begin{array}{ll} 2. & V_{IL} \mbox{ (min.)} = -2.0V \mbox{ for pulse durations of less than 20 ns.} \\ 3. & Tested initially and after any design or process changes that may affect these parameters. \end{array}$



AC Test Loads and Waveforms^[4]





Switching Characteristics Over the Operating Range^[5]

		-	10	-	12		15	
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle	<u>.</u>		•		•	•		-
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	CE LOW to Data Valid		10		12		15	ns
t _{DOE}	OE LOW to Data Valid		5		6		7	ns
t _{LZOE}	OE LOW to Low-Z	0		0		0		ns
t _{HZOE}	OE HIGH to High-Z ^[6, 7]		5		6		7	ns
t _{LZCE}	CE LOW to Low-Z ^[7]	3		3		3		ns
t _{HZCE}	CE HIGH to High-Z ^[6, 7]		5		6		7	ns
t _{PU} ^[8]	CE LOW to Power-up	0		0		0		ns
t _{PD} ^[8]	CE HIGH to Power-down		10		12		15	ns
Write Cycle ^{[9,}	10]	•						
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	CE LOW to Write End	8		9		10		ns
t _{AW}	Address Set-up to Write End	8		9		10		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	WE Pulse Width	7		8		10		ns
t _{SD}	Data Set-up to Write End	5		6		8		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	WE HIGH to Low-Z ^[7]	3		3		3		ns
t _{HZWE}	WE LOW to High-Z ^[6, 7]		5		6		7	ns

Notes:

AC characteristics (except High-Z) for all speeds are tested using the Thèvenin load shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c). 4.

Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (d) of AC Test Loads. Transition is measured \pm 500 mV from steady-state voltage. 5. 6.

7.

At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.

8.

This parameter is guaranteed by design and is not tested. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and <u>hold</u> timing should be referenced to the leading edge of the signal that terminates the Write. The minimum Write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}. 9.

10.



CY7C1018CV33

Switching Waveforms

Read Cycle No. 1^[11, 12]



Read Cycle No. 2 (OE Controlled)^[12, 13]



Write Cycle No. 1 (CE Controlled)^[14, 15]



Notes:

- 11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.

- WE is HIGH for Read cycle.
 WE is HIGH for Read cycle.
 Address valid prior to or coinc<u>ide</u>nt with CE transition LOW.
 Data I/O is high impedance if OE = V_{IH}.
 If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Write Cycle No. 2 (WE Controlled, OE HIGH During Write)^[14, 15]



Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[10, 15]



Truth Table

CE	OE	WE	I/O ₀ –I/O ₇	Mode	Power
Н	Х	Х	High-Z	Power-down	Standby (I _{SB})
L	L	Н	Data Out	Read	Active (I _{CC})
L	Х	L	Data In	Write	Active (I _{CC})
L	Н	Н	High-Z	Selected, Outputs Disabled	Active (I _{CC})

Note:

16. During this period the I/Os are in the output state and input signals should not be applied.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1018CV33-10VC	51-85041	32-lead 300-mil Molded SOJ	Commercial
12	CY7C1018CV33-12VC		32-lead 300-mil Molded SOJ	Commercial
	CY7C1018CV33-12VXI		32-lead 300-mil Molded SOJ (Pb-Free)	Industrial
15	CY7C1018CV33-15VXC		32-lead 300-mil Molded SOJ (Pb-Free)	Commercial

Package Diagram

32-lead (300-mil) Molded SOJ (51-85041)



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Document History Page

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109426	12/14/01	HGK	New Data Sheet
*A	113432	04/10/02	NSL	AC Test Loads split based on speed
*В	115046	05/30/02	HGK	I _{CC} and I _{SB1} modified
*C	116476	09/16/02	CEA	Add applications foot note on data sheet, pg 1
*D	493543	See ECN	NXR	Added Industrial Operating Range Removed 8 ns speed bin from Product offering Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated the Ordering Information Table