

### 3.3V Low Skew 1-to-4, 800MHz, Differential to LVDS Fanout Buffer

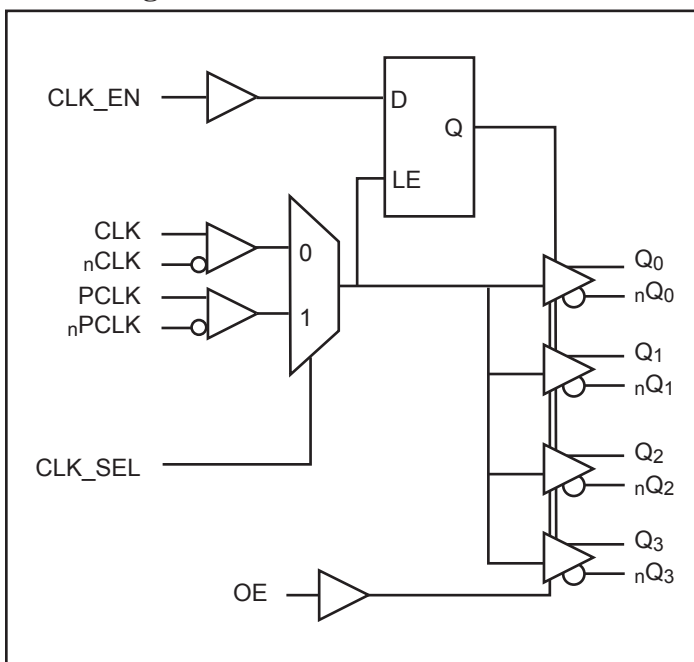
#### Features

- Maximum operation frequency: 800 MHz
- 4 pair of differential LVDS outputs
- Selectable differential CLK and PCLK inputs
- CLK, nCLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- PCLK, nPCLK pair supports LVPECL, CML and SSTL input level
- Output Skew: 40ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 2.2ns (maximum)
- 3.3V power supply
- Pin-to-pin compatible to ICS8543
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green):  
-20-pin TSSOP (L)

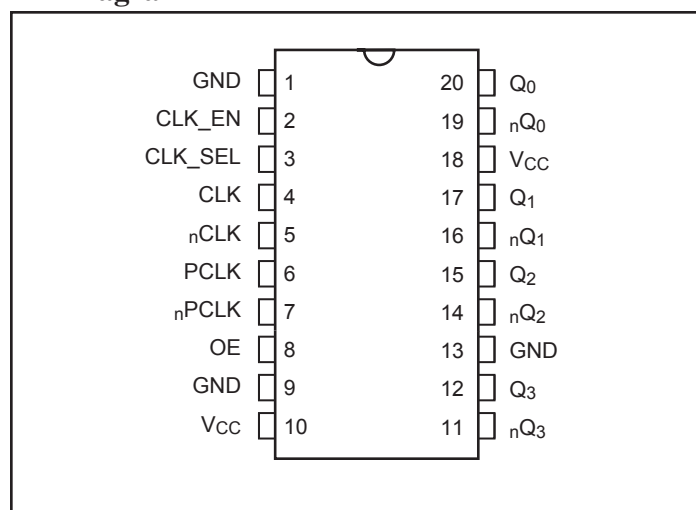
#### Description

The PI6C48543 is a high-performance low-skew LVDS fanout buffer. PI6C48543 features two selectable differential inputs and translates to four LVDS outputs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LPECL or LVDS or LVHSTL or SSTL or HCSL signals, and PCLK input accepts LVPECL or SSTL or CML signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK\_EN pin. PI6C48543 is ideal for differential to LVDS translations and/or LVDS clock distribution. Typical clock translation and distribution applications are data-communications and telecommunications.

#### Block Diagram



#### Pin Diagram



### Pin Description

Name	Pin #	Type	Description
GND	1, 9, 13	P	Connect to Ground
CLK_EN	2	I_PU	Synchronized clock enable. When high, clock outputs follow clock input. When low, Q <sub>x</sub> outputs are forced low, <sub>n</sub> Q <sub>x</sub> outputs are forced high. LVCMOS/LVTTL level with 80kΩ pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK <sub>1</sub> input. When low, selects CLK <sub>0</sub> input. LVCMOS/LVTTL level with 80kΩ pull down.
CLK	4	I_PD	Non-inverting differential clock input
<sub>n</sub> CLK	5	I_PU	Inverting differential clock input
PCLK	6	I_PD	Non-inverting differential clock input
<sub>n</sub> PCLK	7	I_PU	Inverting differential clock input
OE	8	I_PU	Output Enable, Controls outputs Q <sub>0</sub> , <sub>n</sub> Q <sub>0</sub> through Q <sub>3</sub> , <sub>n</sub> Q <sub>3</sub>
V <sub>CC</sub>	10, 18	P	Connect to 3.3V.
Q <sub>3</sub> , <sub>n</sub> Q <sub>3</sub>	11, 12	O	Differential output pair, LVDS interface level.
Q <sub>2</sub> , <sub>n</sub> Q <sub>2</sub>	14, 15	O	Differential output pair, LVDS interface level.
Q <sub>1</sub> , <sub>n</sub> Q <sub>1</sub>	16, 17	O	Differential output pair, LVDS interface level.
Q <sub>0</sub> , <sub>n</sub> Q <sub>0</sub>	19, 20	O	Differential output pair, LVDS interface level.

**Notes:**

1. I = Input, O = Output, P = Power supply connection, I\_PD = Input with pull down, I\_PU = Input with pull up

### Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance			6		pF
R <sub>pullup</sub>	Input Pullup Resistance			80		kΩ
R <sub>pulldown</sub>	Input Pulldown Resistance			80		

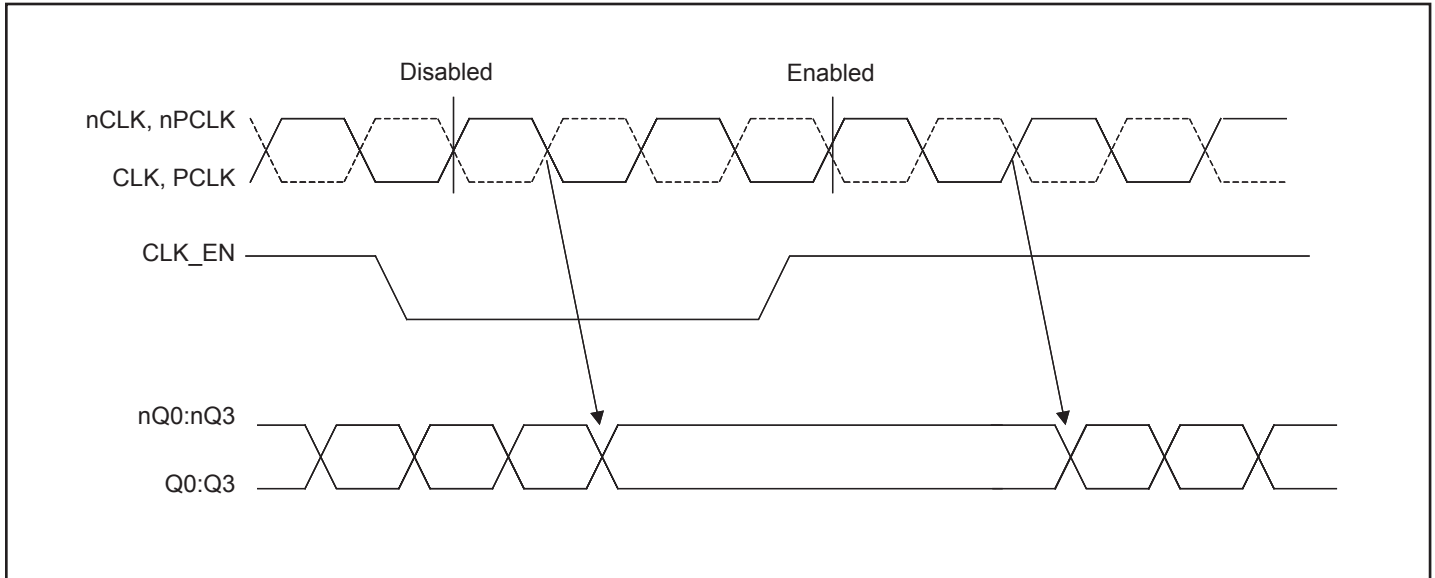
### Control Input Function Table

Inputs				Outputs	
OE	CLK_EN	CLK_SEL	Selected Source	Q <sub>0</sub> :Q <sub>3</sub>	<sub>n</sub> Q <sub>0</sub> : <sub>n</sub> Q <sub>3</sub>
1	0	0	CLK, <sub>n</sub> CLK	Diabld: Low	Diabld: High
1	0	1	PCLK, <sub>n</sub> PCLK	Disabled: Low	Disabled: High
1	1	0	CLK, <sub>n</sub> CLK	Enabled	Enabled
1	1	1	PCLK, <sub>n</sub> PCLK	Enabled	Enabled
0	x	x		Hi-Z	Hi-Z

**Notes:**

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

**Figure 1. CLK\_EN Timing Diagram**



**Clock Input Function Table** (See Figure 2)

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	nCLK or nPCLK	Q0:Q3	nQ0:nQ3		
0	1	LOW	HIGH	Differential to Differential	None Inverting
1	0	HIGH	LOW	Differential to Differential	None Inverting
0	Biased; $V_{IN} = V_{CC}/2$	LOW	HIGH	Single Ended to Differential	None Inverting
1	Biased; $V_{IN} = V_{CC}/2$	HIGH	LOW	Single Ended to Differential	None Inverting
Biased; $V_{IN} = V_{CC}/2$	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; $V_{IN} = V_{CC}/2$	1	LOW	HIGH	Single Ended to Differential	Inverting

**Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{CC}$	Supply voltage	Referenced to GND			4.6	V
$V_{IN}$	Input voltage	Referenced to GND	-0.5		$V_{CC}+0.5V$	
$V_{OUT}$	Output voltage	Referenced to GND	-0.5		$V_{CC}+0.5V$	
$T_{STG}$	Storage temperature		-65		150	°C

**Notes:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>CC</sub>	Power Supply Voltage		3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Temperature		-40		85	°C
I <sub>CC</sub>	Power Supply Current				60	mA

### LVC MOS/LVTTL DC Characteristics (T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 3.135V to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
V <sub>IH</sub>	Input High Voltage		2		3.765	V	
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8		
I <sub>IH</sub>	Input High Current	CLK_SEL	V <sub>IN</sub> = V <sub>CC</sub> = 3.465V			150	μA
		CLK_EN, OE	V <sub>IN</sub> = V <sub>CC</sub> = 3.465V			5	
I <sub>IL</sub>	Input Low Current	CLK_SEL	V <sub>IN</sub> = 0V, V <sub>CC</sub> = 3.465V	-5			
		CLK_EN, OE	V <sub>IN</sub> = 0V, V <sub>CC</sub> = 3.465V	-150			

### Differential DC Characteristics (T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 3.135V to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
I <sub>IH</sub>	Input High Current	nCLK, nPCLK	V <sub>IN</sub> = V <sub>CC</sub> = 3.465V			5	μA
		CLK, PCLK	V <sub>IN</sub> = V <sub>CC</sub> = 3.465V			150	μA
I <sub>IL</sub>	Input Low Current	nCLK, nPCLK	V <sub>CC</sub> = 3.465V, V <sub>IN</sub> = 0V	-150			μA
		CLK, PCLK	V <sub>CC</sub> = 3.465V, V <sub>IN</sub> = 0V	-5			μA
V <sub>PP</sub>	Peak-to-peak Voltage		0.15		1.3	V	
V <sub>CMR</sub>	Common Mode Input Voltage <sup>(1)</sup>		0.5		V <sub>CC</sub> -0.85V	V	

**Notes:**

- For single ended applications, the maximum input voltage for CLK and nCLK is V<sub>CC</sub>+0.3V

### LVPECL DC Characteristics (T<sub>A</sub> = -40°C to 85°C, V<sub>CC</sub> = 3.135V to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
I <sub>IH</sub>	Input High Current	nCLK, nPCLK	V <sub>IN</sub> = V <sub>CC</sub> = 3.465V			5	μA
		CLK, PCLK	V <sub>IN</sub> = V <sub>CC</sub> = 3.465V			150	
I <sub>IL</sub>	Input Low Current	nCLK, nPCLK	V <sub>CC</sub> = 3.465V, V <sub>IN</sub> = 0V	-150			
		CLK, PCLK	V <sub>CC</sub> = 3.465V, V <sub>IN</sub> = 0V	-5			
V <sub>PP</sub>	Peak-to-peak Voltage		0.3		1	V	
V <sub>CMR</sub>	Common Mode Input Voltage; Note <sup>(1)</sup>		1.5		V <sub>CC</sub>		

**Notes:**

- For single ended applications, the maximum input voltage for PCLK and nPCLK is V<sub>CC</sub>+0.3V.

**LVDS DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.135\text{V}$  to  $3.465\text{V}$  unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{OD}$	Differential Output Voltage		200	280	360	mV
$\Delta V_{OD}$	VOD Magnitude Change			0	40	
$V_{OS}$	Offset Voltage		1.125	1.25	1.375	V
$\Delta V_{OS}$	VOS Magnitude Change			5	25	mV
$I_{OZ}$	High Impedance Leakage Current		-10		+10	$\mu\text{A}$
$I_{OFF}$	Power OFF Leakage		-20	$\pm 1$	+20	
$I_{OSD}$	Differential Output Short Circuit Current			-3.5	-5	mA
$I_{OS}$	Output Short Circuit Current			-3.5	-5	
$V_{OH}$	Output Voltage High			1.34	1.6	V
$V_{OL}$	Output Voltage Low		0.9	1.06		

**AC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.135\text{V}$  to  $3.465\text{V}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{\max}$	Output Frequency				800	MHz
$t_{pd}$	Propagation Delay <sup>(1)</sup>	$f \leq 800$ MHz	1.0		2.2	ns
$T_{sk(o)}$	Output-to-output Skew <sup>(2)</sup>				40	ps
$T_{sk(pp)}$	Part-to-part Skew <sup>(3)</sup>				300	
$t_r/t_f$	Output Rise/Fall time	20% - 80%	100		300	
odc	Output duty cycle		48		52	%

**Notes:**

1. Measured from the differential input crossing point to the differential output crossing point
2. Skew between outputs with the same supply voltage and equal load conditions. Measured at the differential outputs crossing point.
3. Skew between outputs on different parts operating with the same supply voltage and equal load conditions. Measured at the differential outputs crossing point.
4. All parameters are measured at 500 MHz unless noted otherwise

**Applications Information**

***Wiring the differential input to accept single ended levels***

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3\text{V}$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .

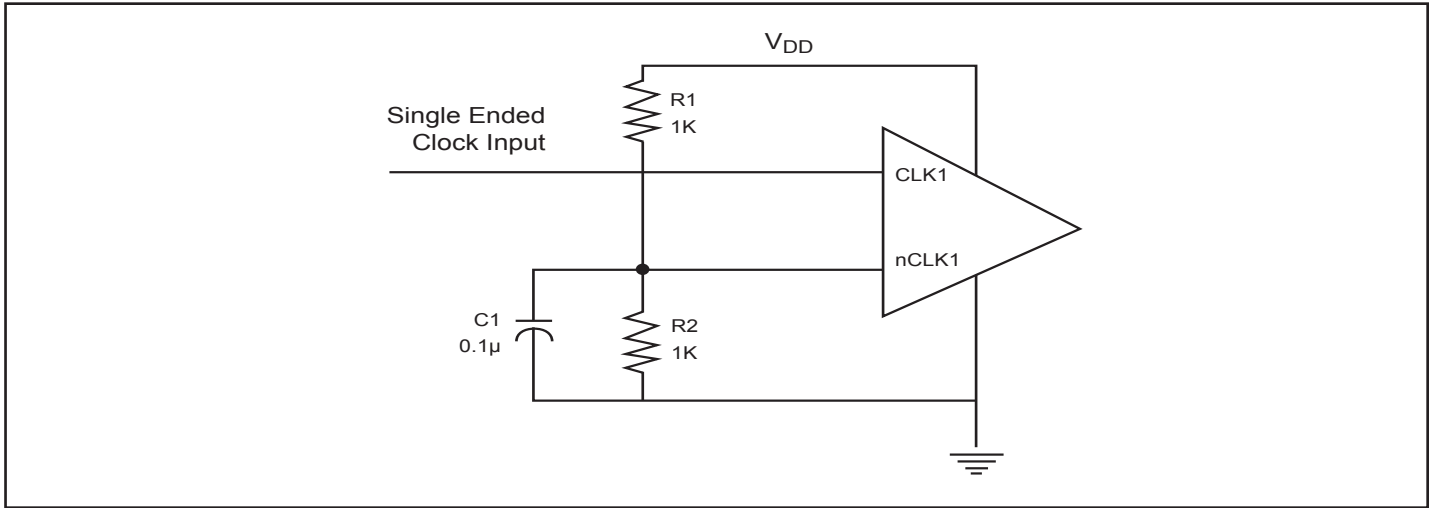
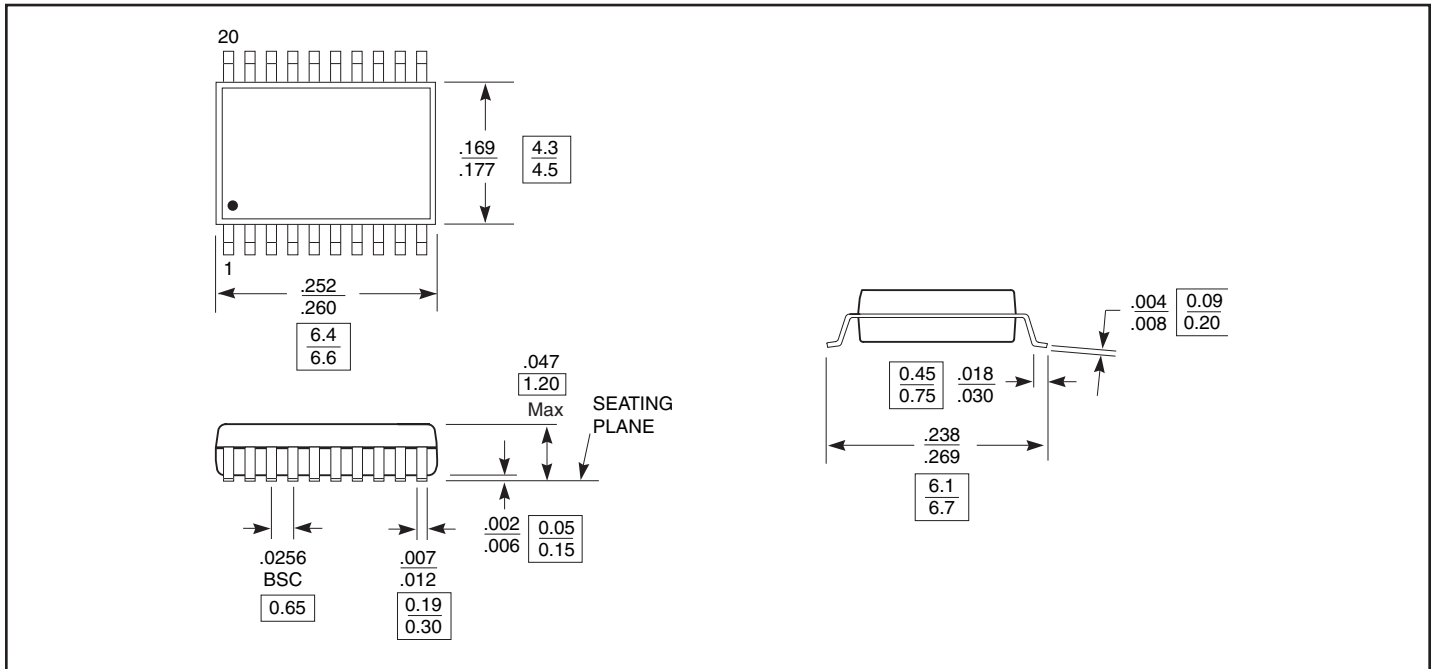


Figure 1: Single-ended Signal Driving Differential Input

### Packaging Mechanical: 20-Pin TSSOP (L)



### Ordering Information

Ordering Code	Package Code	Package Description
PI6C48543LE	L	Pb-free & Green 20-pin 173-mil wide TSSOP

#### Notes:

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)

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