DS14C89A Quad CMOS Receiver

Check for Samples: DS14C89A

FEATURES

- **Meets EIA/TIA-232-E and CCITT V.28 Standards**
- **Failsafe - Output High for Open Input**
- **LOW Power Consumption**
- **On Chip Noise Filter**
- **Available in SOIC Package**

DESCRIPTION

The DS14C89A, pin-for-pin compatible to the DS1489A/MC1489A, ia a quad receiver designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate levels conforming to EIA-232E and CCITT V.28 standards to TTL/CMOS logic levels.

The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to their bipolar equivalents: 900 µA (DS14C89A) versus 26 mA (DS1489A).

The DS14C89A provides on chip noise filtering which eliminates the need for external response control filter capacitors. When replacing the DS1489A with the DS14C89A, the response control filter pins can be tied high, low, or not connected.

Connection Diagram

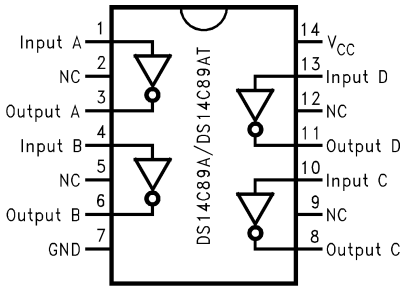


Figure 1. See Package Number D, NFF0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

V_{CC}		+6V
Input Voltage		−30V to +30V
Receiver Output Voltage		(V_{CC}) +0.3V to GND−0.3V
Junction Temperature		+150°C
Continuous Power Dissipation @ +25°C(3)	NFF0014A Package	1513 mW
	D Package	1063 mW
Lead Temp.	(Soldering 4 seconds)	+260°C
Storage Temp. Range		−65°C to +150°C
ESD Rating ≥ 1.8 kV, Typically ≥ 2 kV (HMB, 1.5 kΩ, 100 pF)		

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of AC Electrical Characteristics specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Derate NFF0014A Package 12.1 mW/°C, and D Package 8.5 mW/°C above +25°C.

Recommended Operating Conditions

		Min	Max	Units
V_{CC} (GND = 0V)		+4.5	+5.5	V
Operating Free Air Temp. (T_A)	DS14C89A	0	+75	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Input High Threshold			1.3		2.7	V
V_{TL}	Input Low Threshold			0.5		1.9	V
V_{HY}	Typical Input Hysteresis				1.0		V
I_{IN}	Input Current	V_{IN} = +25V	V_{CC} = +4.5V to +5.5V	3.6		8.3	mA
		V_{IN} = −25V		−3.6		−8.3	mA
		V_{IN} = +3V		0.43		1.0	mA
		V_{IN} = −3V		−0.43		−1.0	mA
		V_{IN} = +15V	V_{CC} = 0V (Power-Off)(1)	2.14		5.0	mA
		V_{IN} = −15V		−2.14		−5.0	mA
		V_{IN} = +3V		0.43		1.0	mA
		V_{IN} = −3V		−0.43		−1.0	mA
V_{OH}	Output High Voltage	V_{IN} = V_{TL} (min)	I_{OUT} = −3.2 mA	2.8	4.0		V
			I_{OUT} = −20µA	3.5	4.7		V
V_{OL}	Output Low Voltage	V_{IN} = V_{TH} (max) I_{OUT} = +3.2 mA			0.15	0.4	V
I_{CC}	Supply Current	No Load, V_{IN} = 2.7V or 0.5V			0.5	900	µA

(1) Under the power-off supply conditions it is assumed that the power supply potential drops to zero (0V) and is replaced by a low impedance or short circuit to ground.

AC Electrical Characteristics(1)

Over recommended operating conditions, unless otherwise specified, C_l = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	Input Pulse Width ≥ 10 µs		3.5	6.5	µs
t_{PHL}	Propagation Delay High to Low	Input Pulse Width ≥ 10 µs		3.2	6.5	µs
t_{SK}	Typical Propagation Delay Skew			400		ns
t_r	Output Rise TIme			40	300	ns
t_f	Output Fall Time			40	300	ns
t_{nw}	Pulse Width assumed to be Noise				1.0	µs

(1) AC input waveforms for test purposes: t_r = t_f = 200 ns, V_{IH} = +3V, V_L = −3V, f = 20 KHz.

Parameter Measurement Information

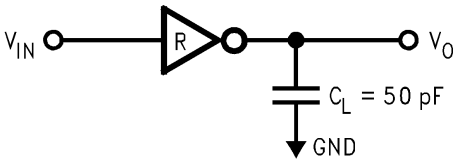


Figure 2. Receiver Load Circuit

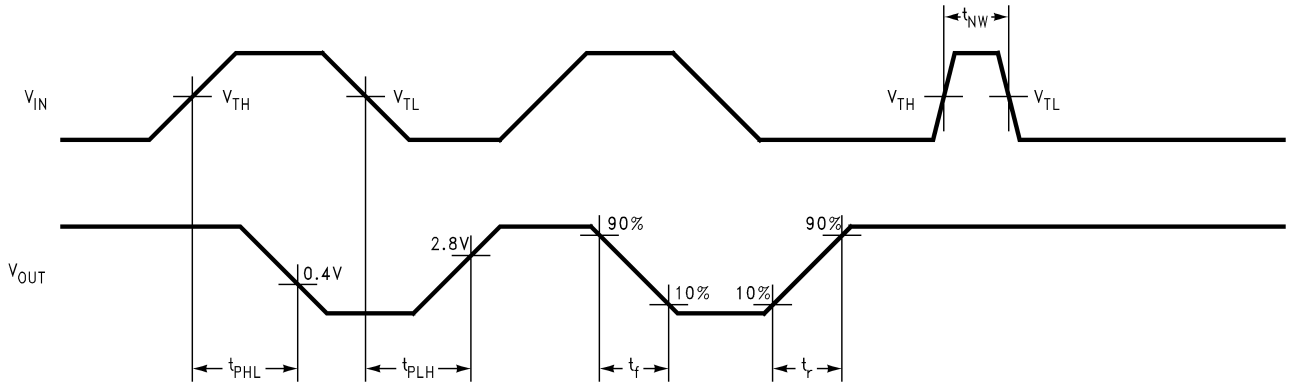


Figure 3. Receiver Switching Waveform (2)

(2) AC input waveforms for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = +3V$, $V_L = -3V$, f = 20 KHz.

TYPICAL APPLICATION INFORMATION

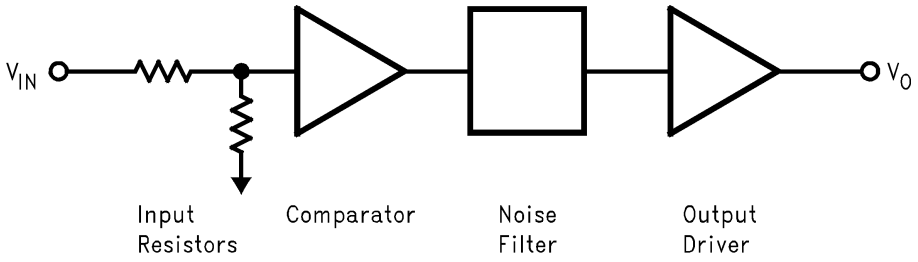


Figure 4. Receiver Block Diagram

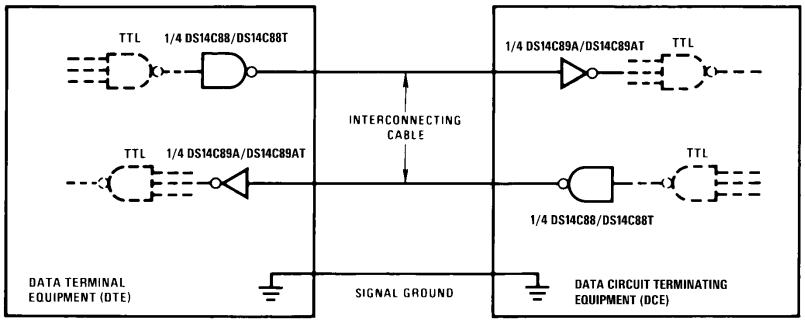


Figure 5. EIA-232D Data Transmission

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS14C89AM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	0 to 70	DS14C89AM	Samples
DS14C89AMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		DS14C89AM	Samples
DS14C89AN/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	0 to 70	DS14C89AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

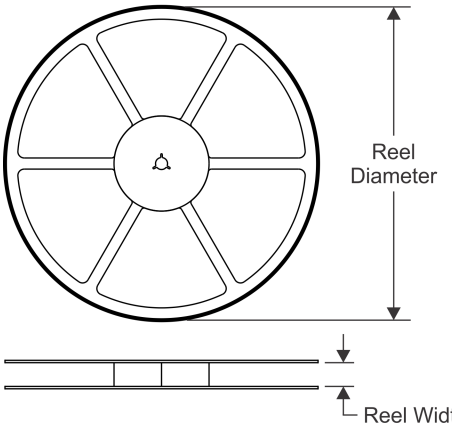
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

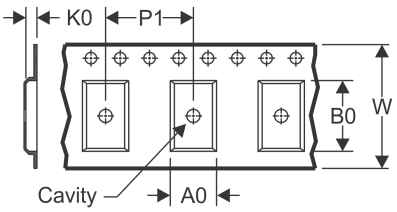
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

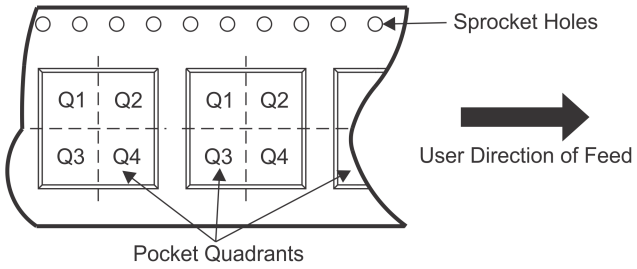


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

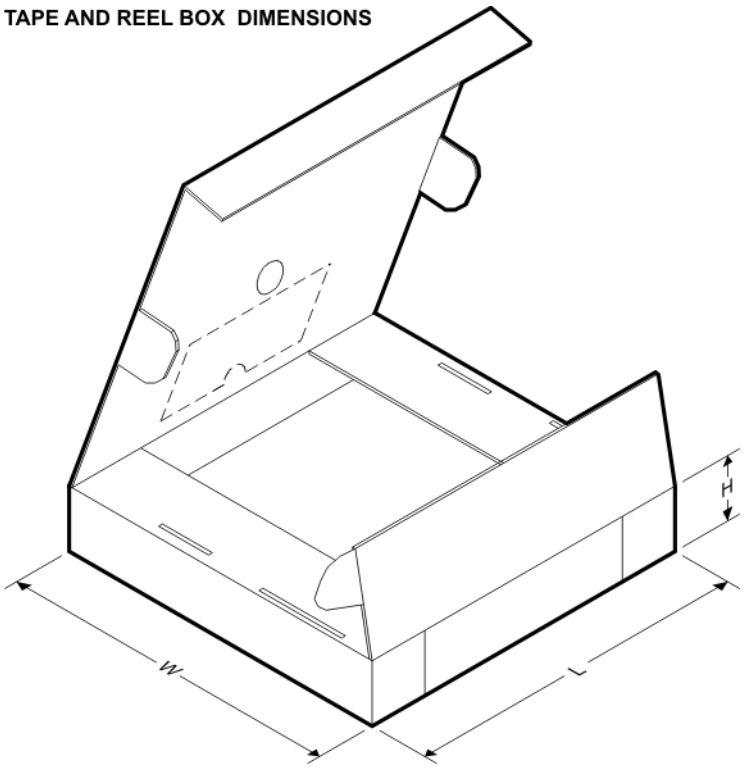
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS14C89AMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

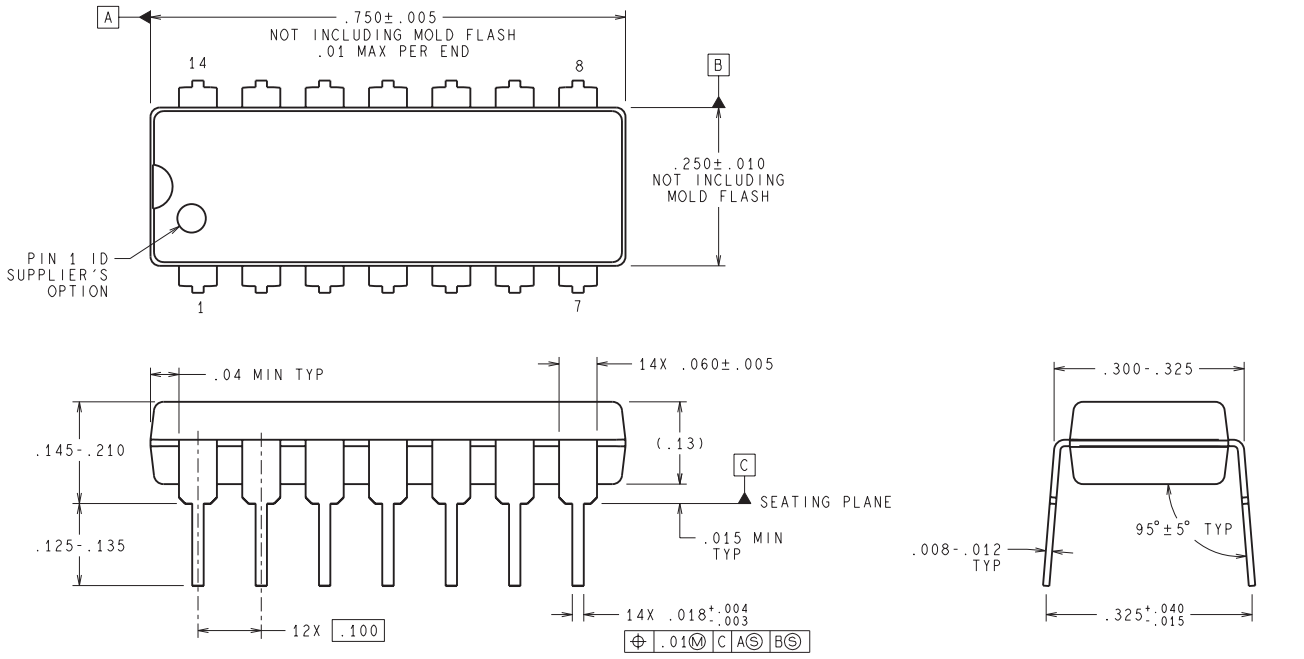
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS14C89AMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

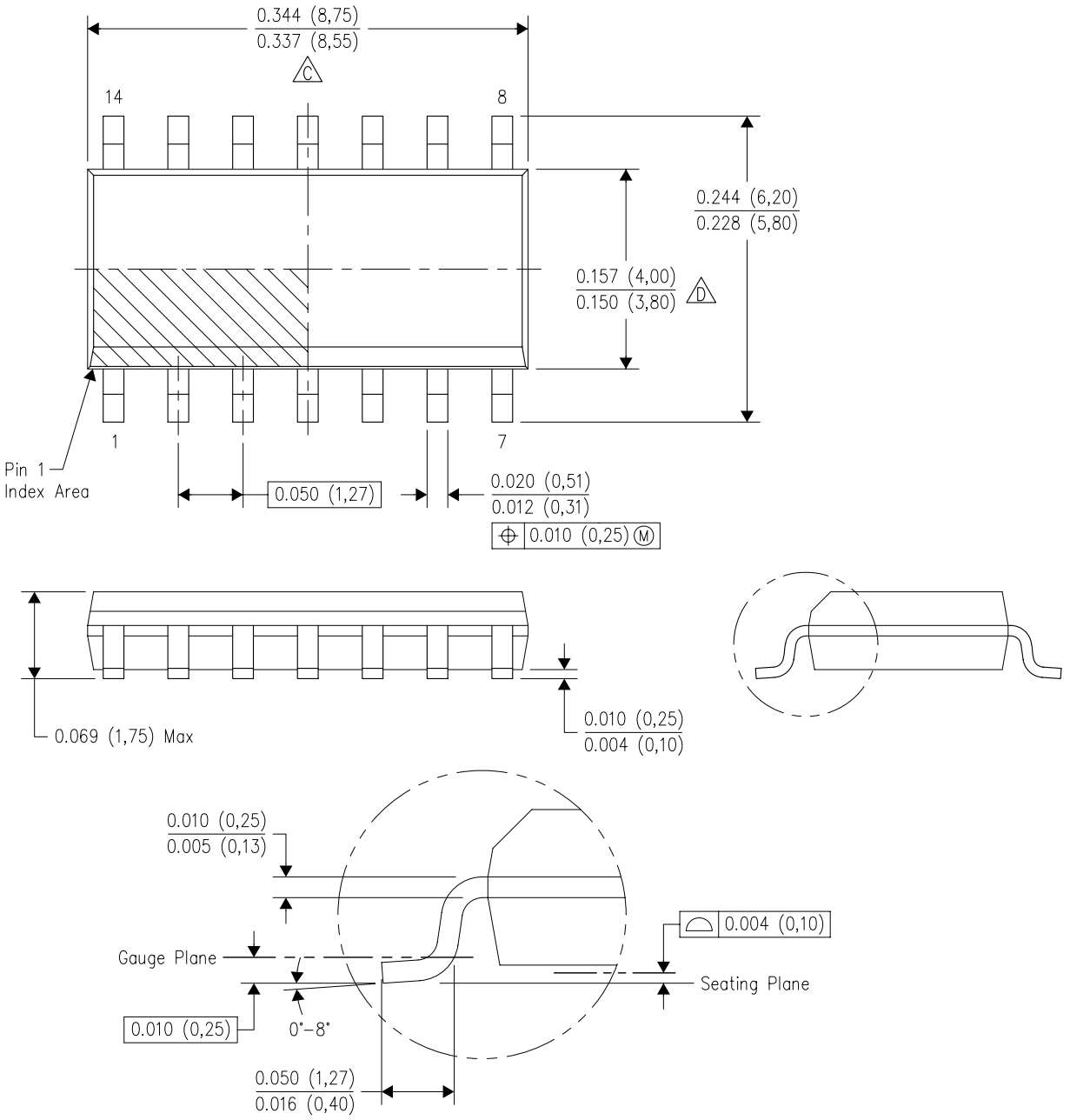
NFF0014A



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

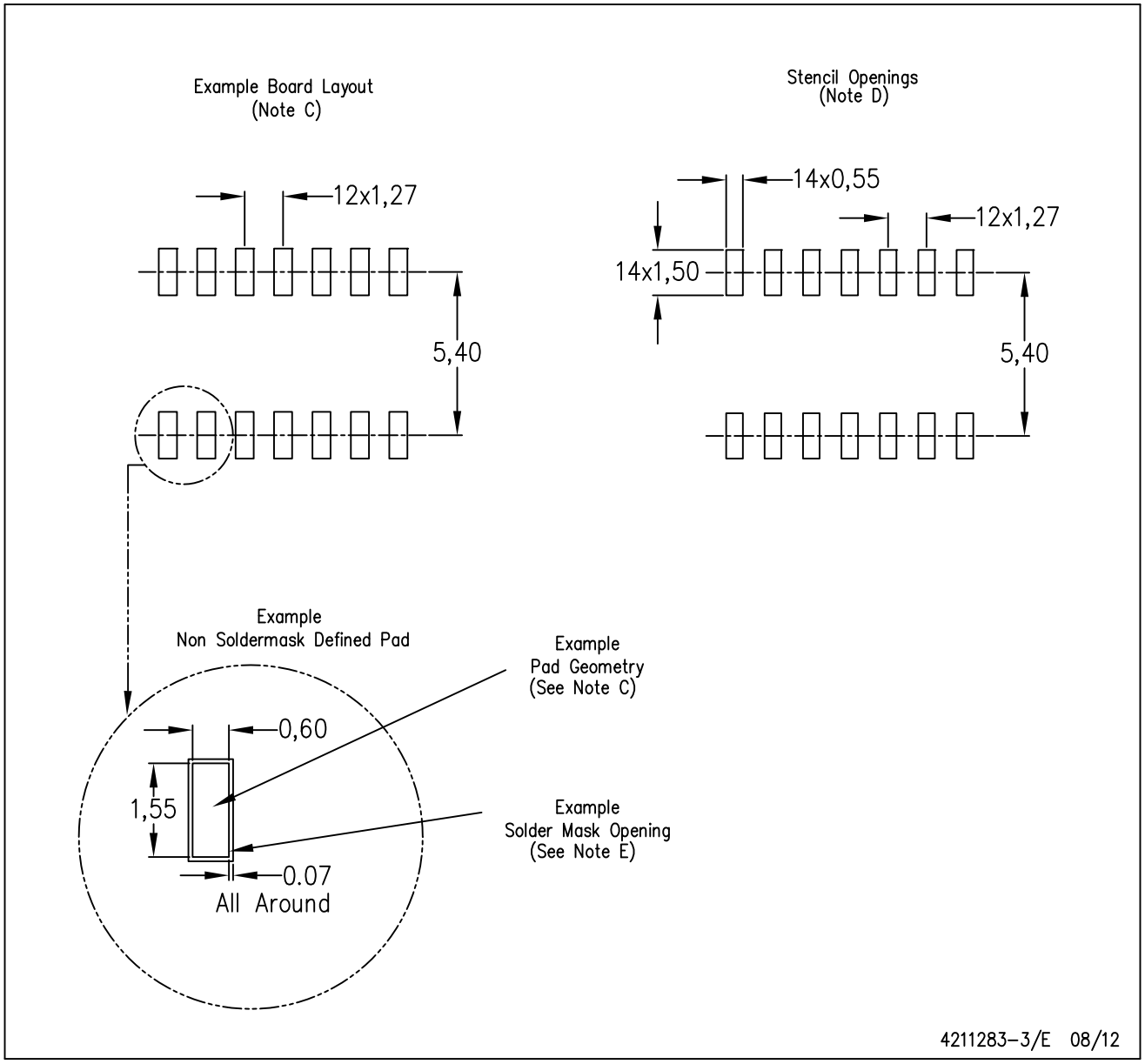
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265