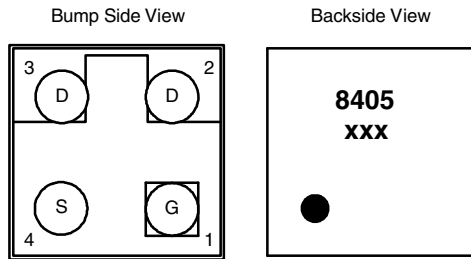


12 V P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
- 12	0.055 at V _{GS} = - 4.5 V	- 4.9
	0.070 at V _{GS} = - 2.5 V	- 4.4
	0.090 at V _{GS} = - 1.8 V	- 4

MICRO FOOT



Device Marking: 8405
xxx = Date/Lot Traceability Code

Ordering Information: Si8405DB-T1-E1 (Lead (Pb)-free and Halogen-free)

FEATURES

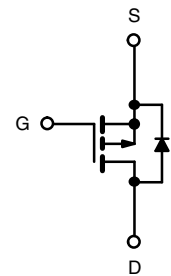
- TrenchFET[®] Power MOSFET
- MICRO FOOT[®] Chipscale Packaging
Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- PA, Battery and Load Switch
- Battery Charger Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	V _{DS}	- 12		V
Gate-Source Voltage	V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	- 4.9	- 3.6
		T _A = 70 °C	- 3.9	- 2.8
Pulsed Drain Current	I _{DM}	- 10		A
Continuous Source Current (Diode Conduction) ^a	I _S	- 2.5	- 1.3	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.77	1.47
		T _A = 70 °C	1.77	0.94
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C
Package Reflow Conditions ^b	IR/Convection	260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 s	35	45	°C/W
		Steady State	72	85	
Maximum Junction-to-Foot (drain)	R _{thJF}	16	20		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.

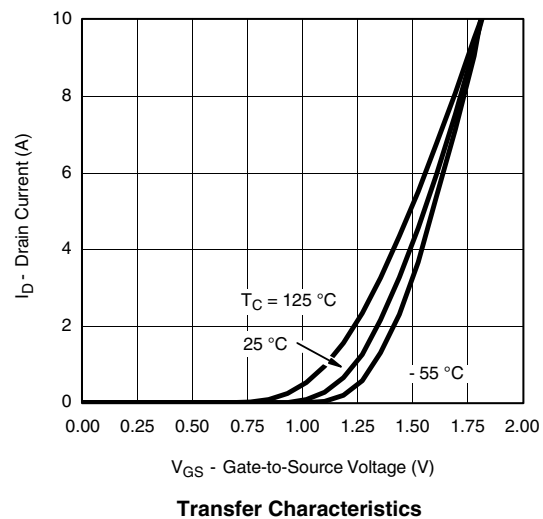
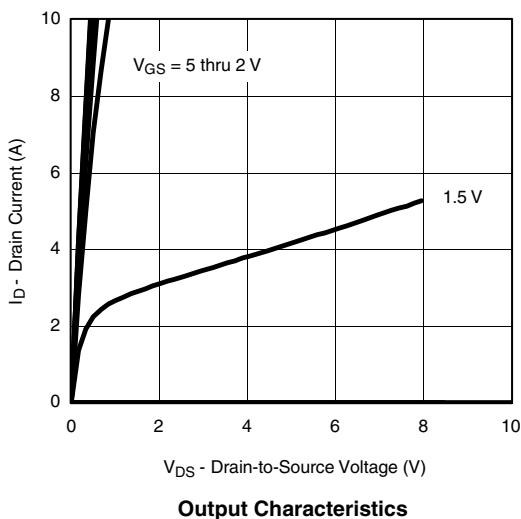
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.45	-0.7	-0.95	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		0.045	0.055	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.055	0.070	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.073	0.090	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -1\text{ A}$		6		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1\text{ A}, V_{GS} = 0\text{ V}$		-0.73	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		14	21	nC
Gate-Source Charge	Q_{gs}		1.7			
Gate-Drain Charge	Q_{gd}		2.5			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 6\text{ }\Omega$ $I_D \equiv -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$		16	25	ns
Rise Time	t_r		32	50		
Turn-Off Delay Time	$t_{d(off)}$		120	180		
Fall Time	t_f		80	120		
Source-Drain Reverse Recovery Time	t_{rr}		$I_F = -1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		46	

Notes:

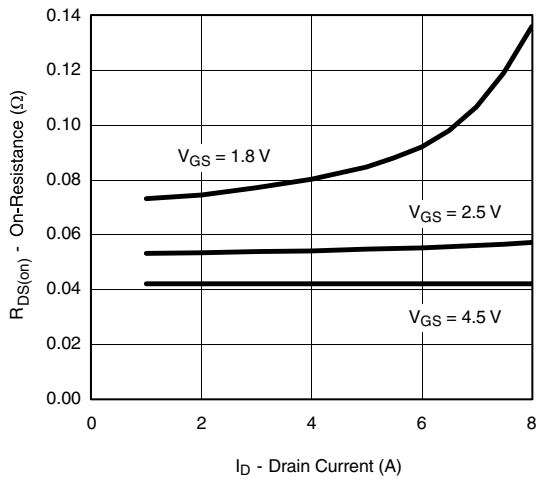
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

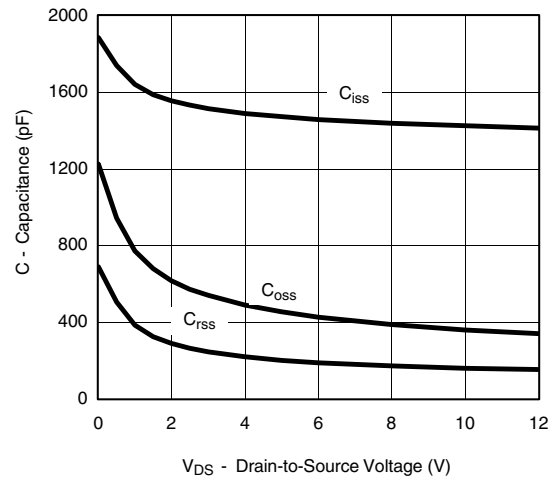
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



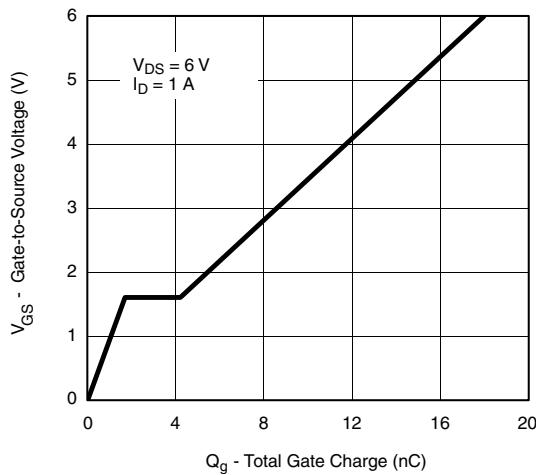
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



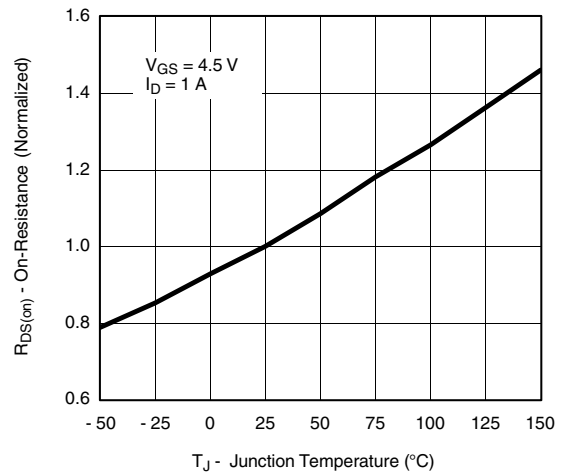
On-Resistance vs. Drain Current



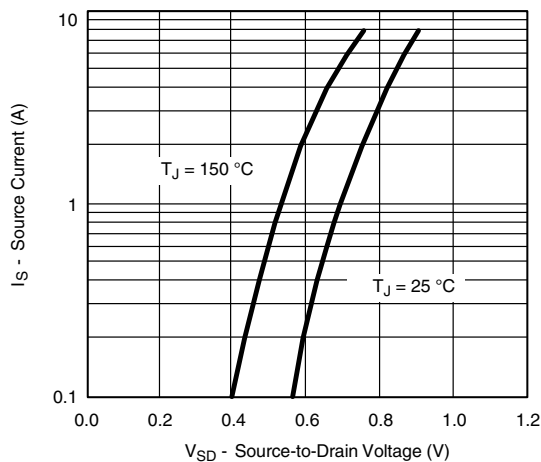
Capacitance



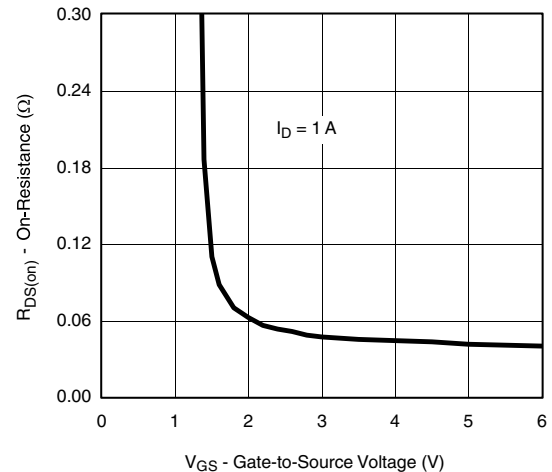
Gate Charge



On-Resistance vs. Junction Temperature

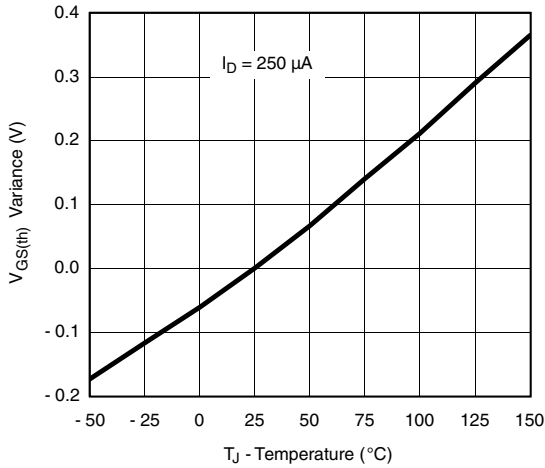


Source-Drain Diode Forward Voltage

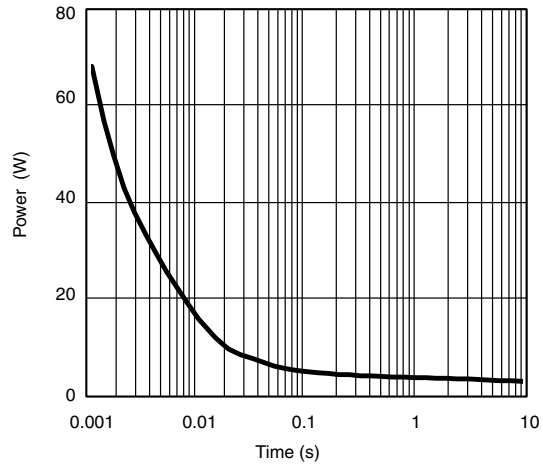


On-Resistance vs. Gate-to-Source Voltage

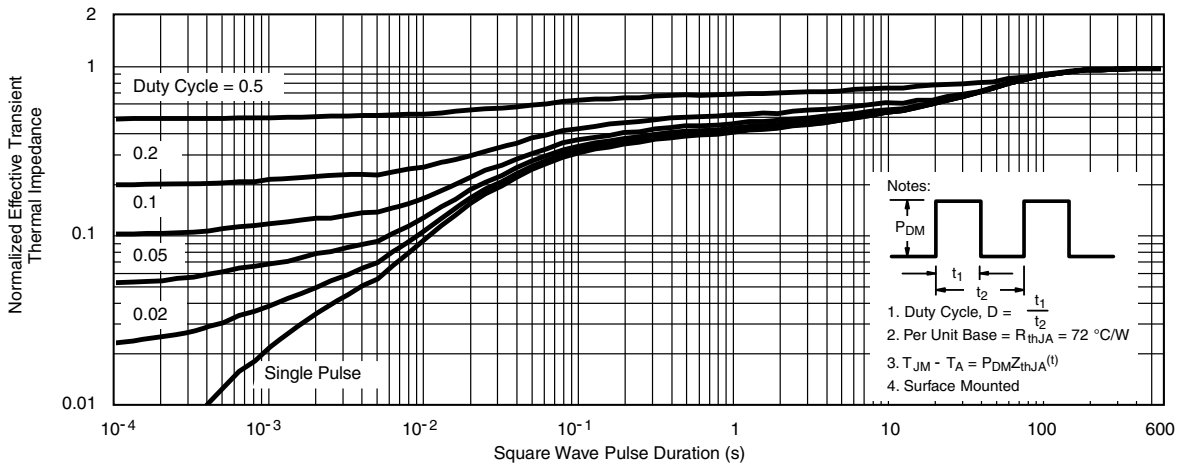
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



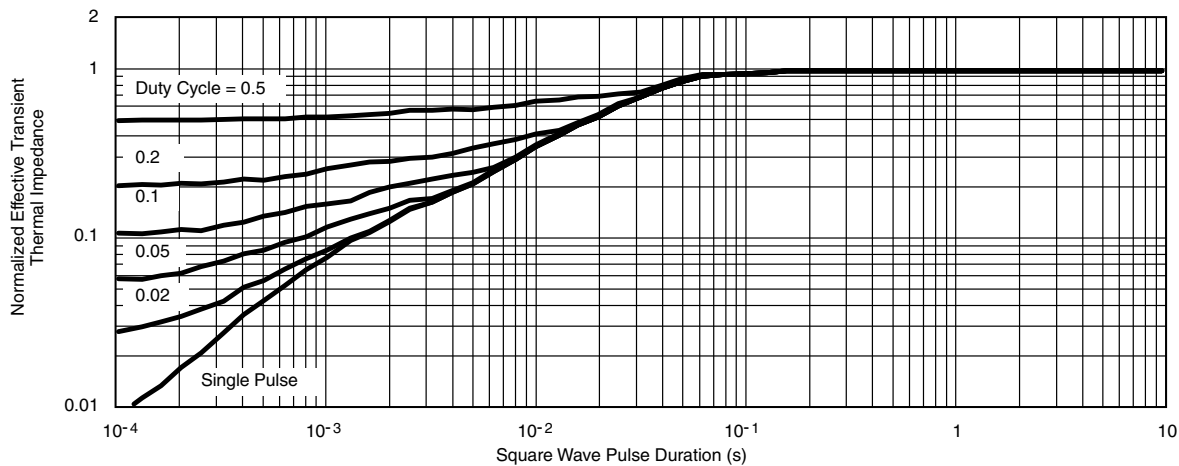
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



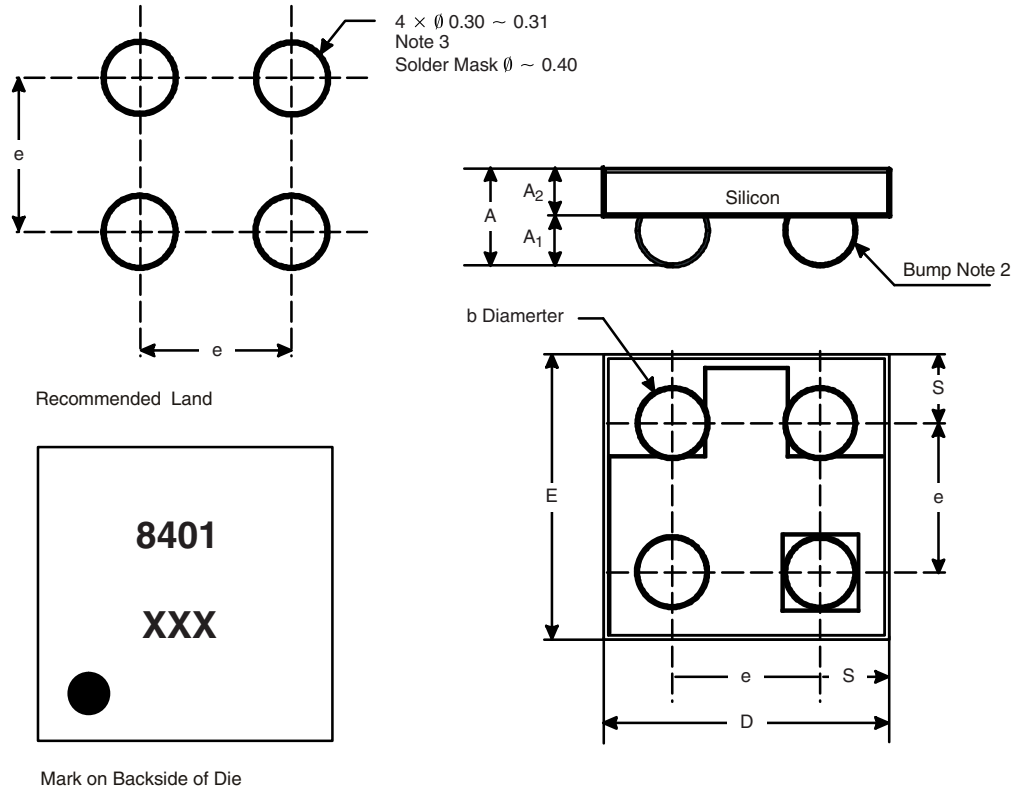
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (0.8 mm PITCH)



- Notes (unless otherwise specified):
1. Laser mark on the silicon die back, coated with a thin metal.
 2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
 3. Non-solder mask defined copper landing pad.
 4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.0102	0.0114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.800		0.0315	
S	0.360	0.400	0.0142	0.0157

- Notes:
- a. Use millimeters as the primary measurement.

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