MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™FD Power-Transistor, 200 V

IPP120N20NFD

Data Sheet

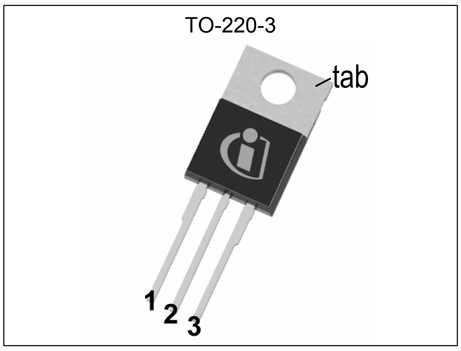
Rev. 2.0
Final

Power Management & Multimarket

1 Description

Features

- N-channel, normal level
- Fast Diode (FD) with reduced Q_{rr}
- Optimized for hard commutation ruggedness
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC [1] for target application
- Halogen-free according to IEC61249-2-21



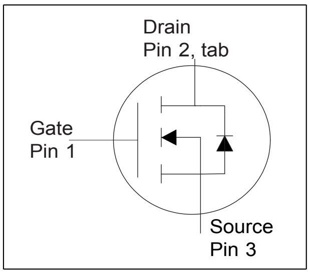


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	200	V
$R_{DS(on),max}$	12	mΩ
I_D	84	A

Type / Ordering Code	Package	Marking	Related Links
IPP120N20NFD	PG-TO220-3	120N20NF	-

[1] J-STD20 and JESD22

Table of Contents

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

at 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	84 60	A	T_C=25 °C T_C=100 °C
Pulsed drain current [1]	$I_{D,pulse}$	-	-	336	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	375	mJ	I_D=67 A, R_{GS}=25 Ω
Reverse diode peak d*v*/d*t*	d*v*/d*t*	-	-	60	kV/µs	I_D=160 A, V_{DS}=100 V, d*i*/d*t*=1500 A/µs, $T_{j,max}$=175 °C
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.3	0.5	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [2]	R_{thJA}	-	-	40	K/W	-

[1] See figure 3

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS}, I_D=270 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=160 V, V_{GS}=0 V, T_j=25 °C V_{DS}=160 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	10.6	12	mΩ	V_{GS}=10 V, I_D=84 A
Gate resistance	R_G	-	2.4	3.6	Ω	-
Transconductance	g_{fs}	70	139	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=84 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5000	6650	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance	C_{oss}	-	400	532	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	6	13	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=42 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	10	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=42 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	24	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=42 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	8	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=42 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	25	-	nC	V_{DD}=100 V, I_D=84 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	8	-	nC	V_{DD}=100 V, I_D=84 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	17	-	nC	V_{DD}=100 V, I_D=84 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	65	87	nC	V_{DD}=100 V, I_D=84 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	V_{DD}=100 V, I_D=84 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	162	-	nC	V_{DD}=100 V, V_{GS}=0 V

[1)] See "Gate charge waveforms" for parameter definition

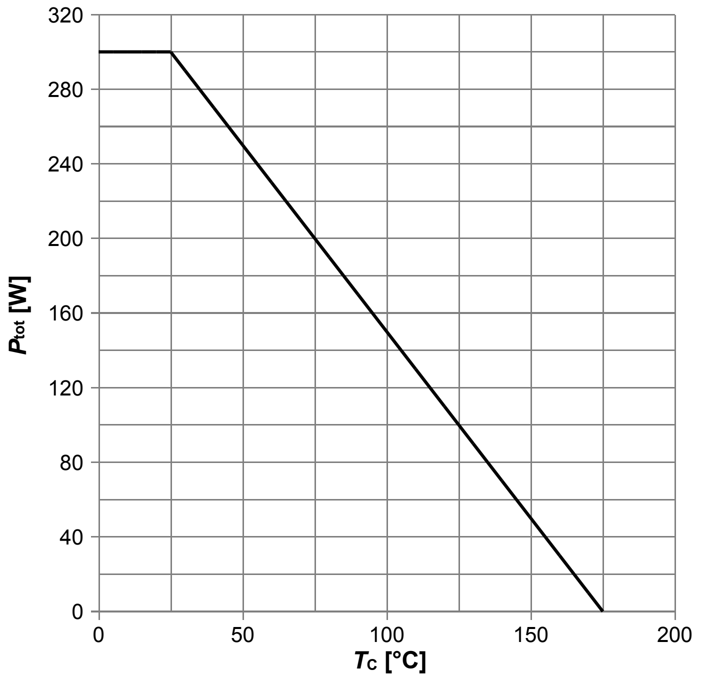
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	84	A	T_C=25 °C
Diode pulse current [1]	$I_{S,pulse}$	-	-	336	A	T_C=25 °C
Diode hard commutation current [2]	$I_{S,hard}$	-	-	160	A	T_C=25 °C, di_F/dt=1500 A/µs
Diode forward voltage	V_{SD}	-	1	1.2	V	V_{GS}=0 V, I_F=84 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	144	288	ns	V_R=100 V, I_F= 56 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	629	-	nC	V_R=100 V, I_F= 56 A, di_F/dt=100 A/µs

[1] Diode pulse current is defined by thermal and/or package limits
[2] Maximum allowed hard-commutated current through diode at di/dt=1500 A/µs

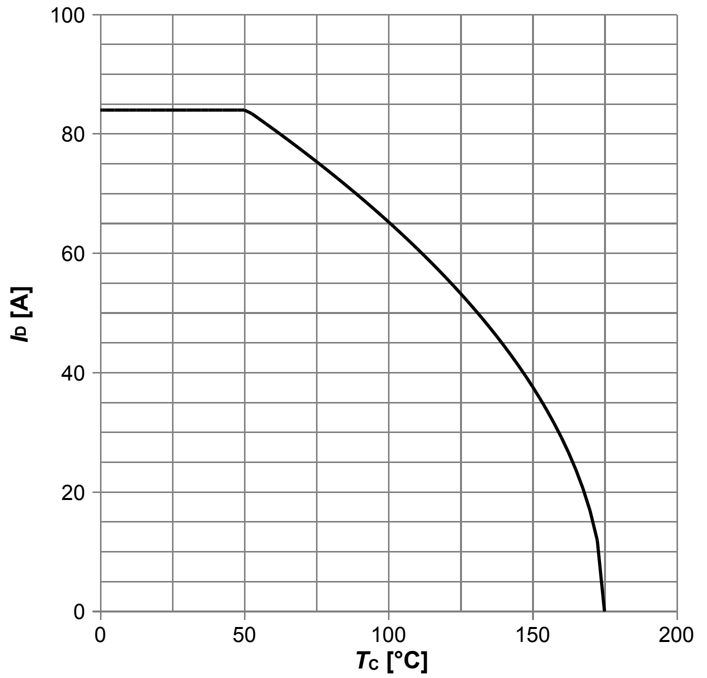
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



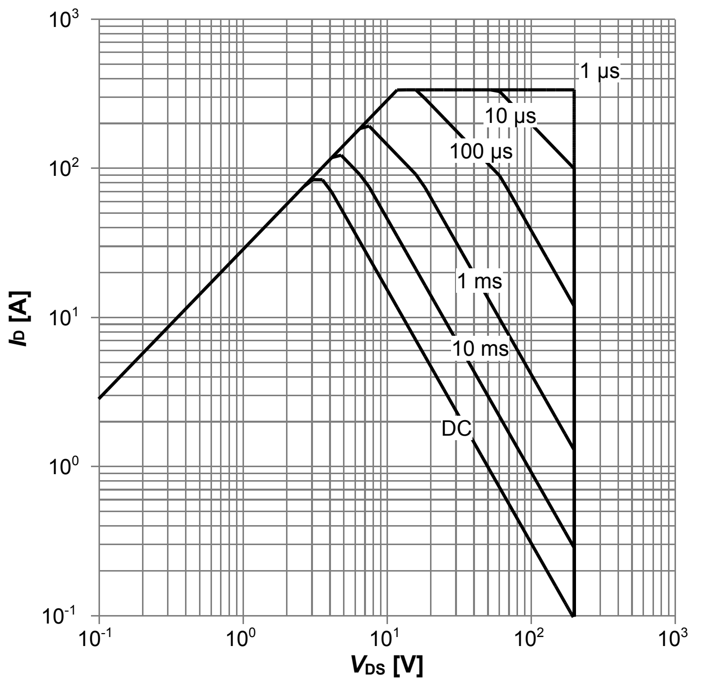
P_{tot}=f(T_C)

Diagram 2: Drain current



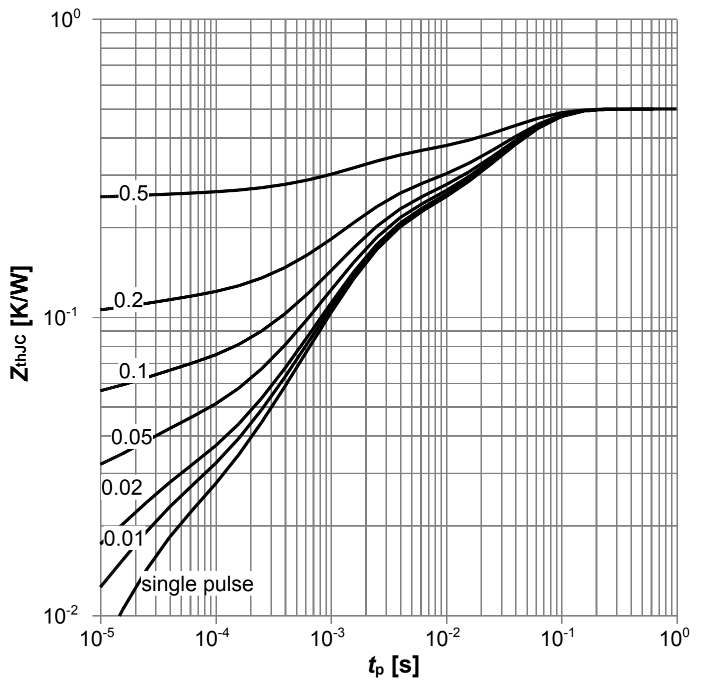
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



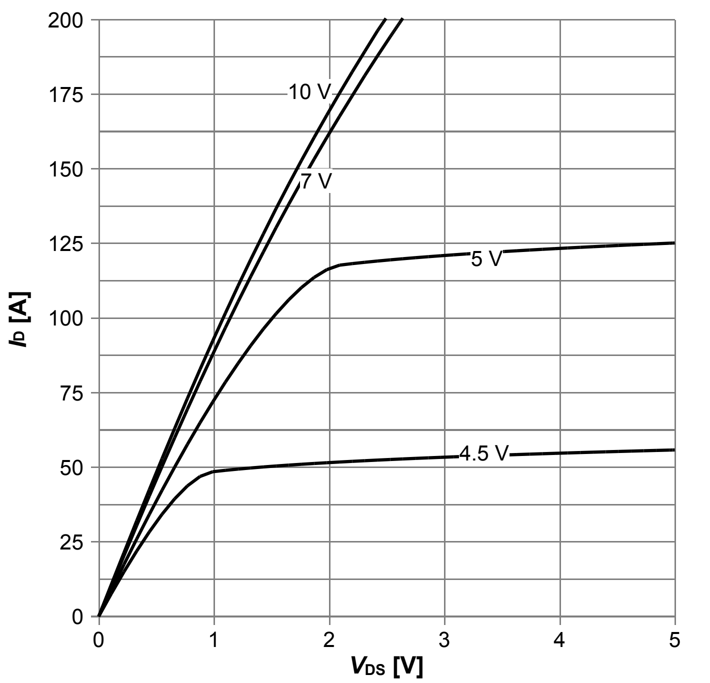
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



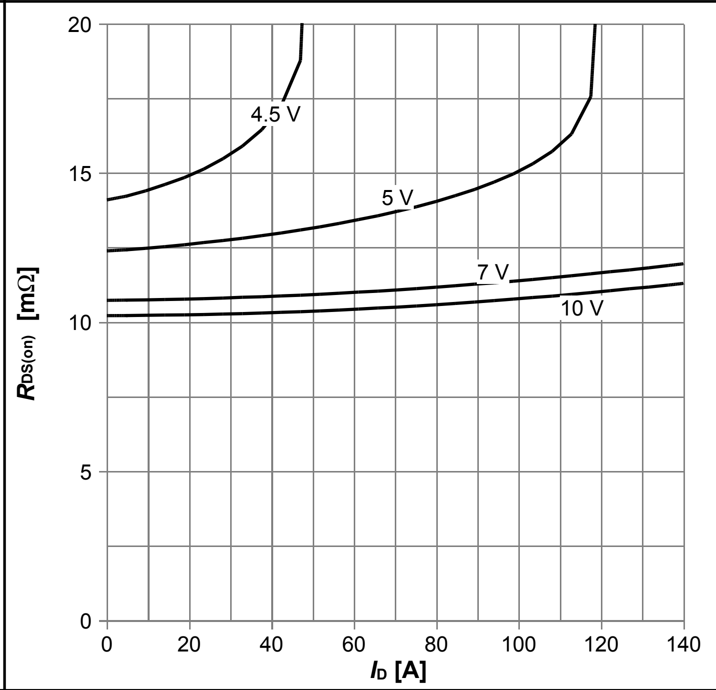
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



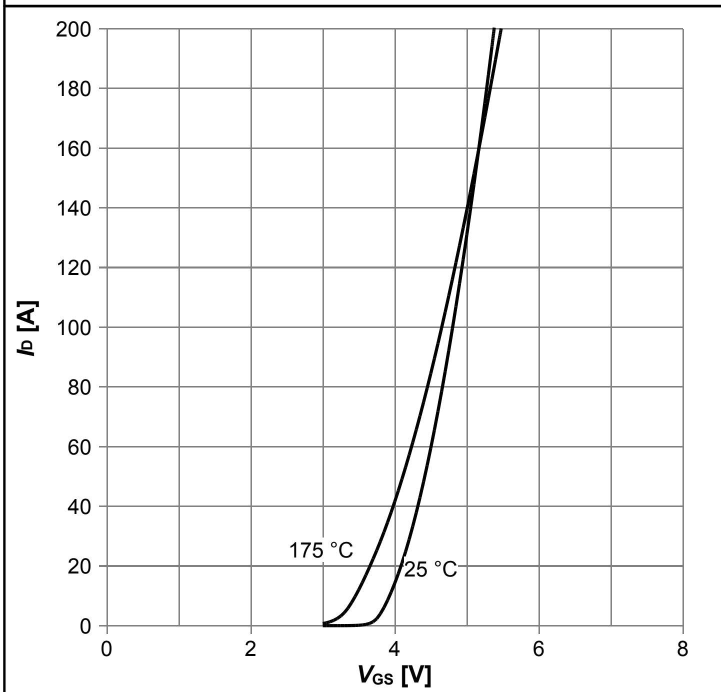
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



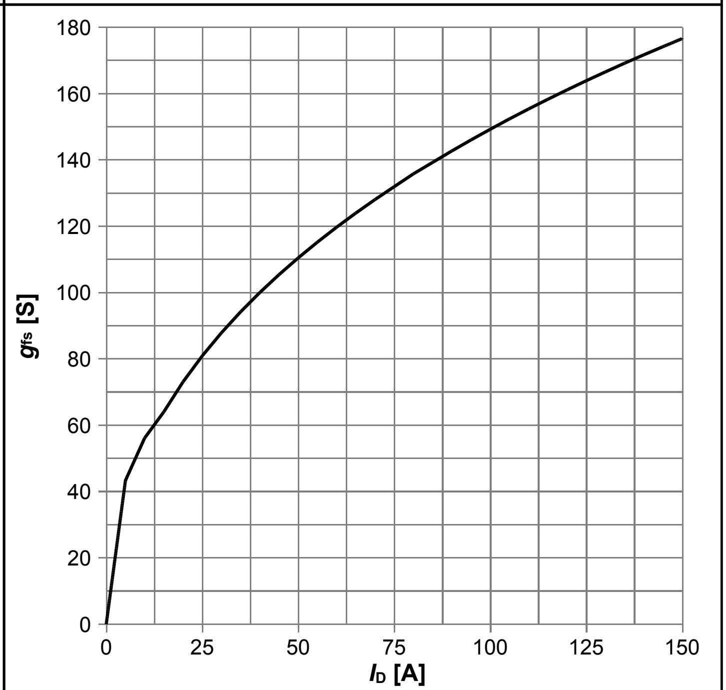
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



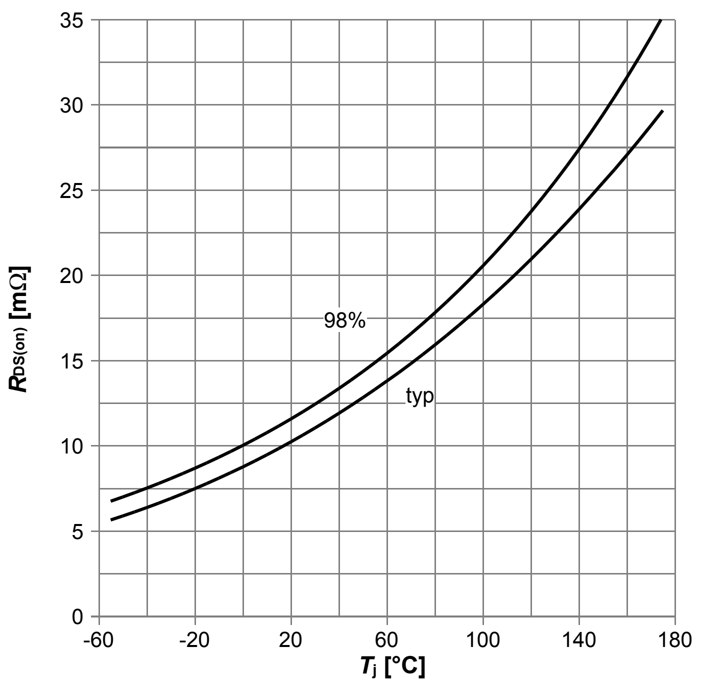
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



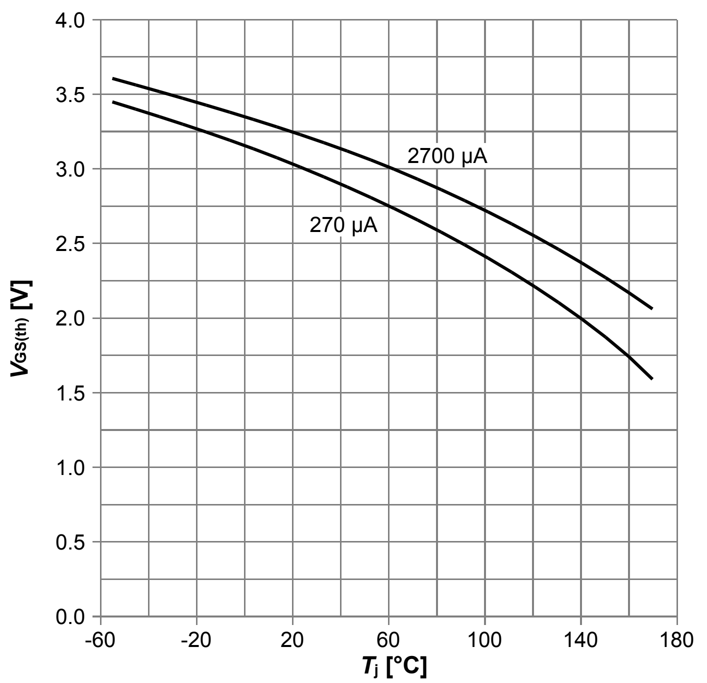
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



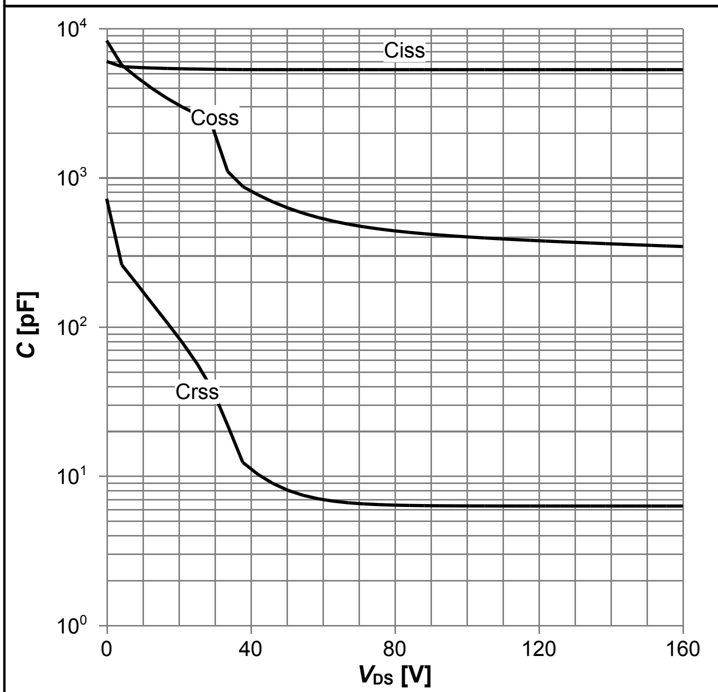
$R_{DS(on)}$=f(T_j); I_D=84 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



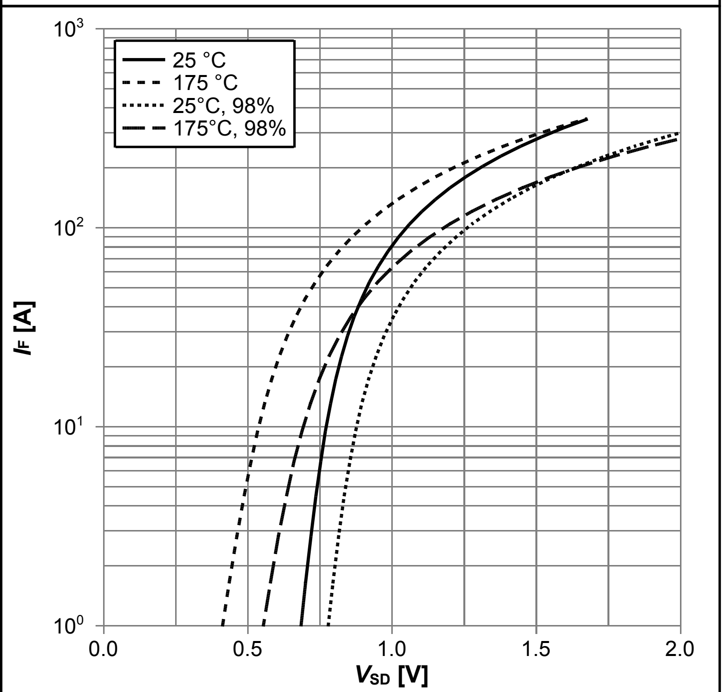
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



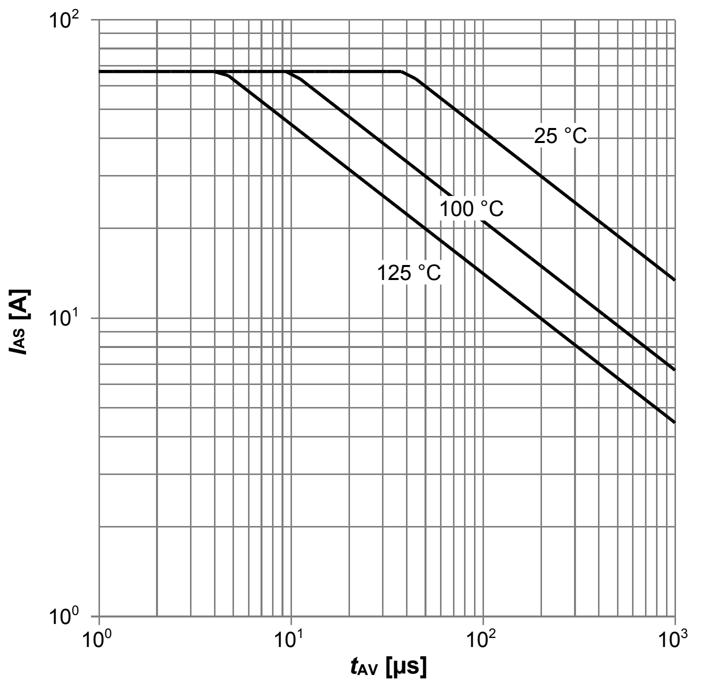
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



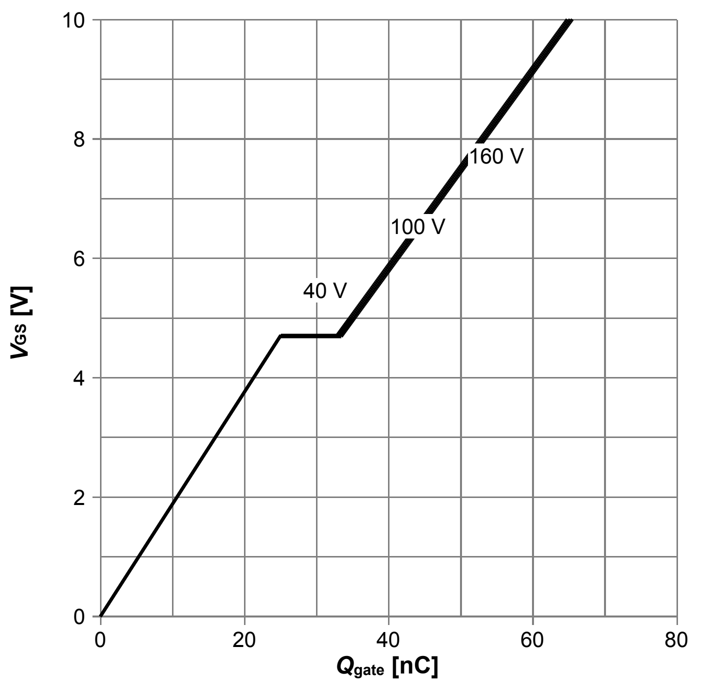
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



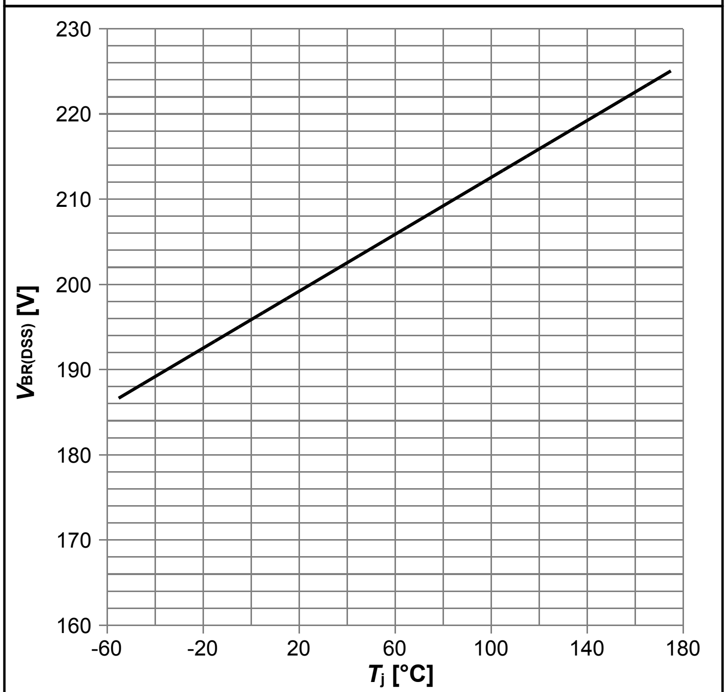
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



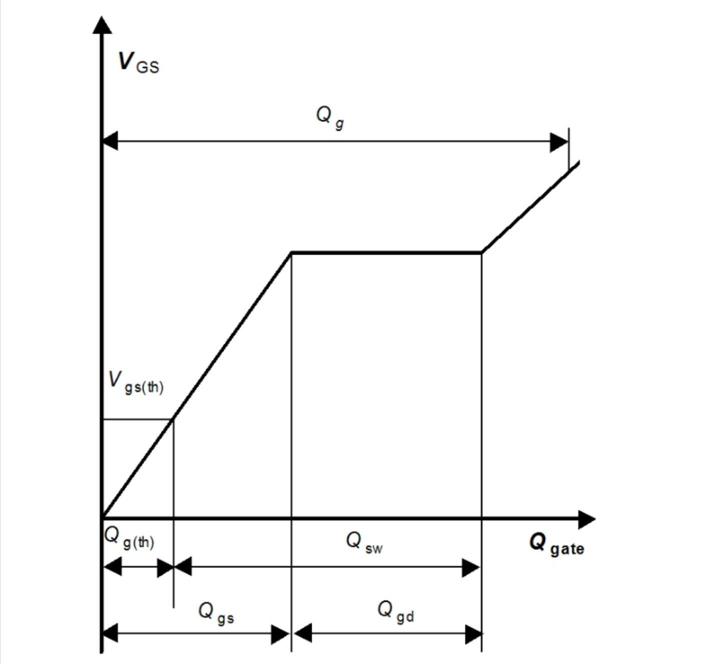
V_{GS}=f(Q_{gate}); I_D=84 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

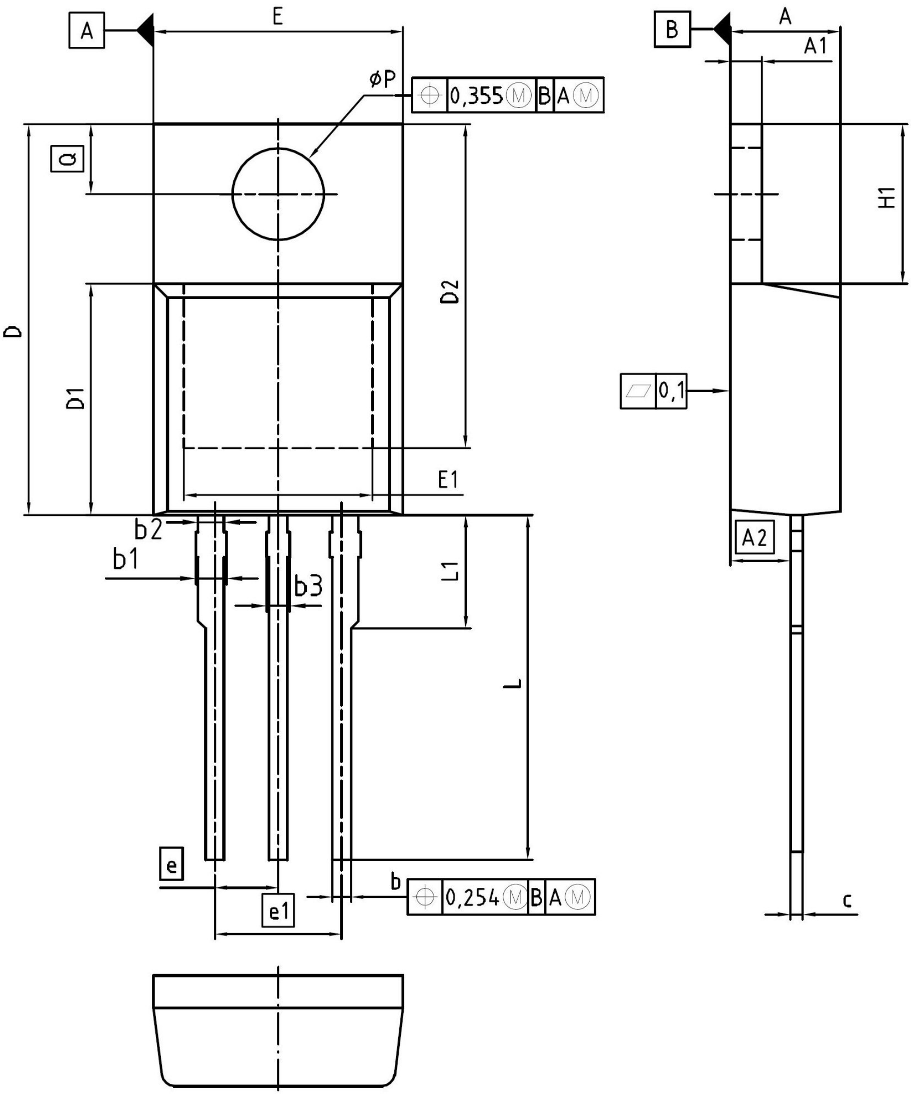


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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REVISION 06

Figure 1 Outline PG-TO220-3, dimensions in mm/inches

Revision History

IPP120N20NFD

Revision: 2014-02-06, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2014-02-06	Release of final version

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