Precision Analog Controller

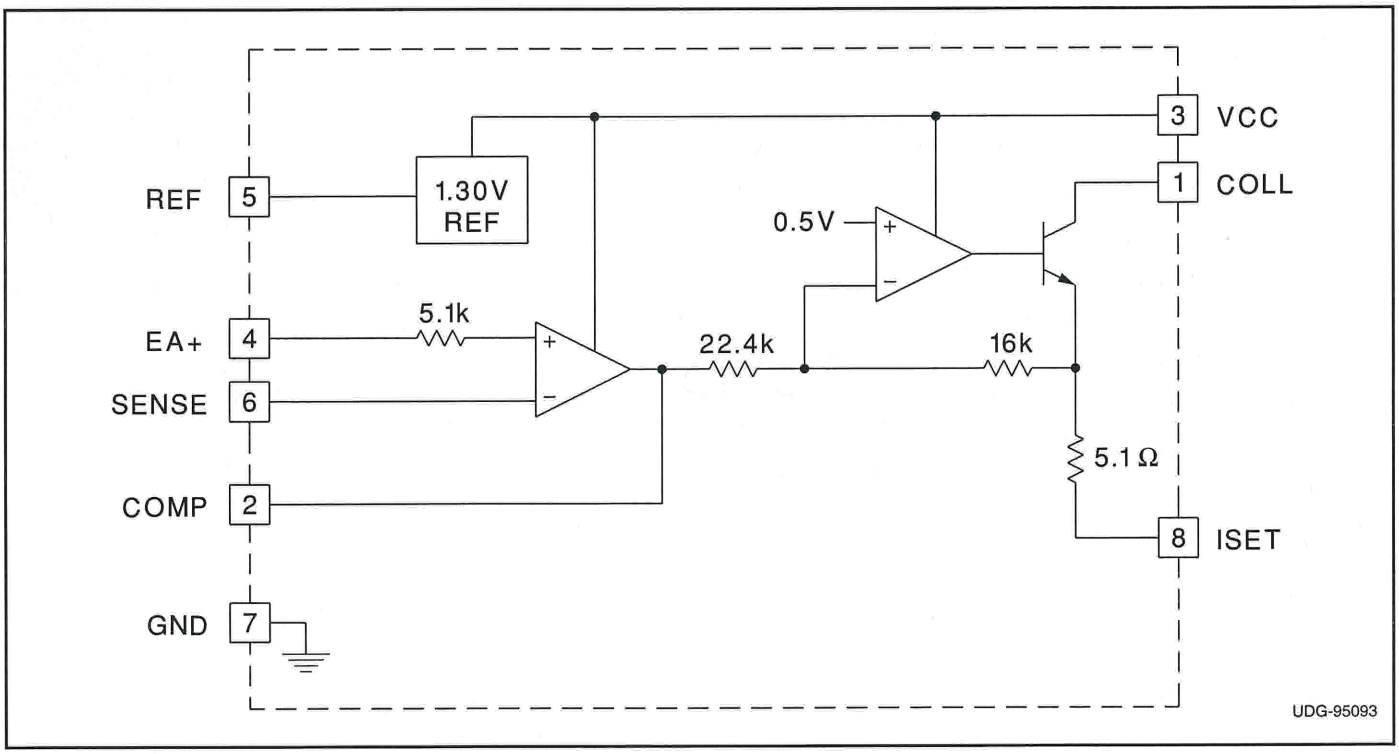
FEATURES

- Programmable Transconductance for Optimum Current Drive
- Accessible 1.3V Precision Reference
- Both Error Amplifier Inputs Available
- 0.7% Overall Reference Tolerance
- 0.4% Initial Accuracy
- 2.2V to 24.0V Operating Supply Voltage and User Programmable Reference
- Reference Accuracy Maintained for Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Low Quiescent Current (0.50mA Typ)

DESCRIPTION

The UC39432 is an adjustable precision analog controller with 100mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration. A sister device, the UC39431 adjustable shunt regulator, has an on-board resistor network providing six preprogrammed voltage levels, as well as external programming capability.

BLOCK DIAGRAM



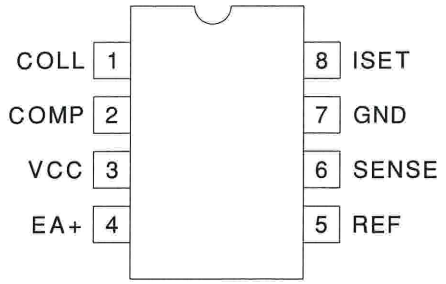
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: VCC 24V
Regulated Output: V_{COLL} 24V
EA Input: SENSE, EA+ 6V
EA Compensation: COMP 6V
Reference Output: REF 6V
Output Sink Current: I_{COLL} 140mA
Output Source Current: ISET . . . . . –140mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C and COLL Output = 2.4V to 24.0V for the UC19432, T_A = –25°C to +85°C and COLL Output = 2.3V to 24.0V for the UC29432, and T_A = 0°C to +70°C and COLL Output = 2.3V to 24.0V for the UC39432, VCC = 15V, I_{COLL} = 10mA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	T_A = 25°C	19432*	1.295	1.3	1.305	V
		39432B	1.29	1.3	1.31	V
Reference Temperature Tolerance	V_{COLL} = 5.0V	19432*	1.291	1.3	1.309	V
		39432B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.4V to 24.0V, V_{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Load Regulation	I_{COLL} = 10mA to 50mA, V_{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Sink Current					10	µA
Reference Source Current					–10	µA
EA Input Bias Current			–0.5	–0.2		µA
EA Input Offset Voltage		19432*			4.0	mV
		39432B			4.0	mV
EA+ Operational Voltage Limitations	(Note 1)		0.9		1.6	V
EA Output Current Sink (Internally Limited)					16	µA
EA Output Current Source					–1	mA
Minimum Operating Current	VCC = 24.0V, V_{COLL} = 5V			0.50	0.80	mA
Collector Current Limit (Note)	V_{COLL} = VCC = 24.0V, Ref = 1.35V ISET = GND			130	145	mA
Collector Saturation	I_{COLL} = 20mA		0.7	1.1	1.5	V
Transconductance (gm) (Note)	VCC = 2.4V to 24.0V, V_{COL} = 3V, I_{COLL} = 20mA ISET = GND	19432*	–170	–140	–110	mS
		39432B	–180	–140	–100	mS
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

** Also applies to the UC29432 and UC39432*
Note: *Programmed transconductance and collector current limit equations are specified in the ISET pin description.*
Note 1: *Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 24V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm • R_L, where gm is designed to be –140mS ±30mS and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

EA+: The non-inverting input to the error amplifier.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

ISET: The current set pin for the transconductance amplifier. The transconductance will be –140mS as specified in the electrical table if this pin is grounded. If a resistance R_L is added to the ISET pin, the resulting new transconductance is calculated using the following equation: gm = –0.714V • (5.1Ω + R_L). The maximum current will be approximately

$$I_{MAX} = \frac{0.6V}{5.1\Omega + R_L}$$

REF: The output of the trimmed precision reference. It can source or sink 10μA and still maintain the 1% temperature specification.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the UC39431 shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 24.0V. The quiescent current is typically 0.50mA.

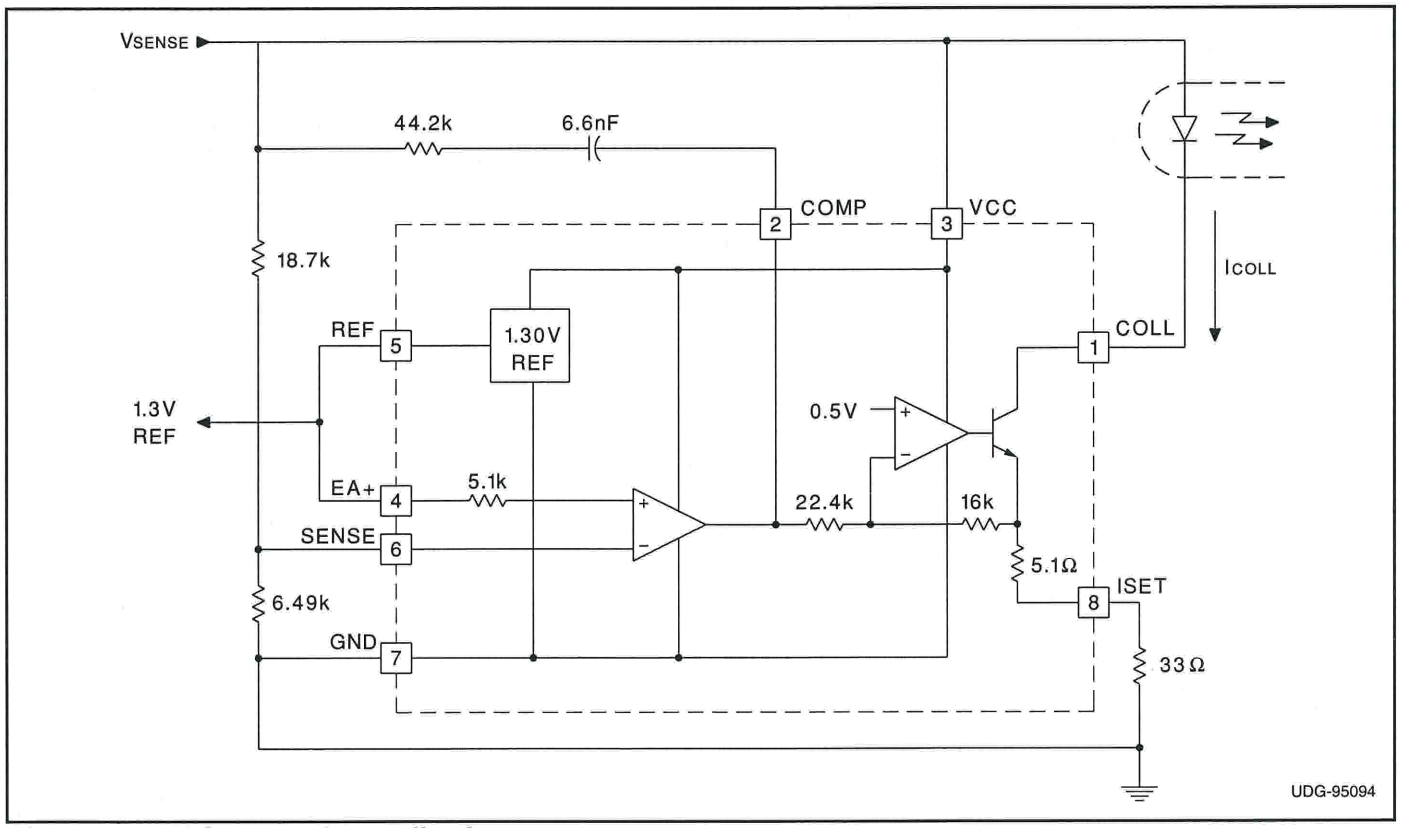


Figure 1. 5.0V Optocoupler application.

OVERVOLTAGE COMPARATOR APPLICATION

The signal V_{IN} senses the input voltage. As long as the input voltage is less than 5.5V, the output is equal to the voltage on V_{IN}. During this region of operation, the diode is reversed biased which keeps the EA+ pin at 1.3V. When V_{IN} exceeds the over voltage threshold of 5.5V, the output is driven low. This forward biases the diode and creates hysteresis by changing the threshold to 4.5V.

OPTOCOUPLER APPLICATION

The optocoupler application shown takes advantage of the accessible pins REF and ISET. The ISET pin has a 33 ohm resistor to ground that protects the opto-coupler by limiting the current to about 16mA. This also lowers the transconductance to approximately 19mS. The ability to adjust the transconductance gives the designer further control of the loop gain. The REF pin is available to satisfy any high precision voltage requirements.

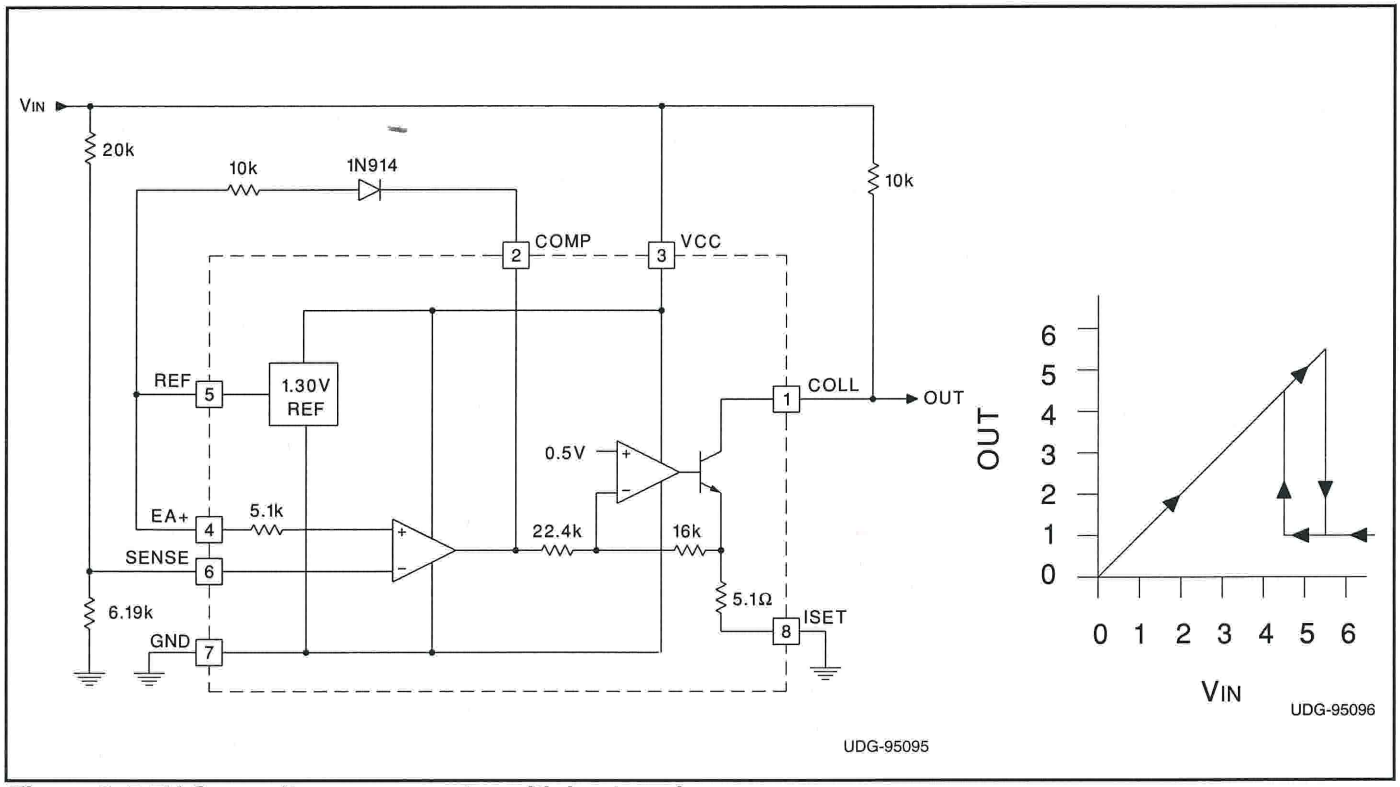


Figure 2. 5.5V Overvoltage comparator with hysteresis.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC19432J	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UC19432J883B	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UC29432D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC29432DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC29432DTR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC29432DTRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC29432N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC29432NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC39432BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39432BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39432BDTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39432BDTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39432BN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC39432BNG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC39432D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39432DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC39432N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC39432NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

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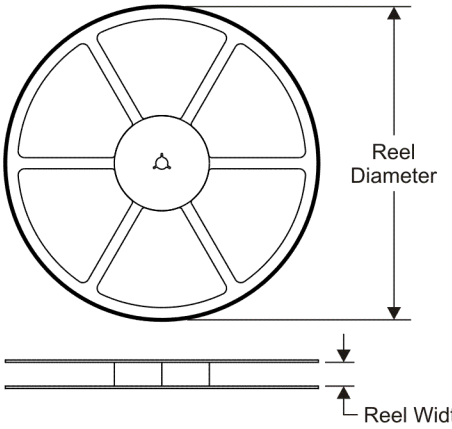
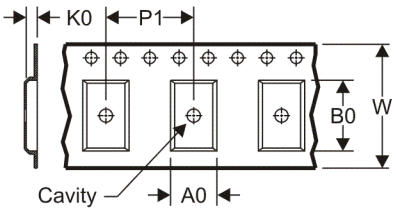
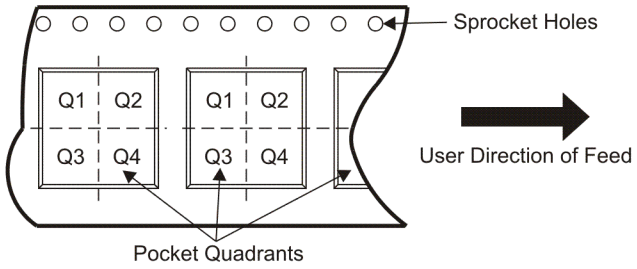


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

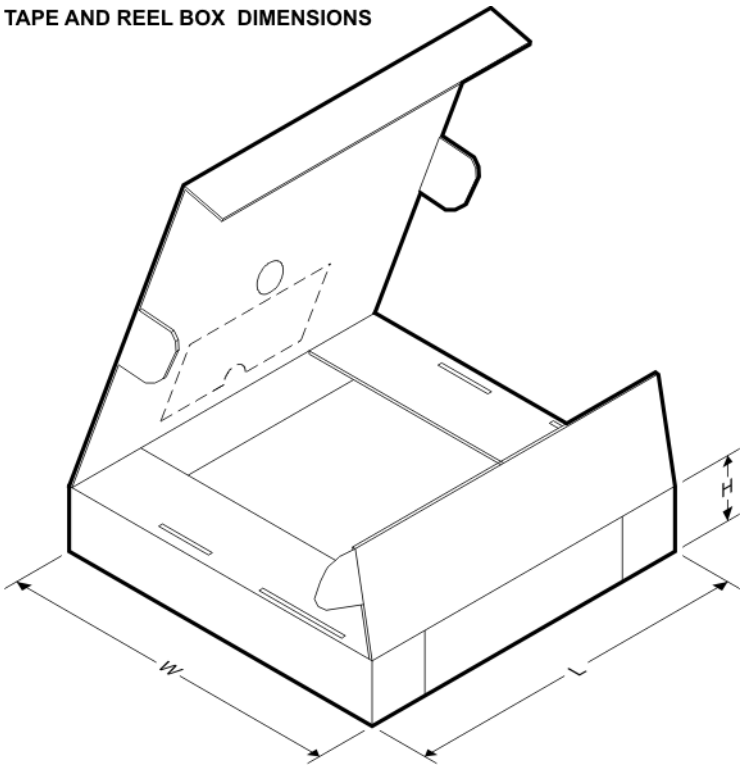
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC29432DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC39432BDTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC29432DTR	SOIC	D	8	2500	346.0	346.0	29.0
UC39432BDTR	SOIC	D	8	2500	346.0	346.0	29.0

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