19-3789; Rev 0; 8/05

# +3.3V/+5V, 8-Channel Relay Drivers with Fast Recovery Time and Power-Save Mode



## General Description

The MAX4822–MAX4825 8-channel relay drivers offer built-in kickback protection and drive +3V/+5V non-latching or dual-coil-latching relays. Each independent open-drain output features a 2.7Ω (typ) on-resistance and is guaranteed to sink 70mA (min) of load current. These devices consume less than 300µA (max) quiescent current and have 1µA output off-leakage current. A Zener-kickback-protection circuit significantly reduces recovery time in applications where switching speed is critical.

The MAX4822/MAX4824 feature a unique power-save mode where the relay current, after activation, can be reduced to a level just above the relay hold-current threshold. This mode keeps the relay activated while significantly reducing the power consumption.

The MAX4822/MAX4823 feature a 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. Input data is shifted into a shift register and latched to the outputs when $\overline{CS}$ transitions from low to high. Each data bit in the shift register corresponds to a specific output, allowing independent control of all outputs.

The MAX4824/MAX4825 feature a 4-bit parallel-input interface. The first 3 bits (A0, A1, A2) determine the output address, and the fourth bit (LVL) determines whether the selected output is switched on or off. Data is latched to the outputs when $\overline{CS}$ transitions from low to high.

The MAX4822–MAX4825 feature separate set and reset functions, allowing turn-on or turn-off of all outputs simultaneously with a single control line. Built-in hysteresis (Schmidt trigger) on all digital inputs allows these devices to be used with slow-rising and falling signals, such as those from optocouplers or RC power-up initialization circuits. The MAX4822–MAX4825 are available in space-saving 4mm x 4mm, 20-pin thin QFN packages. They are specified over the -40°C to +85°C extended temperature range.

## Applications

ATE Equipment

DSL Redundancy Protection (ADSL/VDSL/HDSL)

T1/E1 Redundancy Protection

T3/E3 Redundancy Protection

Industrial Equipment

Test Equipment (Oscilloscopes, Spectrum Analyzers)

*SPI is a trademark of Motorola, Inc.*
*QSPI is a trademark of Motorola, Inc.*
*MICROWIRE is a trademark of National Semiconductor Corp.*

## Features

- ♦ **Built-In Zener Kickback Protection for Fast Recovery**
- ♦ **Programmable Power-Save Mode Reduces Relay Power Consumption (MAX4822/MAX4824)**
- ♦ **10MHz SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- ♦ **Eight Independent Output Channels**
- ♦ **Drive +3V and +5V Relays**
- ♦ **Guaranteed 70mA (min) Coil Drive Current**
- ♦ **Guaranteed 5Ω (max) $R_{ON}$**
- ♦ **$\overline{SET}$ / $\overline{RESET}$ Functions to Turn On/Off All Outputs Simultaneously**
- ♦ **Serial Digital Output for Daisy Chaining**
- ♦ **Optional Parallel Interface (MAX4824/MAX4825)**
- ♦ **Low 300µA (max) Quiescent Supply Current**
- ♦ **Space-Saving, 4mm x 4mm, 20-Pin TQFN Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PACKAGE CODE |
|---|---|---|---|
| **MAX4822**ETP | -40°C to +85°C | 20 TQFN-EP* | T2044-3 |
| **MAX4823**ETP | -40°C to +85°C | 20 TQFN-EP* | T2044-3 |
| **MAX4824**ETP | -40°C to +85°C | 20 TQFN-EP* | T2044-3 |
| **MAX4825**ETP | -40°C to +85°C | 20 TQFN-EP* | T2044-3 |

**For maximum heat dissipation, packages have an exposed pad (EP) on the bottom. Solder exposed pad to GND.*

## Selector Guide

| PART | INTERFACE | POWER SAVE |
|---|---|---|
| MAX4822 | Serial | Yes |
| MAX4823 | Serial | No |
| MAX4824 | Parallel | Yes |
| MAX4825 | Parallel | No |

***Pin Configurations appear at end of data sheet.***

# +3.3V/+5V, 8-Channel Relay Drivers with Fast Recovery Time and Power-Save Mode

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ ....................-0.3V to +6.0V
OUT_ ....................-0.3V to +11V
$\overline{CS}$, SCLK, DIN, $\overline{SET}$, $\overline{RESET}$, A0, A1, A2, LVL......-0.3V to +6.0V
DOUT....................-0.3V to ($V_{CC}$ + 0.3V)
PSAVE ....................-0.3V to ($V_{CC}$ + 0.3V)
Continuous OUT_ Current (all outputs turned on) ............150mA
Continuous OUT_ Current (single output turned on) ........300mA
Continuous Power Dissipation ($T_A$ = +70°C)
20-Lead Thin QFN (derate 16.9mW/°C above +70°C) ..1350mW
Operating Temperature Range ....................-40°C to +85°C
Junction Temperature ....................+150°C
Storage Temperature Range ....................-65°C to +150°C
Soldering Temperature (10s) ....................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 2.7V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{CC}$ | | | 2.3 | | 5.5 | V |
| Quiescent Current | $I_{CC}$ | $I_{OUT\_}$ = 0, logic inputs = 0 or $V_{CC}$ | $V_{CC}$ = 3.6V | | 160 | 300 | µA |
| | | | $V_{CC}$ = 5.5V | | 180 | 300 | |
| Dynamic Supply Current | $I_D$ | $f_{SCLK}$ =10MHz, $C_{DOUT}$ = 50pF | $V_{CC}$ = 3.6V | | 1.2 | | mA |
| | | | $V_{CC}$ = 5.5V | | 1.6 | | |
| Thermal Shutdown | | Power-save disable threshold (Note 2) | | | +130 | | °C |
| | | Output disable threshold (Note 3) | | | +150 | | |
| Power-On Reset | | Transform from high voltage to low voltage | | 0.6 | 1.2 | 2.0 | V |
| Power-On Reset Hysteresis | | | | | 140 | | mV |
| **DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, LVL, A0, A1, A2, $\overline{RESET}$, $\overline{SET}$)** | | | | | | | |
| Input Logic-High Voltage | $V_{IH}$ | $V_{CC}$ = 2.7V to 3.6V | | 2.0 | | | V |
| | | $V_{CC}$ = 4.2V to 5.5V | | 2.4 | | | |
| Input Logic-Low Voltage | $V_{IL}$ | $V_{CC}$ = 2.7V to 3.6V | | | | 0.6 | V |
| | | $V_{CC}$ = 4.2V to 5.5V | | | | 0.8 | |
| Input Logic Hysteresis | $V_{HYST}$ | | | | 150 | | mV |
| Input Leakage Current | $I_{LEAK}$ | Input voltages = 0 or 5.5V | | -1.0 | +0.01 | +1.0 | µA |
| Input Capacitance | $C_{IN}$ | | | | 5 | | pF |
| **DIGITAL OUTPUT (DOUT)** | | | | | | | |
| DOUT Low Voltage | $V_{OL}$ | $I_{SINK}$ = 6mA | | | | 0.4 | V |
| DOUT High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 0.5mA | | $V_{CC}$ - 0.5 | | | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 2.7V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **RELAY OUTPUT DRIVERS (OUT1–OUT8)** | | | | | | | |
| OUT_ Drive Voltage, Power-Save On (MAX4822) | $V_{OUTPS\_}$ | $V_{CC}$ = 2.7V (Note 4) | PS = 001 | 0.65 x $V_{CC}$ | 0.7 x $V_{CC}$ | 0.75 x $V_{CC}$ | V |
| | | | PS = 010 | 0.55 x $V_{CC}$ | 0.6 x $V_{CC}$ | 0.65 x $V_{CC}$ | |
| | | | PS = 011 | 0.45 x $V_{CC}$ | 0.5 x $V_{CC}$ | 0.55 x $V_{CC}$ | |
| | | | PS = 100 | 0.35 x $V_{CC}$ | 0.4 x $V_{CC}$ | 0.45 x $V_{CC}$ | |
| | | | PS = 101 | 0.25 x $V_{CC}$ | 0.3 x $V_{CC}$ | 0.35 x $V_{CC}$ | |
| | | | PS = 110 | 0.15 x $V_{CC}$ | 0.2 x $V_{CC}$ | 0.25 x $V_{CC}$ | |
| | | | PS = 111 | 0.05 x $V_{CC}$ | 0.1 x $V_{CC}$ | 0.15 x $V_{CC}$ | |
| OUT_ Drive Voltage, Power-Save On (MAX4824) | $V_{OUTPS\_}$ | $V_{CC}$ = 2.7V (Note 4) | | 0.35 x $V_{CC}$ | 0.4 x $V_{CC}$ | 0.45 x $V_{CC}$ | V |
| OUT_ On-Resistance | $R_{ON}$ | $V_{CC}$ = 2.7V, $I_{OUT\_}$ = 70mA | | | 2.7 | 5.0 | Ω |
| OUT_ Off-Leakage Current | $I_{LEAK}$ | $V_{OUT\_}$ = $V_{CC}$, all outputs off | | -1 | | +1 | µA |
| Zener Clamping Voltage | $V_{CLAMP}$ | $I_{OUT\_}$ = 70mA (Note 5) | | 7.0 | 9 | 10.5 | V |
| **SPI TIMING (MAX4822/MAX4823)** | | | | | | | |
| Turn-On Time (OUT_) | $t_{ON}$ | From rising edge of $\overline{CS}$, $R_L$ = 50Ω, $C_L$ = 50pF | | | | 1.0 | µs |
| Turn-Off Time (OUT_) | $t_{OFF}$ | From rising edge of $\overline{CS}$, $R_L$ = 50Ω, $C_L$ = 50pF | | | | 3.0 | µs |
| SCLK Frequency | $f_{SCLK}$ | | | 0 | | 10 | MHz |
| Cycle Time | $t_{CH} + t_{CL}$ | | | 100 | | | ns |
| $\overline{CS}$ Fall-to-SCLK Rise Setup | $t_{CSS}$ | | | 50 | | | ns |
| $\overline{CS}$ Rise-to-SCLK Hold | $t_{CSH}$ | | | 50 | | | ns |
| SCLK High Time | $t_{CH}$ | | | 40 | | | ns |
| SCLK Low Time | $t_{CL}$ | | | 40 | | | ns |
| Data Setup Time | $t_{DS}$ | | | 20 | | | ns |

## ELECTRICAL CHARACTERISTICS (continued)

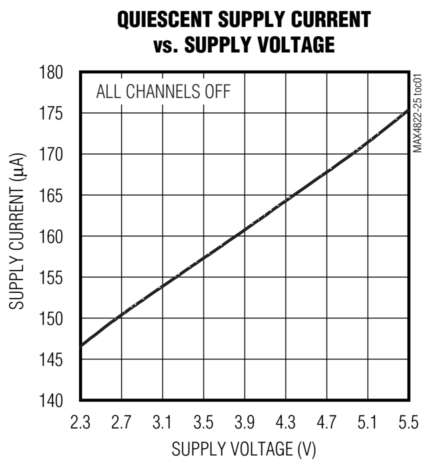
($V_{CC}$ = +2.7V to +5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 2.7V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

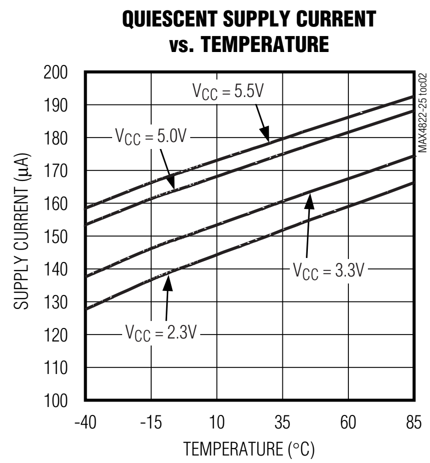
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Hold Time | $t_{DH}$ | | 0 | | | ns |
| SCLK Fall to DOUT Valid | $t_{DO}$ | 50% of SCLK to ($V_{IH}$, $V_{IL}$ of $D_{IN}$), $C_L$ = 50pF | | 17 | 28 | ns |
| Rise Time (DIN, SCLK, $\overline{CS}$, $\overline{SET}$, $\overline{RESET}$) | $t_{SCR}$ | 20% of $V_{CC}$ to 70% of $V_{CC}$, $C_L$ = 50pF (Note 6) | | | 2 | µs |
| Fall Time (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SET}$) | $t_{SCF}$ | 20% of $V_{CC}$ to 70% of $V_{CC}$, $C_L$ = 50pF (Note 6) | | | 2 | µs |
| $\overline{RESET}$ Minimum Pulse Width | $t_{RW}$ | | 70 | | | ns |
| $\overline{SET}$ Minimum Pulse Width | $t_{SW}$ | | 70 | | | ns |
| $\overline{CS}$ Minimum Pulse Width | $t_{CSW}$ | | 40 | | | ns |
| **PARALLEL TIMING (MAX4824/MAX4825)** | | | | | | |
| Turn-On Time | $t_{ON}$ | From rising edge of $\overline{CS}$, $R_L$ = 50Ω, $C_L$ = 50pF | | | 1 | µs |
| Turn-Off Time | $t_{OFF}$ | From rising edge of $\overline{CS}$, $R_L$ = 50Ω, $C_L$ = 50pF | | | 3 | µs |
| LVL Setup Time | $t_{LS}$ | | 20 | | | ns |
| LVL Hold Time | $t_{LH}$ | | 0 | | | ns |
| Address to $\overline{CS}$ Setup Time | $t_{AS}$ | | 20 | | | ns |
| Address to $\overline{CS}$ Hold Time | $t_{AH}$ | | 0 | | | ns |
| Rise Time (A2, A1, A0, LVL) | $t_{SCR}$ | 20% of $V_{CC}$ to 70% of $V_{CC}$, $C_L$ = 50pF (Note 6) | | | 2 | µs |
| Fall Time (A2, A1, A0, LVL) | $t_{SCF}$ | 20% of $V_{CC}$ to 70% of $V_{CC}$, $C_L$ = 50pF (Note 6) | | | 2 | µs |
| $\overline{RESET}$ Pulse Width | $t_{RW}$ | | 70 | | | ns |
| $\overline{SET}$ Pulse Width | $t_{SW}$ | | 70 | | | ns |
| $\overline{CS}$ Minimum Pulse Width | $t_{CSW}$ | | 40 | | | ns |
| **POWER-SAVE TIMING (MAX4822/MAX4824)** | | | | | | |
| Power-Save Delay Time | $t_{PS}$ | Variation from typical value, $C_L$ = 100nF (Note 7) | 1.6 | 3.2 | 5.4 | ms |
| Minimum PSAVE Low Time to Power-Save Reset | $t_{PSR}$ | | | 2 | 3.5 | ms |

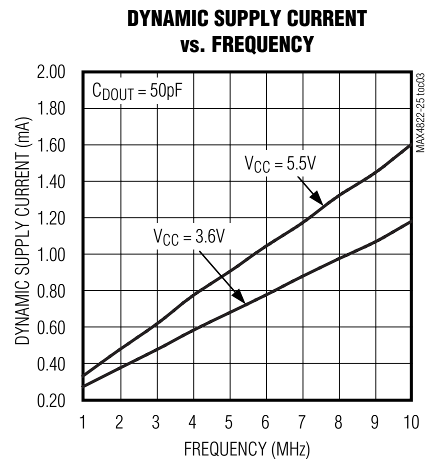
**Note 1:** Specifications at -40°C are guaranteed by design and not production tested.
**Note 2:** Thermal shutdown disables power save from all channels to reduce power dissipation inside the device.
**Note 3:** Thermal shutdown turns off all channels.
**Note 4:** The circuit can set the output voltage in power-save mode only if $I_{OUT} \times R_{ON} < V_{OUTP}$.
**Note 5:** After relay turn-off, inductive kickback can momentarily cause the OUT_ voltage to exceed $V_{CC}$. This is considered part of normal operation and does not damage the device.
**Note 6:** Guaranteed by design.
**Note 7:** For other capacitance values, use the equation $t_{PS} = 32 \times C$.

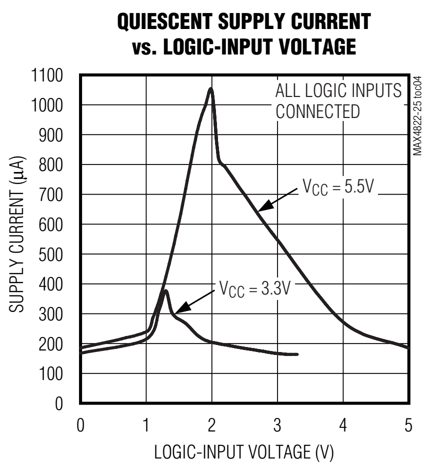
## Typical Operating Characteristics

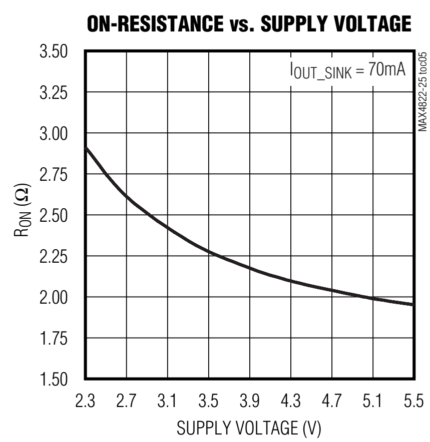
($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

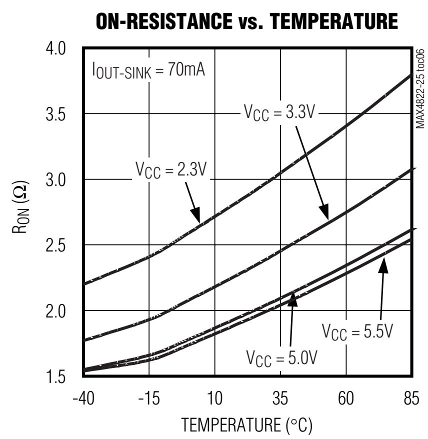


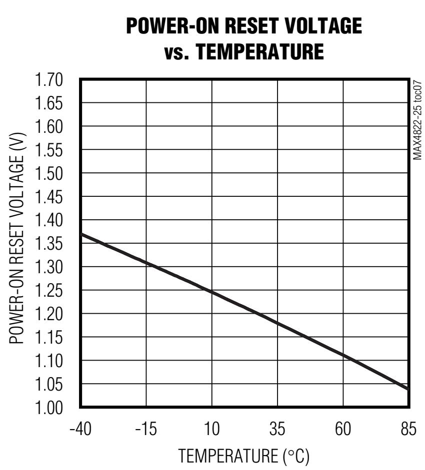



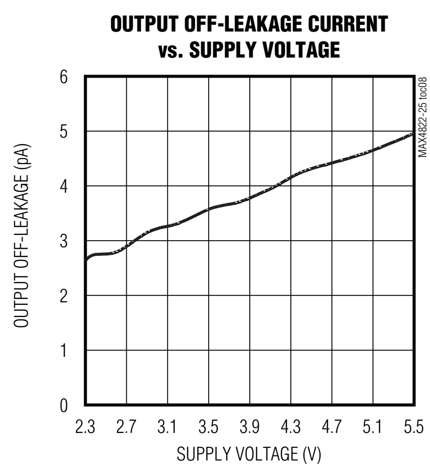



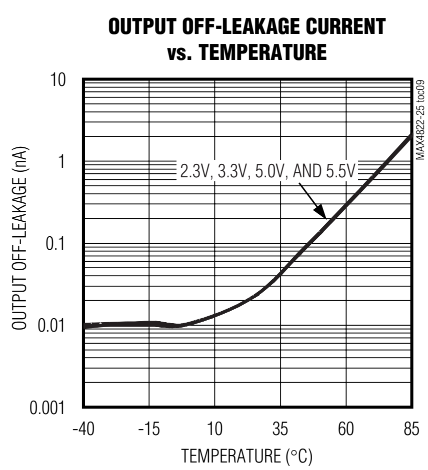



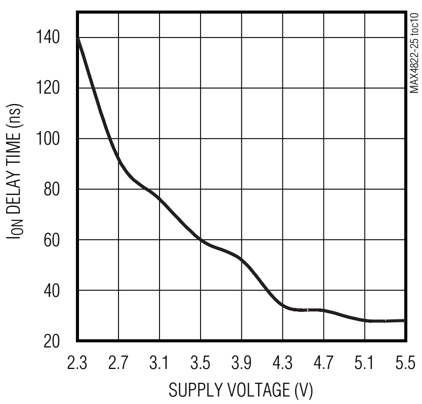



# +3.3V/+5V, 8-Channel Relay Drivers with Fast Recovery Time and Power-Save Mode

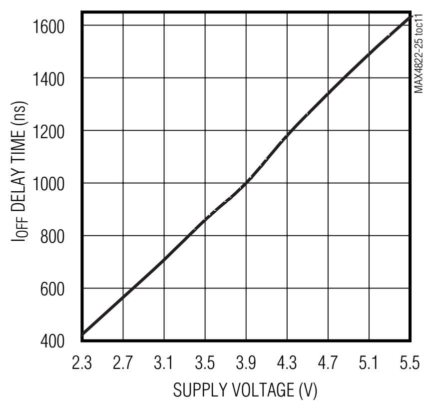
## Typical Operating Characteristics (continued)

($V_{CC}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

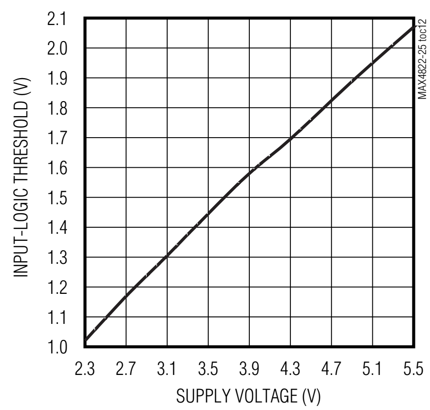
**OUT_ TURN-ON DELAY TIME vs. SUPPLY VOLTAGE**



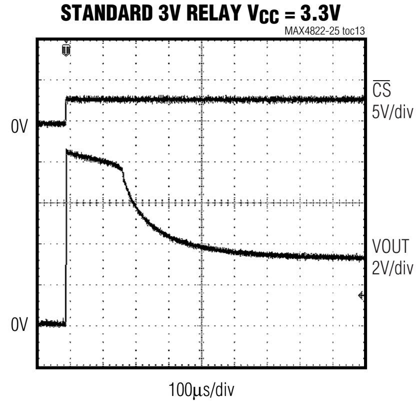

**OUT_ TURN-OFF DELAY TIME vs. SUPPLY VOLTAGE**



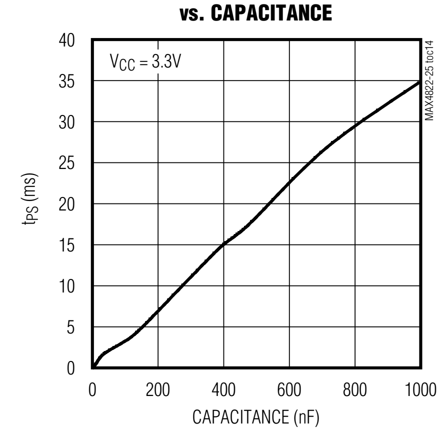

**INPUT-LOGIC THRESHOLD vs. SUPPLY VOLTAGE**



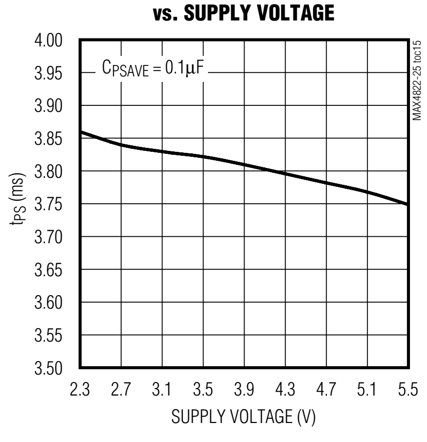

**BACK EMF CLAMPING WITH STANDARD 3V RELAY $V_{CC}$ = 3.3V**



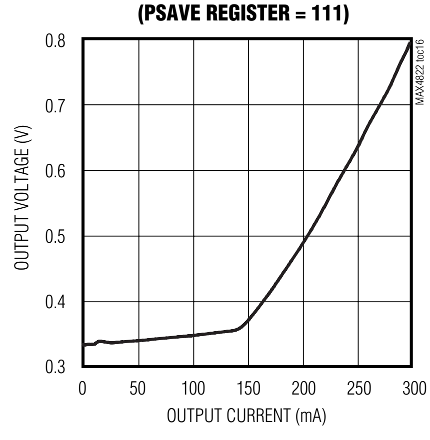

**POWER-SAVE DELAY TIME vs. CAPACITANCE**




**POWER-SAVE DELAY TIME vs. SUPPLY VOLTAGE**




**OUTPUT VOLTAGE vs. OUTPUT CURRENT IN POWER-SAVE MODE (PSAVE REGISTER = 111)**



## MAX4822/MAX4823 Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4822 | MAX4823 | | |
| 1 | 1 | $\overline{RESET}$ | Reset Input. Drive $\overline{RESET}$ low to clear all latches and registers (all outputs are high impedance). $\overline{RESET}$ overrides all other inputs. If $\overline{RESET}$ and $\overline{SET}$ are pulled low at the same time, then $\overline{RESET}$ takes precedence. |
| 2 | 2 | $\overline{CS}$ | Chip-Select Input. Drive $\overline{CS}$ low to select the device. When $\overline{CS}$ is low, data at DIN is clocked into the shift register on SCLK's rising edge. Drive $\overline{CS}$ from low to high to latch the data to the registers and activate the relay outputs. |
| 3 | 3 | DIN | Serial Data Input |
| 4 | 4 | SCLK | Serial Clock Input |
| 5 | 5 | DOUT | Serial Data Output. DOUT is the output of the shift register. DOUT can be used to daisy-chain multiple MAX4822/MAX4823 devices. The data at DOUT appears synchronous to SCLK's falling edge. |
| 6 | 6, 13 | N.C. | No Connection. Not internally connected. |
| 7 | 7 | GND | Ground |
| 8 | 8 | OUT8 | Open-Drain Output 8. Connect OUT8 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 9 | 9 | OUT7 | Open-Drain Output 7. Connect OUT7 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 10, 16 | 10, 16 | PGND | Power Ground. PGND is a return for the output sinks. Connect PGND pins together and to GND. |
| 11 | 11 | OUT6 | Open-Drain Output 6. Connect OUT6 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 12 | 12 | OUT5 | Open-Drain Output 5. Connect OUT5 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 13 | — | PSAVE | Power-Save Control. Connect a timing capacitor from PSAVE to ground. The capacitor value determines power-save timing as explained under the *Applications Information* section. PSAVE can also be driven externally to control power-save mode asynchronously. When asserted high, PSAVE reduces the current to all active outputs as determined by the *Power-Save Configuration Register* (see Figure 1). To disable power-save mode in all channels, drive PSAVE low for at least 3ms after the last output setting. |
| 14 | 14 | OUT4 | Open-Drain Output 4. Connect OUT4 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 15 | 15 | OUT3 | Open-Drain Output 3. Connect OUT3 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 17 | 17 | OUT2 | Open-Drain Output 2. Connect OUT2 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 18 | 18 | OUT1 | Open-Drain Output 1. Connect OUT1 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |

# +3.3V/+5V, 8-Channel Relay Drivers with Fast Recovery Time and Power-Save Mode

## MAX4822/MAX4823 Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4822 | MAX4823 | | |
| 19 | 19 | $V_{CC}$ | Input Supply Voltage. Bypass $V_{CC}$ to GND with a 0.1µF capacitor. |
| 20 | 20 | $\overline{SET}$ | Set Input. Drive $\overline{SET}$ low to set all latches and registers high (all outputs are low impedance). $\overline{SET}$ overrides all parallel and serial control inputs. $\overline{RESET}$ overrides $\overline{SET}$ under all conditions. |
| EP | EP | EP | Exposed Pad. Connect exposed paddle to GND. |

## MAX4824/MAX4825 Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4824 | MAX4825 | | |
| 1 | 1 | $\overline{RESET}$ | Reset Input. Drive $\overline{RESET}$ low to clear all latches and registers (all outputs are high impedance). $\overline{RESET}$ overrides all other inputs. If $\overline{RESET}$ and $\overline{SET}$ are pulled low at the same time, then $\overline{RESET}$ takes precedence. |
| 2 | 2 | $\overline{CS}$ | Chip-Select Input. Drive $\overline{CS}$ low to select the device. The $\overline{CS}$ falling edge latches the output address (A0, A1, A2). The $\overline{CS}$ rising edge latches level data (LVL). |
| 3 | 3 | LVL | Level Input. LVL determines whether the selected address is switched on or off. Logic-high on LVL switches on the addressed output. A logic-low on LVL switches off the addressed output. |
| 4 | 4 | A0 | Digital Address 0 Input. (See Figure 3 for address mapping.) |
| 5 | 5 | A1 | Digital Address 1 Input. (See Figure 3 for address mapping.) |
| 6 | 6 | A2 | Digital Address 2 Input. (See Figure 3 for address mapping.) |
| 7 | 7 | GND | Ground |
| 8 | 8 | OUT8 | Open-Drain Output 8. Connect OUT8 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 9 | 9 | OUT7 | Open-Drain Output 7. Connect OUT7 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 10, 16 | 10, 16 | PGND | Power Ground. PGND is a return for the output sinks. Connect PGND pins together and to GND. |
| 11 | 11 | OUT6 | Open-Drain Output 6. Connect OUT6 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 12 | 12 | OUT5 | Open-Drain Output 5. Connect OUT5 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |

## MAX4824/MAX4825 Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4824 | MAX4825 | | |
| 13 | — | PSAVE | Power-Save Control. Connect a timing capacitor from PSAVE to ground. The capacitor value determines power-save timing as explained under the *Applications Information* section. PSAVE can also be driven externally to control power-save mode asynchronously. When PSAVE is asserted high, the current through the coils is reduced to 60% of the initial nominal current value. To disable power-save mode in all channels, drive PSAVE low for at least 3ms after last output setting. |
| 14 | 14 | OUT4 | Open-Drain Output 4. Connect OUT4 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 15 | 15 | OUT3 | Open-Drain Output 3. Connect OUT3 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 17 | 17 | OUT2 | Open-Drain Output 2. Connect OUT2 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 18 | 18 | OUT1 | Open-Drain Output 1. Connect OUT1 to the low side of a relay coil. This output is pulled to PGND when activated, but otherwise is high impedance. |
| 19 | 19 | $V_{CC}$ | Input Supply Voltage. Bypass $V_{CC}$ to GND with a 0.1µF capacitor. |
| 20 | 20 | $\overline{SET}$ | Set Input. Drive $\overline{SET}$ low to set all latches and registers high (all outputs are low impedance). $\overline{SET}$ overrides all parallel and serial control inputs. $\overline{RESET}$ overrides $\overline{SET}$ under all conditions. |
| — | 13 | N.C. | No Connection. Not internally connected. |
| EP | EP | EP | Exposed Pad. Connect exposed paddle to ground. |

## Detailed Description

### Serial Interface (MAX4822/MAX4823)

Depending on the MAX4822/MAX4823 device, the serial interface can be controlled by either 8- or 16-bit words as depicted in Figures 1 and 2. The MAX4823 does not support power-save mode, so the serial interface consists of an 8-bit-only shift register for faster control.

The MAX4822 consists of a 16-bit shift register and parallel latch controlled by SCLK and $\overline{CS}$. The input to the shift register is a 16-bit word. In the MAX4822, the first 8 bits determine the register address and are followed by 8 bits of data as depicted in Figure 1. Bit A7 corresponds to the MSB of the 8-bit register address in Figure 1, while bit D7 corresponds to the MSB of the 8 bits of data in the same Figure 1.

The MAX4823 consists of an 8-bit shift register and parallel latch controlled by SCLK and $\overline{CS}$. The input to the shift register is an 8-bit word. Each data bit controls one of the eight outputs, with the most significant bit (D7) corresponding to OUT8, and the least significant bit (D0) corresponding to OUT1 (see Figure 2).

| ADDRESS [A7...A0] | ACTIVE REGISTER |
|---|---|
| 00h | Output Control Register—OUTR |
| 01h | Power-Save Configuration Register—PS |

**Serial-Input Address Map**

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| $OUT_8$ | $OUT_7$ | $OUT_6$ | $OUT_5$ | $OUT_4$ | $OUT_3$ | $OUT_2$ | $OUT_1$ |
| MSB | | | | | | | LSB |

**Output Control Register—$OUT_R$ (Address = 00h)**

**Note:** Setting $D_N$ to logic 1 turns on output $OUT_{N+1}$. Setting $D_N$ to logic 0, turns off $OUT_{N+1}$. Example: Setting $D_2 = 1$ turns on $OUT_3$.

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | PS0 | PS1 | PS2 |
| MSB | | | | | | | LSB |

**Power-Save Configuration Register—PS (Address= 01h)**

| PS0 | PS1 | PS2 | POWER-SAVE CONFIGURATION |
|---|---|---|---|
| 0 | 0 | 0 | Power-save is disabled (Default Operation) |
| 0 | 0 | 1 | Power-save is enabled. $V_{OUT}$ set to 70% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 30%, typical after $t_{PS}$ ms. |
| 0 | 1 | 0 | Power-save is enabled. $V_{OUT}$ set to 60% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 40%, typical after $t_{PS}$ ms. |
| 0 | 1 | 1 | Power-save is enabled. $V_{OUT}$ set to 50% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 50%, typical after $t_{PS}$ ms. |
| 1 | 0 | 0 | Power-save is enabled. $V_{OUT}$ set to 40% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 60%, typical after $t_{PS}$ ms. |
| 1 | 0 | 1 | Power-save is enabled. $V_{OUT}$ set to 30% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 70%, typical after $t_{PS}$ ms. |
| 1 | 1 | 0 | Power-save is enabled. $V_{OUT}$ set to 20% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 80%, typical after $t_{PS}$ ms. |
| 1 | 1 | 1 | Power-save is enabled. $V_{OUT}$ set to 10% of $V_{CC}$, typical after $t_{PS}$ ms (see Note 1), causes $I_{OUT\_}$ to be reduced to approximately 90%, typical after $t_{PS}$ ms. |

**Power-Save Configuration Options**

**Note 1:** The time period $t_{PS}$ is determined by the capacitor connected to PSAVE.

*Figure 1. 16-Bit Register Map for MAX4822*

When $\overline{CS}$ is low (MAX4822/MAX4823 device is selected), data at DIN is clocked into the shift register synchronously with SCLK's rising edge. Driving $\overline{CS}$ from low to high latches the data in the shift register (Figures 5 and 6).

DOUT is the output of the shift register. Data appears on DOUT synchronously with SCLK's falling edge and is identical to the data at DIN delayed by eight clock cycles for the MAX4823, or 16 clock cycles for the MAX4822. When shifting the input data, A7 is the first input bit in and out of the shift register for the MAX4822 device. D7 is the first bit in or out of the shift register for

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| $OUT_8$ | $OUT_7$ | $OUT_6$ | $OUT_5$ | $OUT_4$ | $OUT_3$ | $OUT_2$ | $OUT_1$ |

**Note:** Setting $D_N$ to logic 1 turns on output $OUT_{N+1}$. Setting $D_N$ to logic 0 turns off output $OUT_{N+1}$.
Example: Setting the $D_2$ = 1 turns $OUT_3$ on.

*Figure 2. 8-Bit Register Map for MAX4823*

| A2 | A1 | A0 | OUTPUT |
|---|---|---|---|
| Low | Low | Low | OUT1 |
| Low | Low | High | OUT2 |
| Low | High | Low | OUT3 |
| Low | High | High | OUT4 |
| High | Low | Low | OUT5 |
| High | Low | High | OUT6 |
| High | High | Low | OUT7 |
| High | High | High | OUT8 |

*Figure 3. Register Address Map for MAX4824/MAX4825*

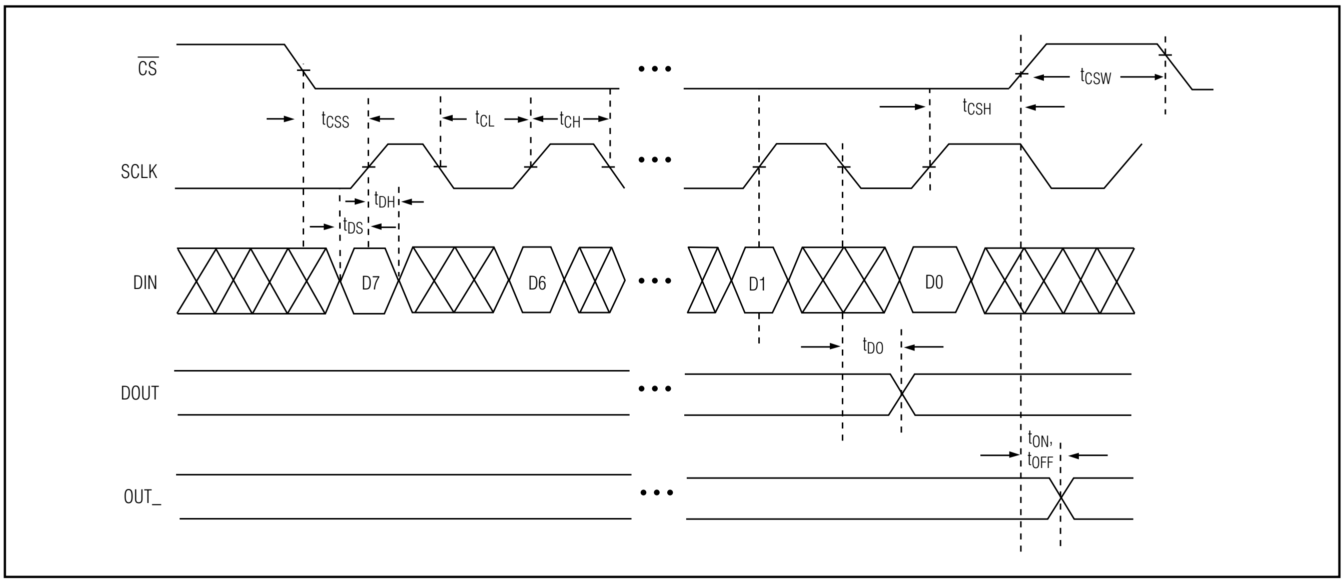



*Figure 4. 3-Wire Serial-Interface Timing Diagram*

the MAX4823 device. If the address A0…….A7 is not 00h or 01h, then the outputs and the PSAVE configuration register are not updated. The address is stored in the shift register only.

While $\overline{CS}$ is low, the OUT_ outputs always remain in their previous state. For the MAX4823, drive $\overline{CS}$ high after 8 bits of data have been shifted in to update the output state of the MAX4823, and to further inhibit data from entering the shift register. For the MAX4822, drive $\overline{CS}$ high after 16 bits of data have been shifted in to update the output state of the MAX4822, and to further inhibit data from entering the shift register. When $\overline{CS}$ is high, transitions at DIN and SCLK have no effect on the output, and the first input bit A7 (or D7) is present at DOUT.

For the MAX4822, if the number of data bits entered while $\overline{CS}$ is low is greater or less than 16, the shift register contains only the last 16 bits, regardless of when they were entered. For the MAX4823, if the number of data bits entered while $\overline{CS}$ is low is greater or less than 8, the shift register contains only the last 8 data bits, regardless of when they were entered.

### Parallel Interface (MAX4824/MAX4825)

The parallel interface consists of 3 address bits (A0, A1, A2) and one level selector bit (LVL). The address bits determine which output is updated, and the level bit determines whether the addressed output is switched on (LVL = high) or off (LVL = low). When $\overline{CS}$ is high, the address and level bits have no effect on the state of the outputs. Driving $\overline{CS}$ from low to high latches

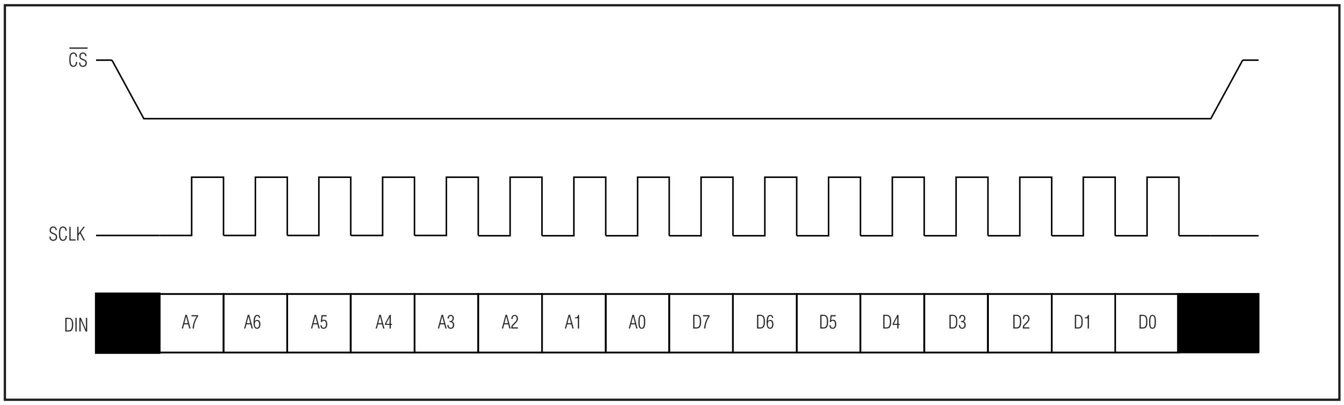



*Figure 5. 3-Wire Serial-Interface Operation for MAX4822*

level data to the parallel register and updates the state of the outputs. Address data entered after $\overline{CS}$ is pulled low is not reflected in the state of the outputs following the next low-to-high transition on $\overline{CS}$ (Figure 7).

### $\overline{SET}$/$\overline{RESET}$ Functions

The MAX4822–MAX4825 feature set and reset inputs that allow simultaneous turn-on or turn-off of all outputs using a single control line. Drive $\overline{SET}$ low to set all latches and registers to 1 and turn all outputs on. $\overline{SET}$ overrides all serial/parallel control inputs. Drive $\overline{RESET}$ low to clear all latches and registers and to turn all outputs off. $\overline{RESET}$ overrides all other inputs including $\overline{SET}$.

### Power-On Reset

The MAX4822–MAX4825 feature power-on reset. The power-on reset function causes all latches to be cleared automatically upon power-up. This ensures that all outputs come up in the off or high-impedance state.

## Applications Information

### Daisy Chaining

The MAX4822/MAX4823 feature a digital output (DOUT) that provides a simple way to daisy chain multiple devices. This feature allows driving large banks of relays using only a single serial interface. To daisy chain multiple devices, connect all $\overline{CS}$ inputs together, and connect the DOUT of one device to the DIN of another device (see Figure 8). During operation, a stream of serial data is shifted through the MAX4822/MAX4823 devices in series. When $\overline{CS}$ goes high, all outputs update simultaneously.

The MAX4822/MAX4823 can also be used in a slave configuration that allows individual addressing of devices. Connect all the DIN inputs together, and use the $\overline{CS}$ input to address one device at a time. Drive $\overline{CS}$ low to select a slave and input the data into the shift register. Drive $\overline{CS}$ high to latch the data and turn on the appropriate outputs. Typically, in this configuration only one slave is addressed at a time.

### Power-Save Mode

The MAX4822/MAX4824 feature a unique power-save mode where the relay current, after activation, can be reduced to a level just above the relay hold-current threshold. This mode keeps the relay activated while significantly reducing the power consumption.

In serial mode (MAX4822), choose between seven current levels ranging from 30% to 90% of the nominal current in 10% increments. The actual percentage is determined by the power-save configuration register (Figure 1).

In parallel mode (MAX4824), the power-save current is fixed at 60% of the nominal current.

#### Power-Save Timer

Every time there is a write operation to the device ($\overline{CS}$ transitions from low to high), the MAX4822/MAX4824 start charging the capacitor connected to PSAVE. The serial power-save implementation is such that a write operation does not change the state of channels already in power-save mode (unless the write turns the channel OFF).

After a certain time period, $t_{PS}$ (determined by the capacitor value), the capacitor reaches a voltage threshold that sets all active outputs to power-save mode. The $t_{PS}$ period should be made long enough to allow the relay to turn on completely. The time period $t_{PS}$ can be adjusted by using different capacitor values connected to PSAVE. The value $t_{PS}$ is given by the following formula:

$$t_{PS} = 32 \times C$$

where C is in µF and $t_{PS}$ is in ms.

For example, if the desired $t_{PS}$ is 20ms, then the required capacitor value is 20 / 32 = 0.625µF.

### Power-Save Mode Accuracy

The current through the relay is controlled by setting the voltage at OUT_ to a percentage of the $V_{CC}$ supply as specified under the *Electrical Characteristics* and in the register description. The current through the relay ($I_{OUT}$) depends on the switch on-resistance, $R_{ON}$, in addition to the relay resistance $R_R$ according to the following relation:

$$I_{OUT} = V_{CC} / (R_{ON} + R_R)$$

The power-save, current-setting $I_{PS}$ depends on the fraction $\alpha$ of the supply voltage $V_{CC}$ that is set by the loop depending on the following relation:

$$I_{PS} = V_{CC} - (\alpha \times V_{CC}) / R_R$$

Therefore:

$$I_{PS} / I_{OUT} = (1- \alpha) \times (1 + R_{ON} / R_R)$$

This relation shows how the fraction of reduction in the current depends on the switch on-resistance, as well as from the accuracy of the voltage setting ($\alpha$). The higher the $R_{ON}$ with respect to $R_R$, the higher the inaccuracy. This is particularly true at low voltage when the relay resistance is low (less than 40Ω) and the switch can account for up to 10% of the total resistance. In addition, when the supply-voltage setting ($\alpha$) is low (10% or 20%) and the supply voltage ($V_{CC}$) is low, the voltage drop across the switch ($I_{OUT} \times R_{ON}$) may already exceed, or may be very close to, the desired voltage-setting value.

### Daisy Chaining and Power-Save Mode

In a normal configuration using the power-save feature, several MAX4822s can be daisy chained as shown in Figure 9. For each MAX4822, the power-save timing $t_{PD}$ (time it takes to reduce the relay current once the relay is actuated) is controlled by the capacitor connected to PSAVE.

An alternative configuration that eliminates the PSAVE capacitors uses a common PSAVE control line driven by an open-drain n-channel MOSFET (Figure 10). In this configuration, the PSAVE inputs are connected together to asynchronously control the power-save timing for all the MAX4822s in the chain. The µC/µP drives the n-channel MOSFET low for the duration of a write cycle to the SPI chain, plus some delay time to allow the relays to close.

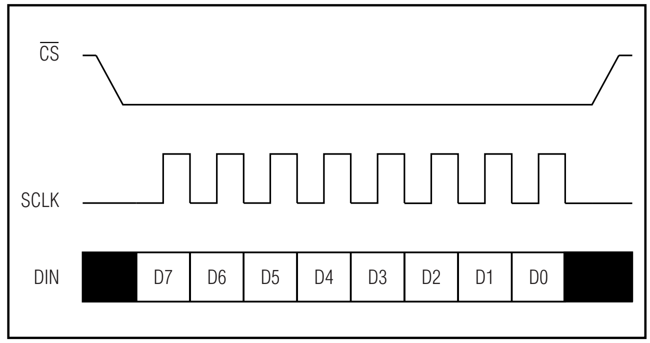



*Figure 6. 3-Wire Serial-Interface Operation for the MAX4823*

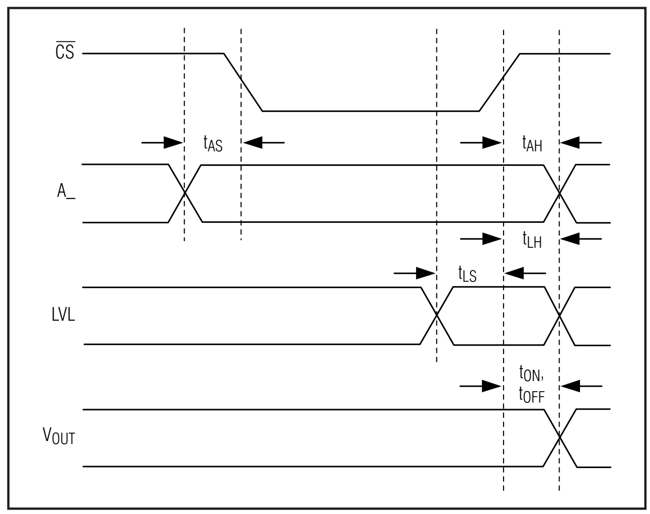



*Figure 7. Parallel-Interface Timing Diagram*

(This time is typically specified in the relay data sheet.) Once this delay time has elapsed, the n-channel MOSFET is turned off, allowing the MAX4822's internal 35µA pullup current to raise PSAVE to a logic-high level, activating the power-save mode in all active outputs.

### MOSFET Selection

In the daisy-chain configuration of Figure 10, the n-channel MOSFET drives PSAVE low. When the n-channel MOSFET is turned off, PSAVE is pulled high by an internal 35µA pullup in each MAX4822, and the power-save mode is enabled. Because of the paralleled PSAVE pullup currents, the required size of the n-channel MOSFET depends upon the number of MAX4822 devices in the chain. Determine the size of the n-channel MOSFET by the following relation:

$$R_{ON} < 1428 / N$$

# +3.3V/+5V, 8-Channel Relay Drivers with Fast Recovery Time and Power-Save Mode

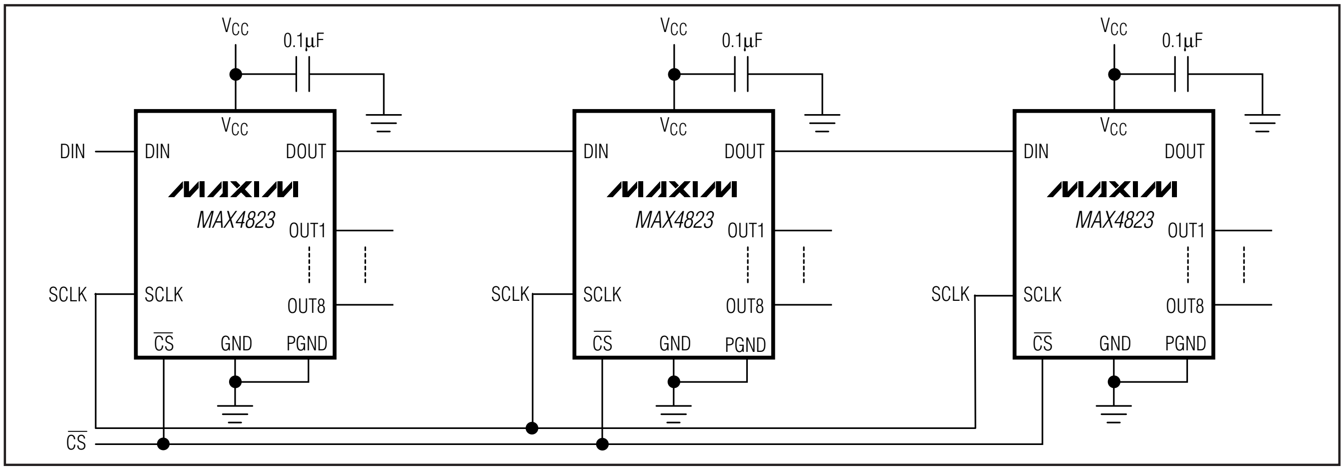



*Figure 8. Daisy-Chain Configuration*

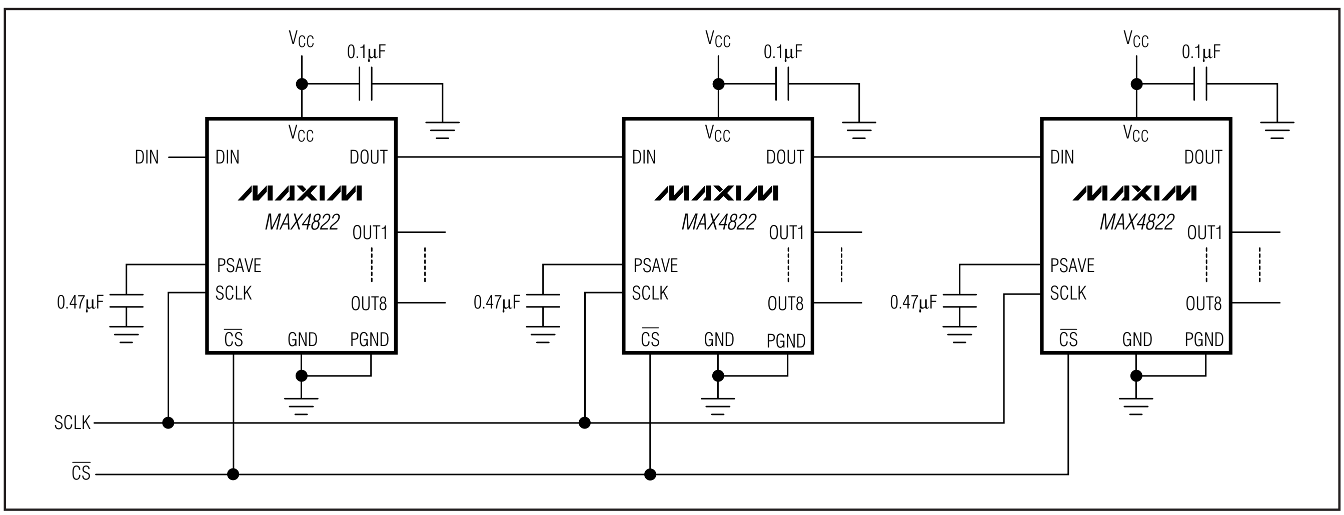



*Figure 9. Daisy-Chained MAX4822s with a Capacitor Connected to PSAVE*

where N is the total number of MAX4822 devices in a single chain, and $R_{ON}$ is the on-resistance of the n-channel MOSFET in Ωs.

For example, if N = 10:

$$R_{ON} < 142\Omega$$

An n-channel MOSFET with $R_{ON}$ less than 142Ω is required for a daisy chain of 10 MAX4822 devices.

### Inductive Kickback Protection with Fast Recovery Time

The MAX4822–MAX4825 feature built-in inductive kickback protection to reduce the voltage spike on OUT_ generated by a relay's coil inductance when the output is suddenly switched off. An internal Zener clamp allows the inductor current to flow back to ground. The Zener configuration significantly reduces the recovery time (time it takes to turn off the relay) when compared to protection configurations with just one diode across the coil.

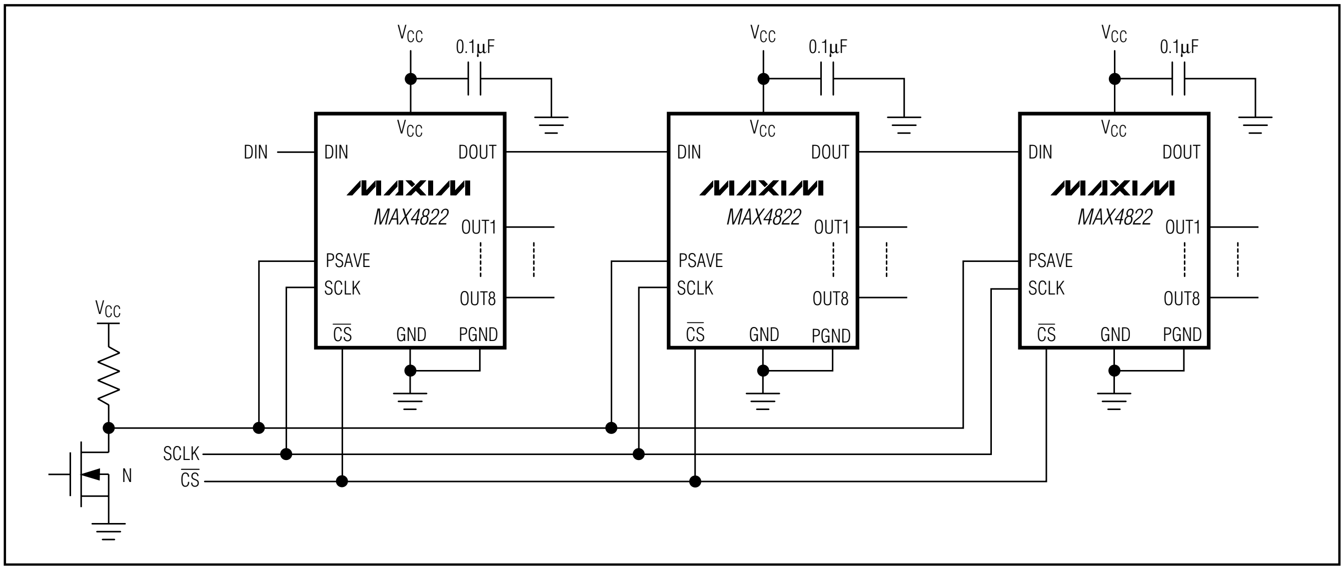


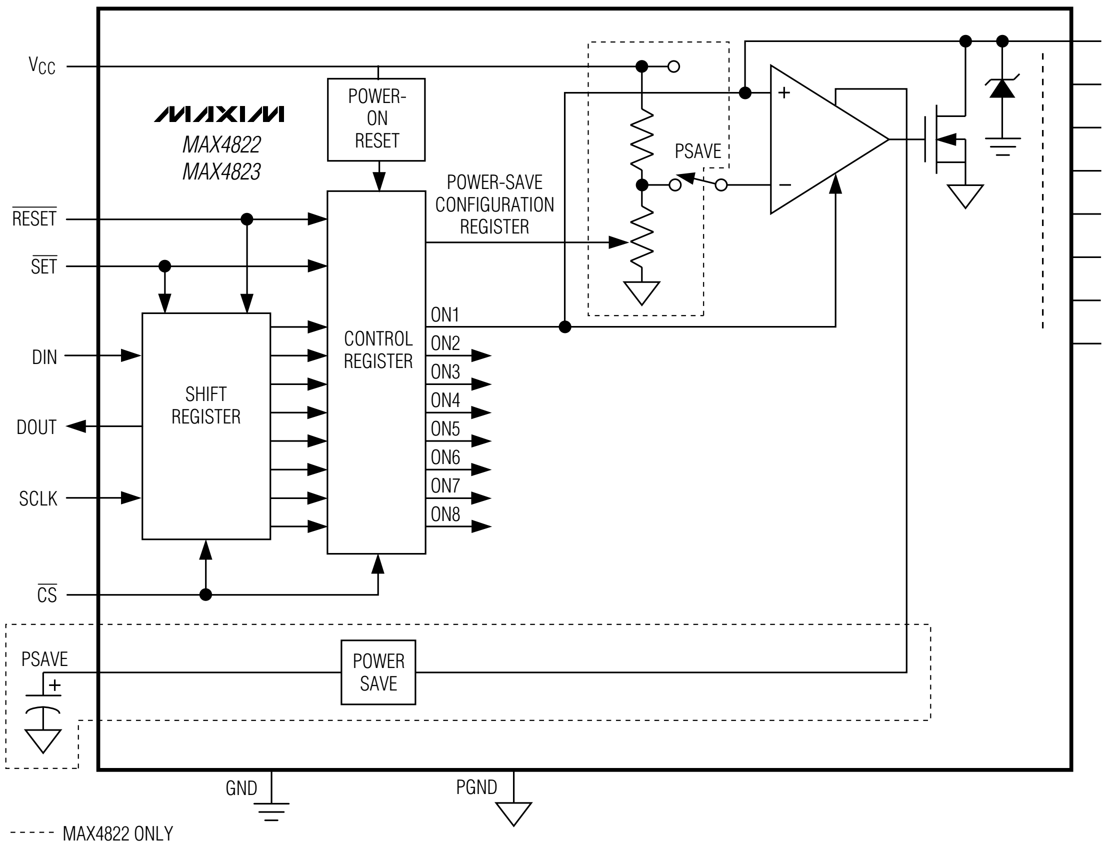

*Figure 10. Daisy-Chaining MAX4822s with a PSAVE Connected to an n-Channel MOSFET*

## Chip Information

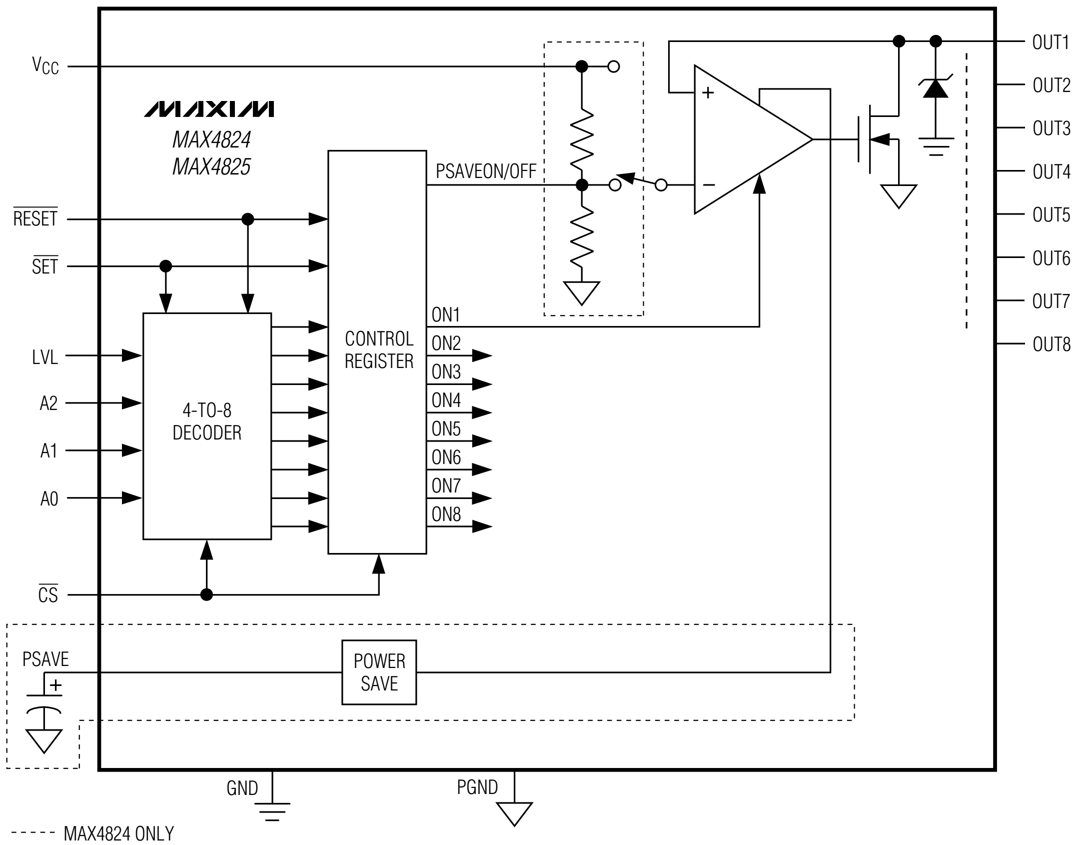
TRANSISTOR COUNT: 5799

PROCESS: BiCMOS

## MAX4822/MAX4823 Functional Diagram (Serial Interface)

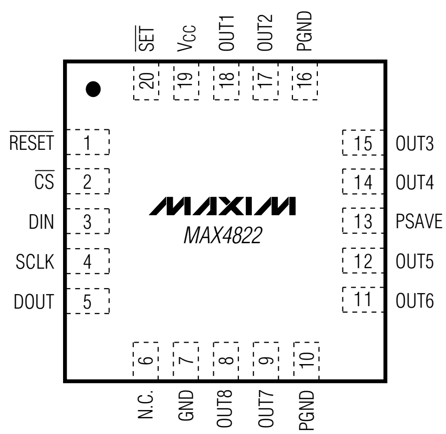


## MAX4824/MAX4825 Functional Diagram (Parallel Interface)

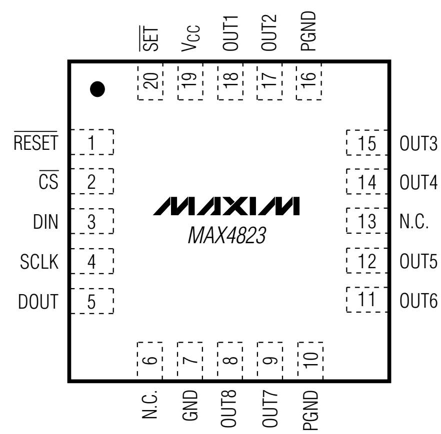


## Pin Configurations

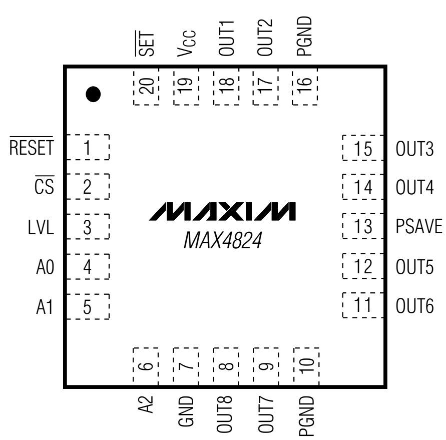
TOP VIEW



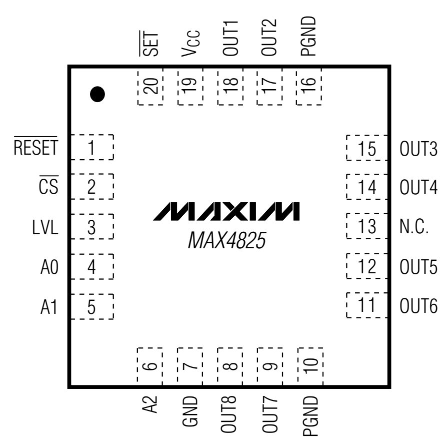

THIN QFN




THIN QFN



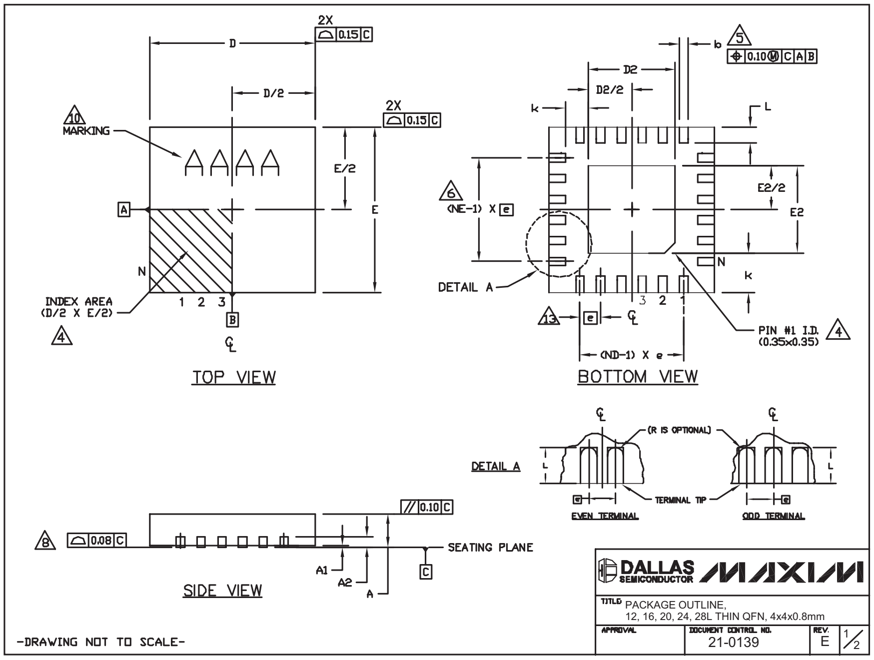

THIN QFN




THIN QFN

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| COMMON DIMENSIONS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PKG | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | | 28L 4x4 | | |
| REF. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 | 0.15 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | | 28 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | | 7 | | |
| Jedec Var. | WGGB | | | WGGC | | | WGGD-1 | | | WGGD-2 | | | WGGE | | |

| EXPOSED PAD VARIATIONS | | | | | | | |
|---|---|---|---|---|---|---|---|
| PKG. CODES | D2 | | | E2 | | | DOWN BONDS ALLOWED |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| T1244-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T1244-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T1644-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T1644-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2044-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T2044-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2444-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T2444-3 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | YES |
| T2444-4 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | NO |
| T2844-1 | 2.50 | 2.60 | 2.70 | 2.50 | 2.60 | 2.70 | NO |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. E | 2/2

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