LOW-POWER CAN TRANSCEIVER WITH BUS WAKE-UP

Check for Samples: SN65HVD1040-HT

FEATURES

- **Improved Drop-in Replacement for the TJA1040**
- **±12 kV ESD Protection**
- **Low-Current Standby Mode with Bus Wake-up: 5 µA Typical**
- **Bus-Fault Protection of –27 V to 40 V**
- **Rugged Split-Pin Bus Stability**
- **Dominant Time-Out Function**
- **Thermal Shutdown Removed**
- **Power-Up/Down Glitch-Free Bus Inputs and Outputs**
  - **High Input Impedance with Low V_{CC}**
  - **Monotonic Outputs During Power Cycling**
- **DeviceNet Vendor ID # 806**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**
- **Vibration/Modal Analysis**
- **Multi-Channel Data Acquisition**
- **Acoustics/Dynamic Strain Gauges**
- **Pressure Sensors**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures. All devices are characterized and qualified for 1000 hours continuous operating life at maximum rated temperature.**

(1) Custom temperature ranges available

DESCRIPTION

The SN65HVD1040 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). As CAN transceivers, these devices provide differential transmit and receive capability for a CAN controller at signaling rates of up to 1 megabit per second (Mbps). (2)

Designed for operation in especially harsh environments, the device features ±12 kV ESD protection on the bus and split pins, cross-wire, overvoltage and loss of ground protection from –27 to 40 V, a –12 V to 12 V common-mode range, and will withstand voltage transients from –200 V to 200 V according to ISO 7637.

The STB input (pin 8) selects between two different modes of operation; high-speed or low-power mode. The high-speed mode of operation is selected by connecting STB to ground.

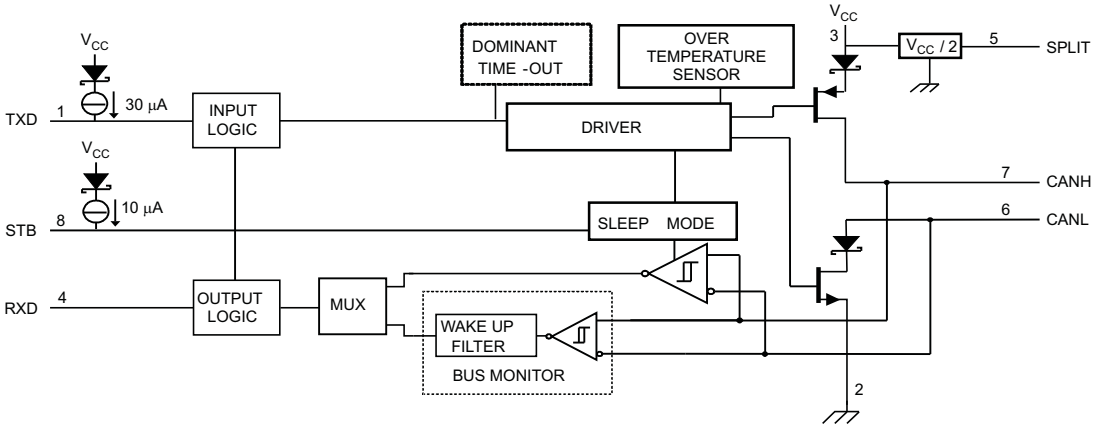
If a high logic level is applied to the STB pin of the SN65HVD1040, the device enters a low-power bus-monitor standby mode. While the SN65HVD1040 is in the low-power bus-monitor standby mode, a dominant bit greater than 5 µs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

A dominant-time-out circuit in the SN65HVD1040 prevents the driver from blocking network communication during a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

(2) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

The SPLIT output (pin 5) is available on the SN65HVD1040 as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network.

The SN65HVD1040 is characterized for operation from –55°C to 210°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	KGD (bare die)	SN65HVD1040SKGD3	NA
	HKQ	SN65HVD1040SHKQ	HVD1040SHKQ
–55°C to 175°C	D	SN65HVD1040HD	H1040

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Floating	CuNiPd	15 microns

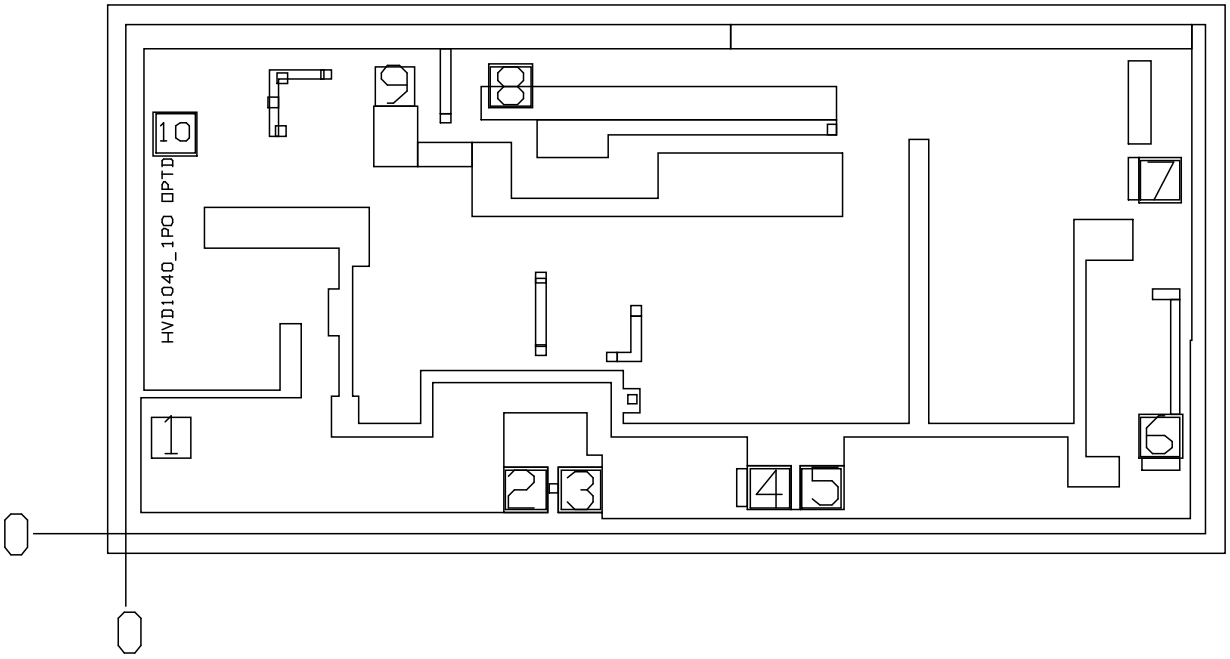


Table 2. BOND PAD COORDINATES (µm)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX	PAD SIZE X	PAD SIZE Y
TXD	1	53.64	162	137.7	246.06	84.06	84.06
GND	2	804.06	50.85	888.12	134.91	84.06	84.06
GND	3	920.07	50.85	1004.13	134.91	84.06	84.06
Vcc	4	1320.21	54.18	1404.27	138.24	84.06	84.06
Vcc	5	1431.09	54.18	1515.15	138.24	84.06	84.06
RXD	6	2148.75	164.34	2232.81	248.4	84.06	84.06
SPLIT	7	2147.4	707.49	2231.46	791.55	84.06	84.06
CANL	8	771.93	907.38	855.99	991.44	84.06	84.06
CANH	9	527.31	907.38	611.37	991.44	84.06	84.06
STB	10	62.28	806.13	146.34	890.19	84.06	84.06

ABSOLUTE MAXIMUM RATINGS(1)

				VALUE
V_{CC}	Supply voltage(2)			–0.3 V to 7 V
$V_{I(bus)}$	Voltage range at any bus terminal (CANH, CANL, SPLIT)			–27 V to 40 V
$I_{O(OUT)}$	Receiver output current			-20 mA to 20 mA
	Voltage input, transient pulse(3), (CANH, CANL, SPLIT)			–200 V to 200 V
ESD	IEC Contact Discharge	(IEC 61000-4-2)	Bus terminals vs GND	±6 kV
	Human body model	JEDEC Standard 22, Test Method A114-C.01	Bus terminals vs GND	±12 kV
			All pins	±4 kV
	Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1 kV
	Machine model	ANSI/ESDS5.2-1996		±200 V
IEC			Bus terminals vs GND	±6 kV
V_I	Voltage input range (TXD, STB)			–0.5 V to 6 V
T_J	Junction temperature			–55°C to 210°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6 & 7.

THERMAL CHARACTERISTICS FOR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

THERMAL INFORMATION FOR D PACKAGE

THERMAL METRIC(1)		SN65HVD1040 D 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	91.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	39.9	
θ_{JB}	Junction-to-board thermal resistance(4)	40.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	3.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	39.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	4.75		5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12(1)		12	–12(1)		12	–12(1)		12	V
V_{IH}	High-level input voltage	TXD, STB	2		5.25	2		5.25	2		5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0		0.8	0		0.8	0		0.8	V
V_{ID}	Differential input voltage		–6		6	–6		6	–6		6	V
I_{OH}	High-level output current	Driver	–70			–70			–70			mA
		Receiver	–2			–2			–2			
I_{OL}	Low-level output current	Driver			70			70			70	mA
		Receiver			2			2			2	
t_{SS}	Maximum pulse width to remain in standby				0.7			0.7			0.7	µs
T_J	Junction temperature		–55		125	–55		175	–55		210	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current, V_{CC}	Dominant	V_I = 0 V, 60 Ω Load, STB at 0 V		50	70		50	70		50	70	mA
		Recessive	V_I = V_{CC}, STB at 0 V		6	10		6	10		6	10	
		Standby	STB at VCC, VI = VCC		5	12		5	20		5	50	µA

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	STB at 0 V, See Figure 10	90		230	90		325	90		450	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	STB at 0 V, See Figure 10	90		230	90		325	90		450	ns

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
$V_{O(D)}$	Bus output voltage (Dominant)	CAN H	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 2 and Figure 3	2.9	3.4	4.5	2.9	3.4	4.6	2.9	3.4	4.6	V
		CANL		0.8		1.75	0.8		1.75	0.8		1.75	
$V_{O(R)}$	Bus output voltage (Recessive)		V_I = 3 V, STB at 0 V, See Figure 2 and Figure 3	2	2.5	3	2	2.5	3	2	2.5	3	V
V_O	Bus output voltage (Standby)		R_L = 60 Ω, STB at V_{CC}, See Figure 2 and Figure 3	–0.1		0.1	–0.125		0.125	–0.15		0.15	V
$V_{OD(D)}$	Differential output voltage (Dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 2 and Figure 3, and Figure 4	1.5		3	1.5		3	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 2 and Figure 3	1.4		3	1.4		3	1.4		3	
V_{SYM}	Output symmetry (Dominant or Recessive) [$V_{O(CANH)}$ + $V_{O(CANL)}$]		STB at 0 V, See Figure 3 and Figure 14	0.9×V_{CC}	V_{CC}	1.1×V_{CC}	0.9×V_{CC}	V_{CC}	1.1×V_{CC}	0.9×V_{CC}	V_{CC}	1.2×V_{CC}	V
$V_{OD(R)}$	Differential output voltage (Recessive)		V_I = 3 V, R_L = 60 Ω, STB at 0 V, See Figure 2 and Figure 3	–0.012		0.012	–0.014		0.017	–0.015		0.02	V
			V_I = 3 V, STB at 0 V, No Load	–0.5		0.05	–0.5		0.225	–0.75		0.8	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		STB at 0 V, See Figure 9	2	2.3	3	2	2.3	3	2	2.3	3.1	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3			0.3			0.3		
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	–3		3	–3		3	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	–50		–10	–50		–10	µA
$I_{O(off)}$	Power-off TXD Leakage current		V_{CC} at 0 V, TXD at 5 V			1			180			600	µA
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL Open, See Figure 13	–120	–72		–120	–72		–130	–72		mA
			V_{CANH} = 12 V, CANL Open, See Figure 13		0.36	1		0.36	1		0.36	1.1	
			V_{CANL} = –12 V, CANH Open, See Figure 13	–1	–0.5		–1	–0.5		–1.1	–0.5		
			V_{CANL} = 12 V, CANH Open, See Figure 13		71	120		71	120		71	130	
C_O	Output capacitance		See Input capacitance to ground in *RECEIVER ELECTRICAL CHARACTERISTICS* .										

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V, See Figure 5	25	65	120	25	65	175	25	65	250	ns
t_{PHL}	Propagation delay time, high-to-low-level output		25	45	120	25	45	175	25	45	250	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				25		25				25	
t_r	Differential output signal rise time			25			25			25		
t_f	Differential output signal fall time			50			50			50		
t_{en}	Enable time from silent mode to dominant	See Figure 8			11			14.5			18	µs
t_{dom}	Dominant time-out	See Figure 11	300	450	700	300	450	700	300	450	700	µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IT+}	Positive-going input threshold voltage	High-speed mode	STB at 0 V, See Table 3		800	900		800	900		800	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		500	650		500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		STB at V_{CC}	100	125		70	125		70	125		
V_{IT}	Input threshold voltage	Standby mode	STB at V_{CC}	500		1150	500		1300	400		1350	
V_{OH}	High-level output voltage		I_O = –2 mA, See Figure 7	4	4.6		4	4.6		4	4.6		V
V_{OL}	Low-level output voltage		I_O = 2 mA, See Figure 7		0.2	0.4		0.2	0.5		0.2	0.55	V
$I_{I(off)}$	Power-off bus input current		CANH or CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			5			15			30	µA
$I_{O(off)}$	Power-off RXD leakage current		V_{CC} at 0 V, RXD at 5 V			20			30			30	µA
C_I	Input capacitance to ground, (CANH or CANL)		TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		20			20			20		pF
C_{ID}	Differential input capacitance		TXD at 3 V, V_I = 0.4 sin (4E6πt)		10			10			10		pF
R_{ID}	Differential input resistance		TXD at 3 V, STD at 0 V	30		80	30		80	30		80	kΩ
R_{IN}	Input resistance, (CANH or CANL)		TXD at 3 V, STD at 0 V	15	30	40	15	30	40	15	30	40	
$R_{I(m)}$	Input resistance matching $[1 - (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$		$V_{CANH} = V_{CANL}$	–3%	0%	3%	–5%	0%	5%	–12%	0%	12%	

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pLH}	Propagation delay time, low-to-high-level output	STB at 0 V, TXD at 3 V, See Figure 7	60	100	130	60	100	200	60	100	200	ns
t_{pHL}	Propagation delay time, high-to-low-level output		45	70	130	45	70	200	45	70	200	
t_r	Output signal rise time			8			8			8		
t_f	Output signal fall time			8			8			8		
t_{BUS}	Dominant time required on bus for wake-up from standby(1)	STB at V_{CC} Figure 12	0.7		5	1.0		5.1	1.45		5.25	µs

(1) The device under test shall not signal a wake-up condition with dominant pulses shorter than t_{BUS} (min) and shall signal a wake-up condition with dominant pulses longer than t_{BUS} (max). Dominant pulses with a length between t_{BUS} (min) and t_{BUS} (max) may lead to a wake-up.

SPLIT-PIN CHARACTERISTICS

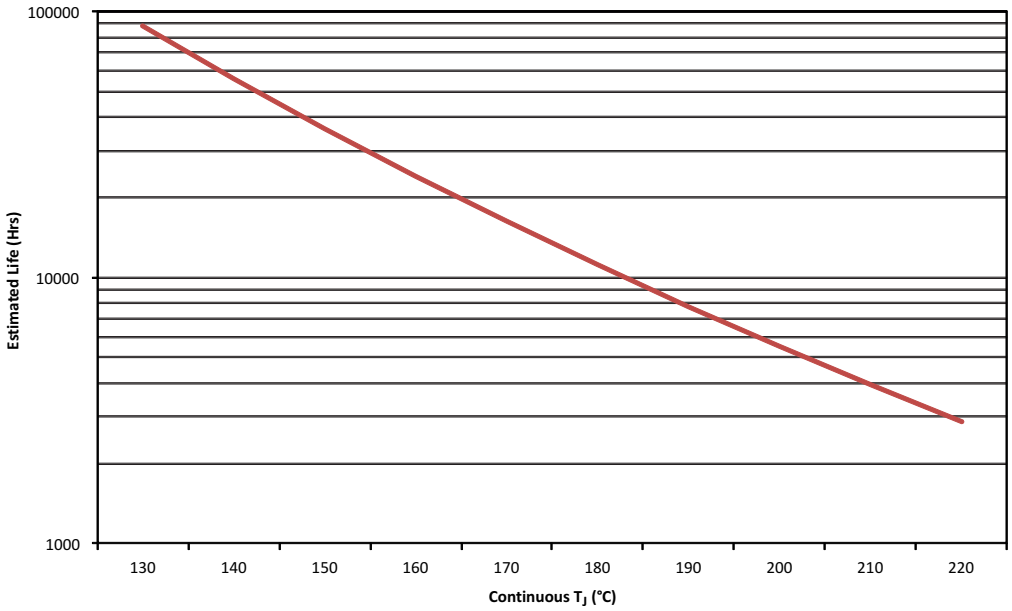
over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output voltage	–500 µA < I_O < 500 µA	$0.3\times V_{CC}$	$0.5\times V_{CC}$	$0.7\times V_{CC}$	$0.28\times V_{CC}$	$0.5\times V_{CC}$	$0.7\times V_{CC}$	$0.28\times V_{CC}$	$0.5\times V_{CC}$	$0.7\times V_{CC}$	V
$I_{O(stb)}$	Standby mode leakage current	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	–7		7	–15		15	µA

STB-PIN CHARACTERISTICS

over recommended operating conditiions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J = -55°C to 125°C			T_J = -55°C to 175°C			T_J = -55°C to 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{IH}	High level input current	STB at 2 V	–10		0	–10		0	–10		0	µA
I_{IL}	Low level input current	STB at 0 V	–10		0	–10		0	–10		0	µA



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

Figure 1. SN65HVD1040-HT Operating Life Derating Chart

PARAMETER MEASUREMENT INFORMATION

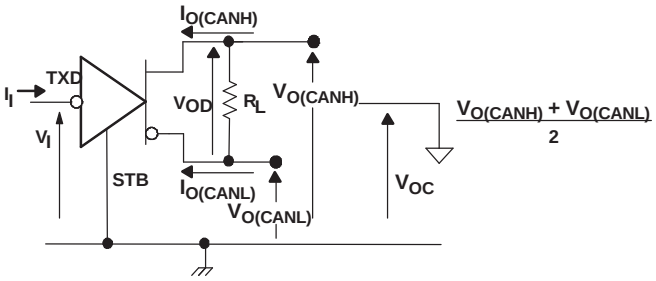


Figure 2. Driver Voltage, Current, and Test Definition

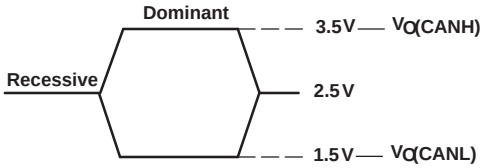


Figure 3. Bus Logic State Voltage Definitions

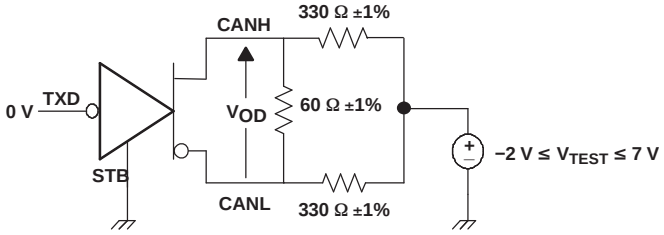


Figure 4. Driver V_{OD} Test Circuit

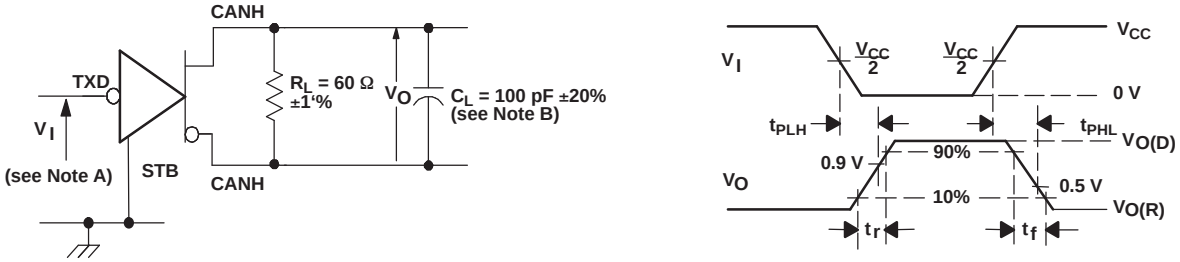


Figure 5. Driver Test Circuit and Voltage Waveforms

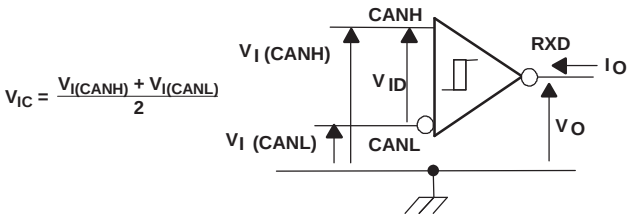
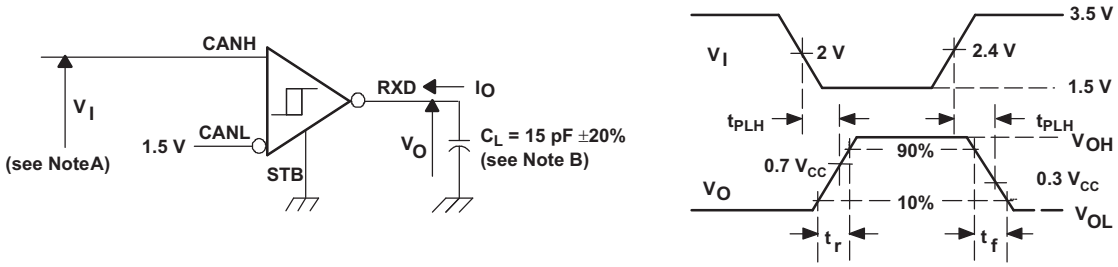


Figure 6. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 7. Receiver Test Circuit and Voltage Waveforms

Table 3. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

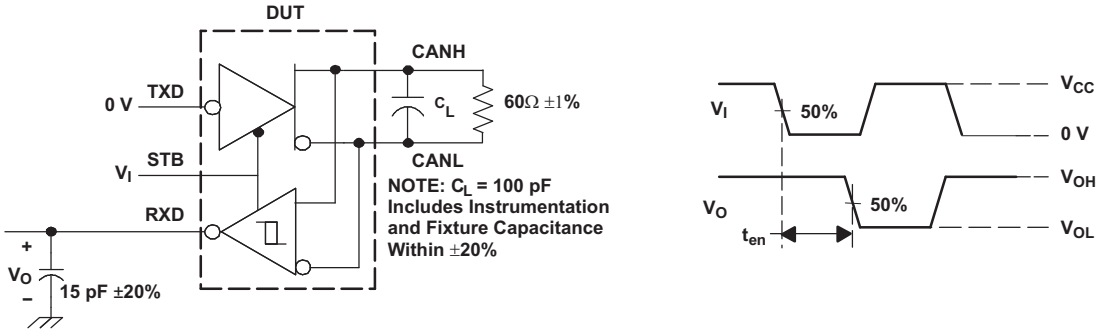
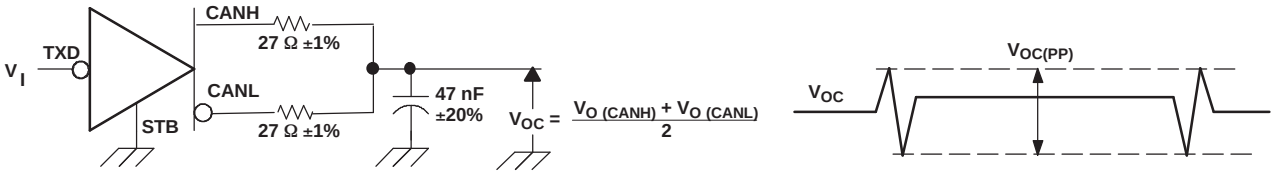
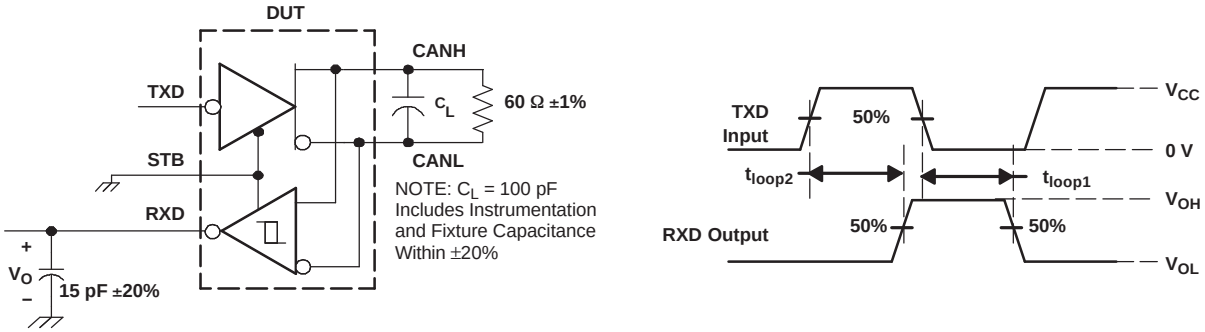


Figure 8. t_{en} Test Circuit and Voltage Waveforms



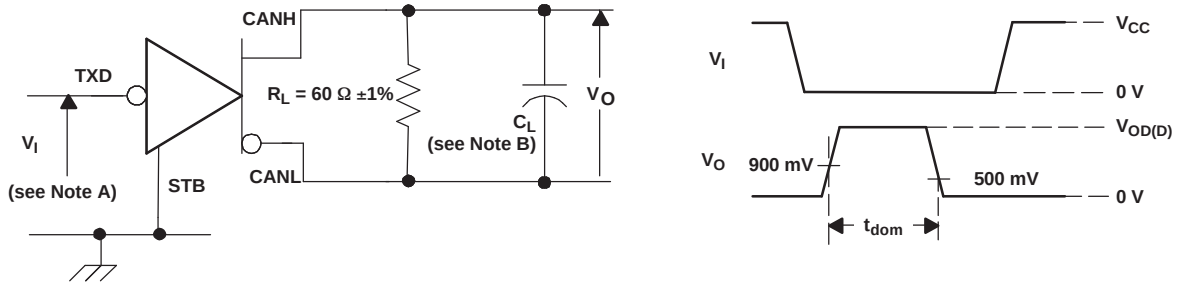
A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. Peak-to-Peak Common Mode Output Voltage Test and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

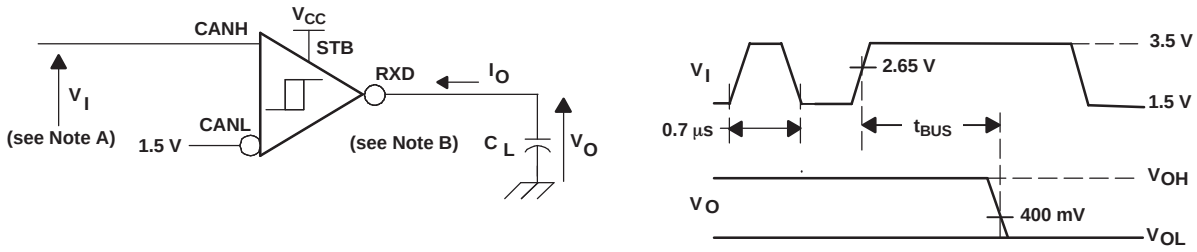
Figure 10. t_{loop} Test Circuit and Voltage Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator with the following characteristics: t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 11. Dominant Time-Out Test Circuit and Waveform



A. For V_I bit width ≤ 0.7 µs, V_O = V_{OH}. For V_II bit width ≥ 5 µs, V_O = V_{OL}. V_I input pulses are supplied from a generator with the following characteristics; t_r or t_f ≤ 6 ns. Pulse Repetition Rate (PRR) = 50 Hz, 30% duty cycle.

B. C_L = 15 pF includes instrumentation and fixture capacitance within ±20%.

Figure 12. t_{BUS} Test Circuit and Waveform

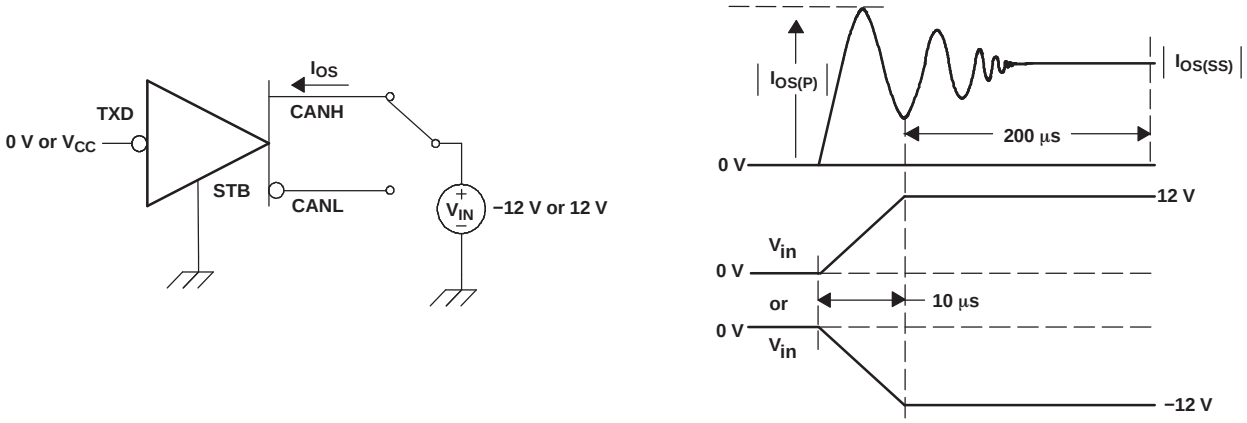


Figure 13. Driver Short-Circuit Current Test and Waveform

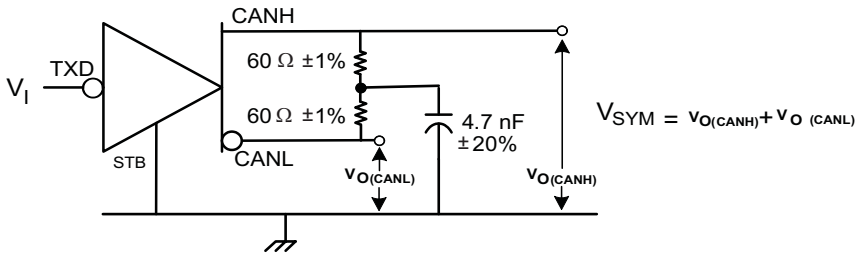


Figure 14. Driver Output Symmetry Test Circuit

DEVICE INFORMATION

Table 4. DRIVER FUNCTION TABLE(1)

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	DOMINANT
H	L	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H or Open	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; Z = high impedance

Table 5. RECEIVER FUNCTION TABLE(1)

DIFFERENTIAL INPUTS V_{ID} = CANH - CANL	STB	OUTPUT RXD	BUS STATE
V_{ID} ≥ 0.9 V	L	L	DOMINANT
V_{ID} ≥ 1.15 V	H or Open	L	DOMINANT
0.5 V < V_{ID} < 0.9 V	X	?	?
V_{ID} ≤ 0.5 V	X	H	RECESSIVE
Open	X	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

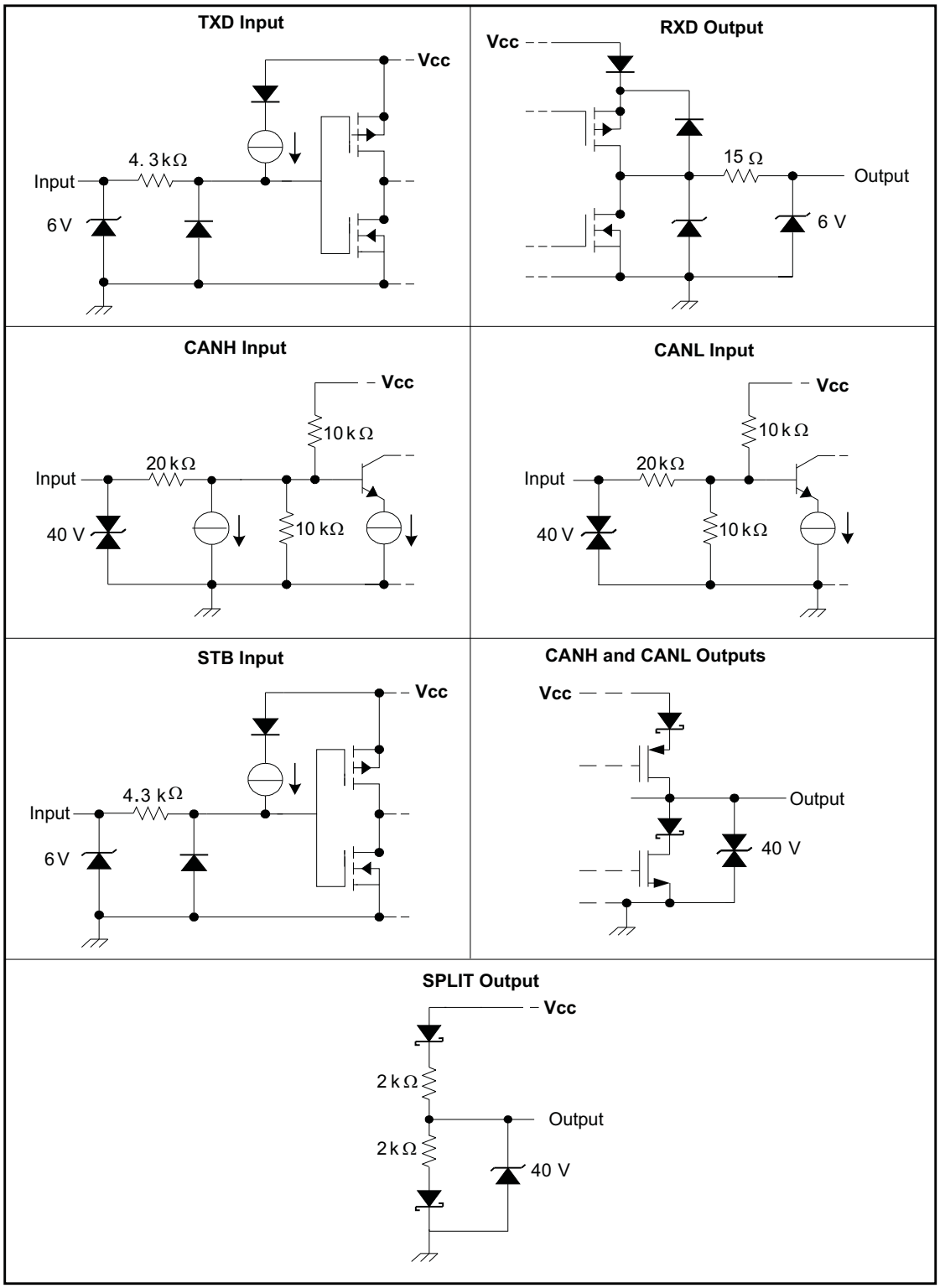
DEVICE INFORMATION

Table 6. Parametric Cross Reference With the TJA1040

TJA1040 (1)	PARAMETER	HVD10xx
TJA1040 DRIVER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
TJA1040 BUS SECTION		
$V_{th(dif)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{hys(dif)}$	Differential input hysteresis	Receiver V_{hys}
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{i(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{O(dif0(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$R_{i(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{i(def)}$	Differential input resistance	Receiver R_{ID}
$R_{i(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
$C_{i(cm)}$	Input capacitance to ground	Receiver C_I
$C_{i(dif)}$	Differential input capacitance	Receiver C_{ID}
TJA1040 RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
TJA1040 SPLIT PIN SECTION		
V_O	Reference output voltage	V_O
TJA1040 TIMING SECTION		
$t_{d(TXD-BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD-BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon-RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
$t_{PD(TXD–RXD)}$	Prop delay TXD to RXD	Device t_{LOOP1} and t_{LOOP2}
$t_{d(stb-norm)}$	Enable time from standby to dominant	Driver t_{en}
TJA1040 STB PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1040 Product Specification, Philips Semiconductors, 2003 February 19.

Equivalent Input and Output Schematic Diagrams



TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

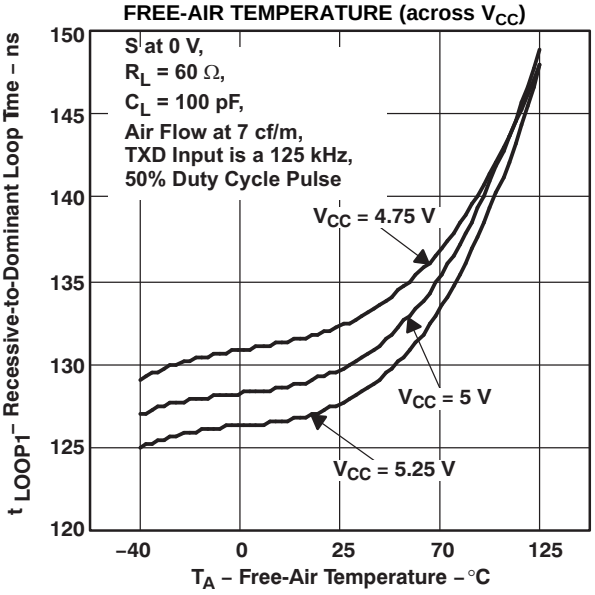


Figure 15.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (across V_{CC})

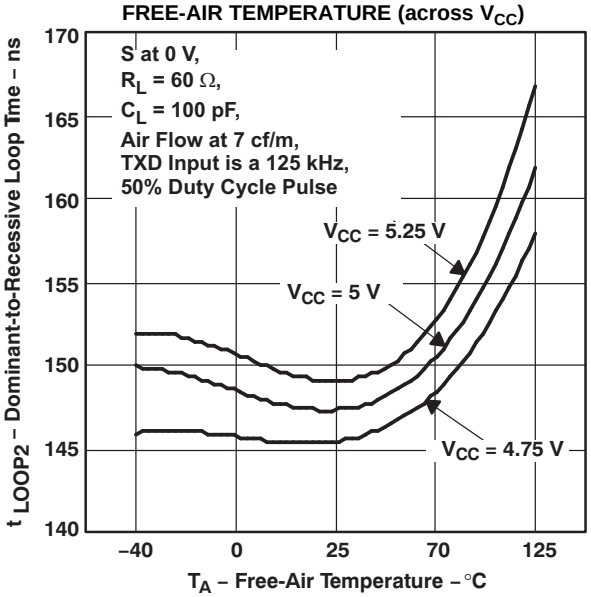


Figure 16.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE

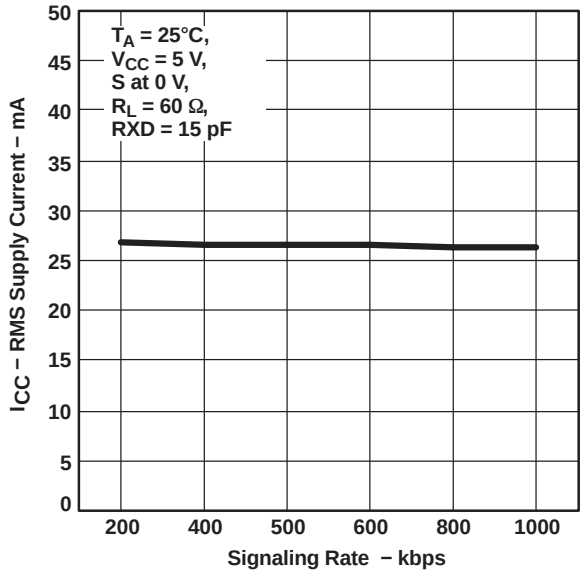


Figure 17.

DRIVER LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

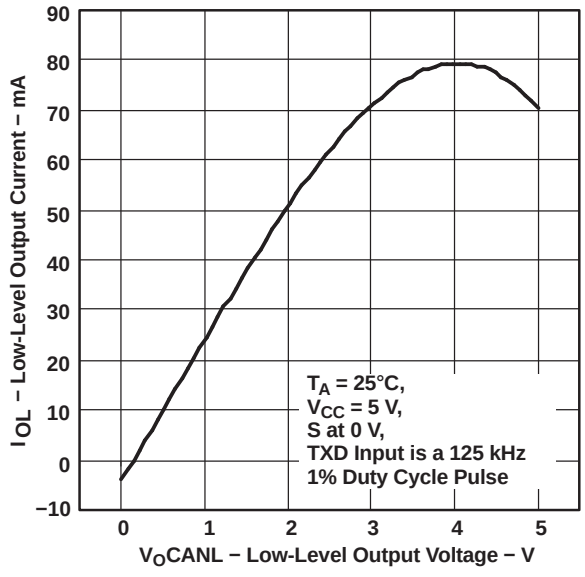


Figure 18.

TYPICAL CHARACTERISTICS (continued)

DRIVER HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

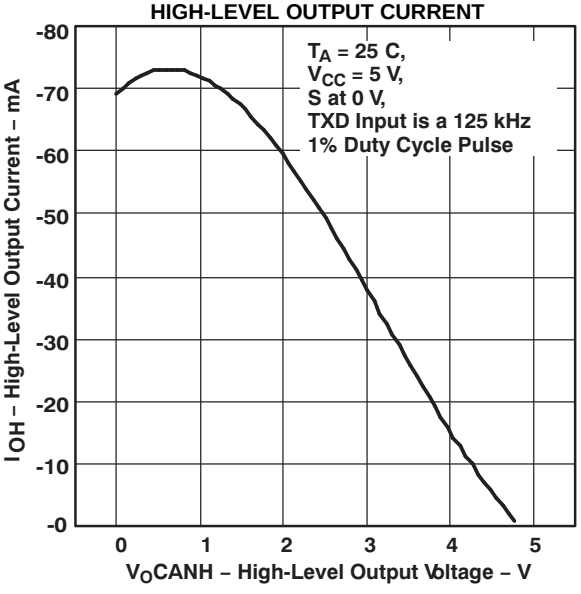


Figure 19.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE (across V_{CC})

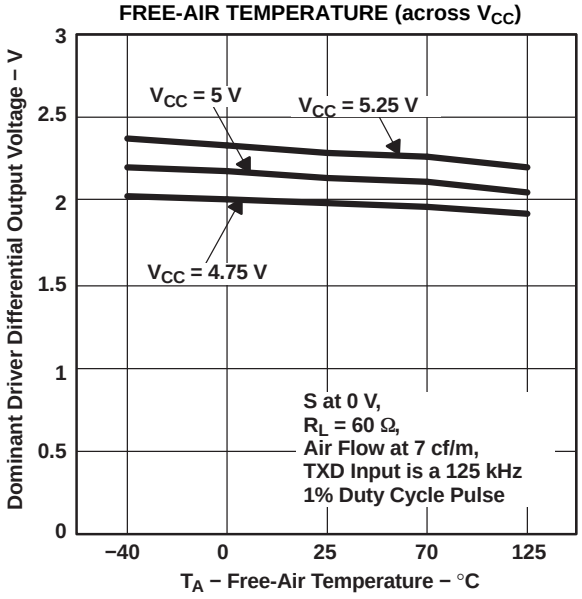


Figure 20.

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

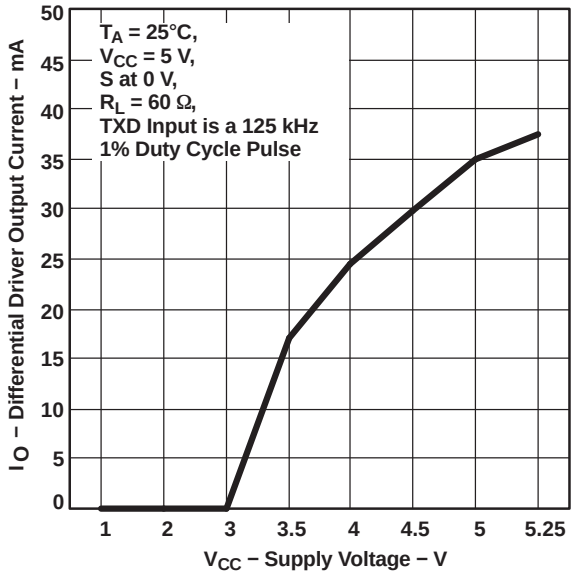


Figure 21.

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

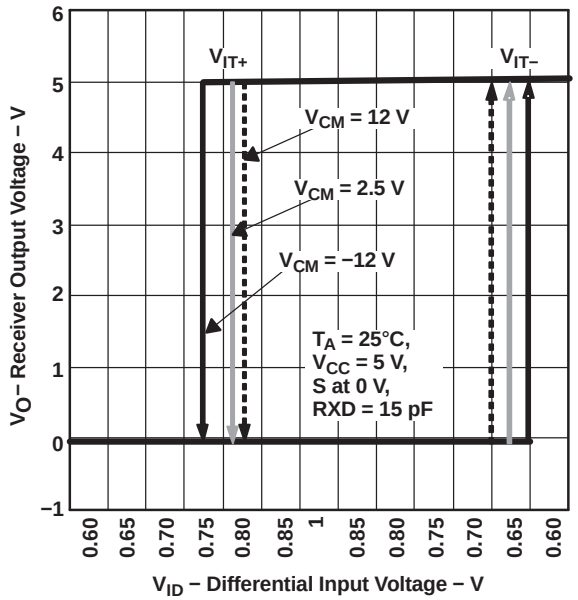


Figure 22.

TYPICAL CHARACTERISTICS (continued)

TYPICAL ELECTROMAGNETIC EMISSIONS UP TO 50 MHZ (Peak Amplitude)

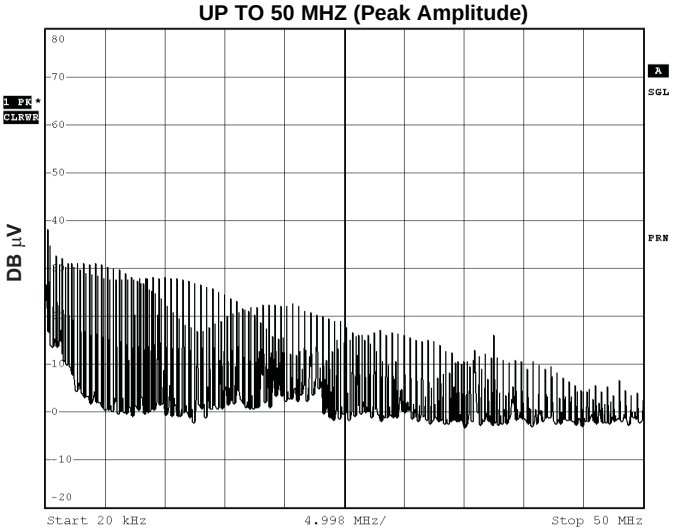


Figure 23. Frequency Spectrum of Common-Mode Emissions

TYPICAL ELECTROMAGNETIC IMMUNITY PERFORMANCE

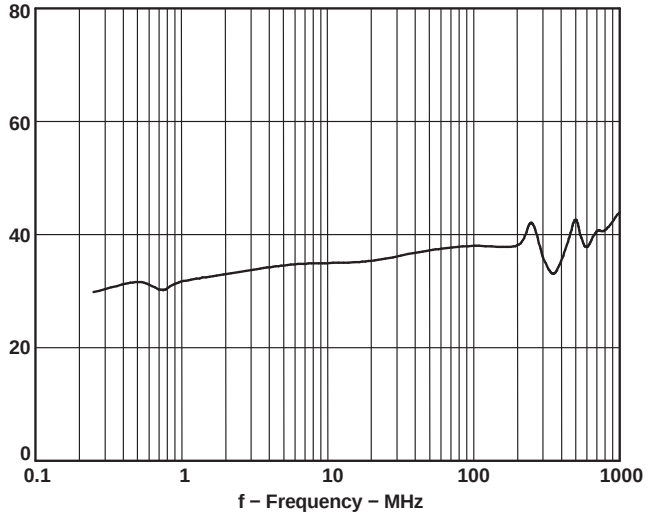


Figure 24. Direct Power Injection (DPI) Response vs Frequency

APPLICATION INFORMATION

CAN Basics

The basics of arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this “sample” is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the approximately 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system also need to be accounted for with adjustments in signaling rate and stub and bus length. Table 7 lists the maximum signaling rates achieved with the SN65HVD1040 with several bus lengths of category 5, shielded twisted pair (CAT 5 STP) cable.

Table 7. Maximum Signaling Rates for Various Cable Lengths

Bus Length (m)	Signaling Rate (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

The ISO 11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A large number of nodes requires a transceiver with high input impedance such as the HVD1040.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the standard should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard’s –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity. The HVD1040 enhances the Standard’s insurance of data integrity with an extended –12 V to 12 V range of common-mode operation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1040HD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-4-260C-72 HR	-55 to 175	H1040	Samples
SN65HVD1040SHKQ	ACTIVE	CFP	HKQ	8	25	TBD	AU	N / A for Pkg Type	-55 to 210	HVD1040S HKQ	Samples
SN65HVD1040SKGD3	ACTIVE	XCEPT	KGD	0	210	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

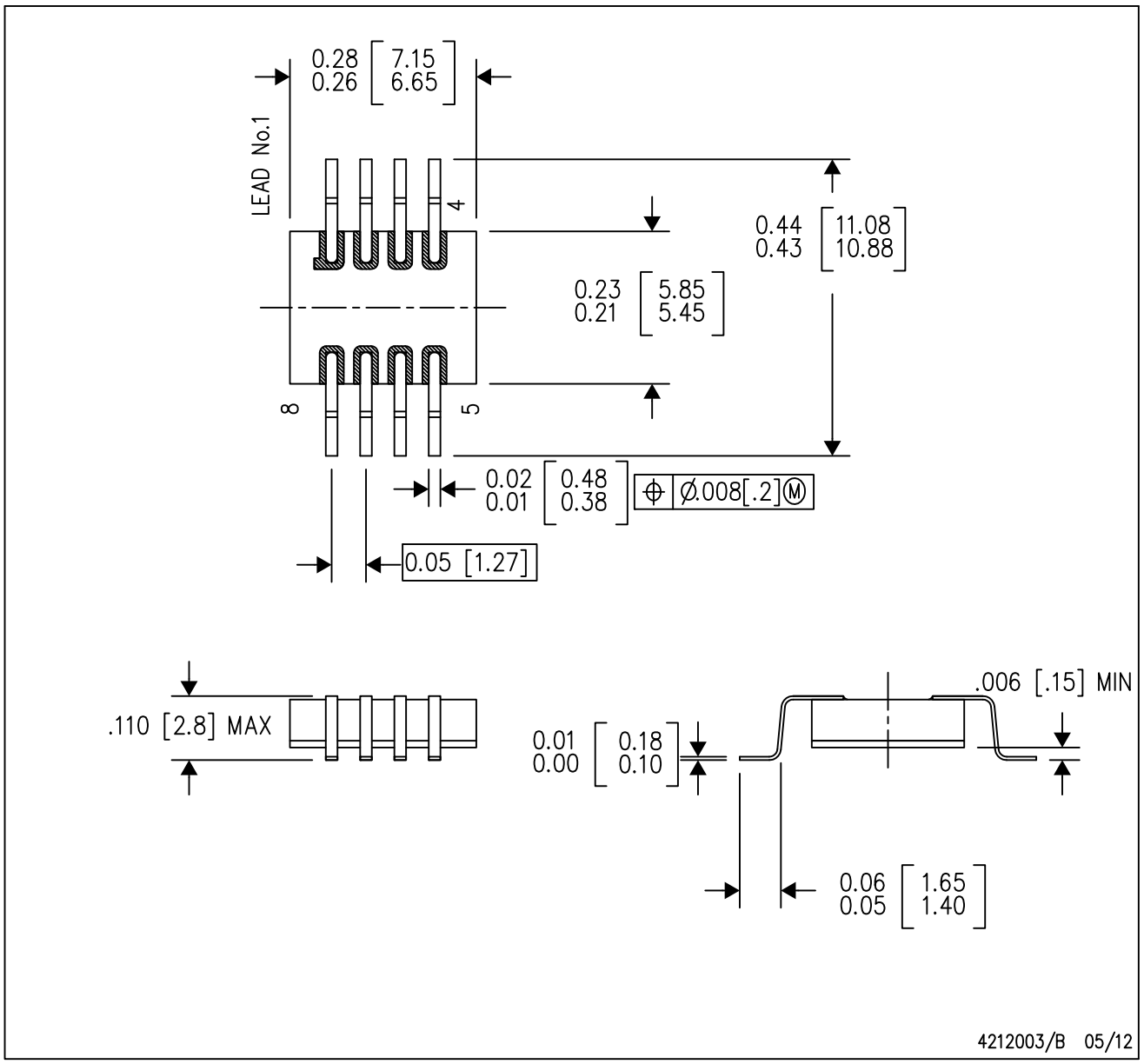
OTHER QUALIFIED VERSIONS OF SN65HVD1040-HT :

- Catalog: SN65HVD1040
- Automotive: SN65HVD1040-Q1

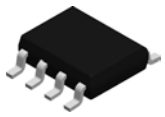
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

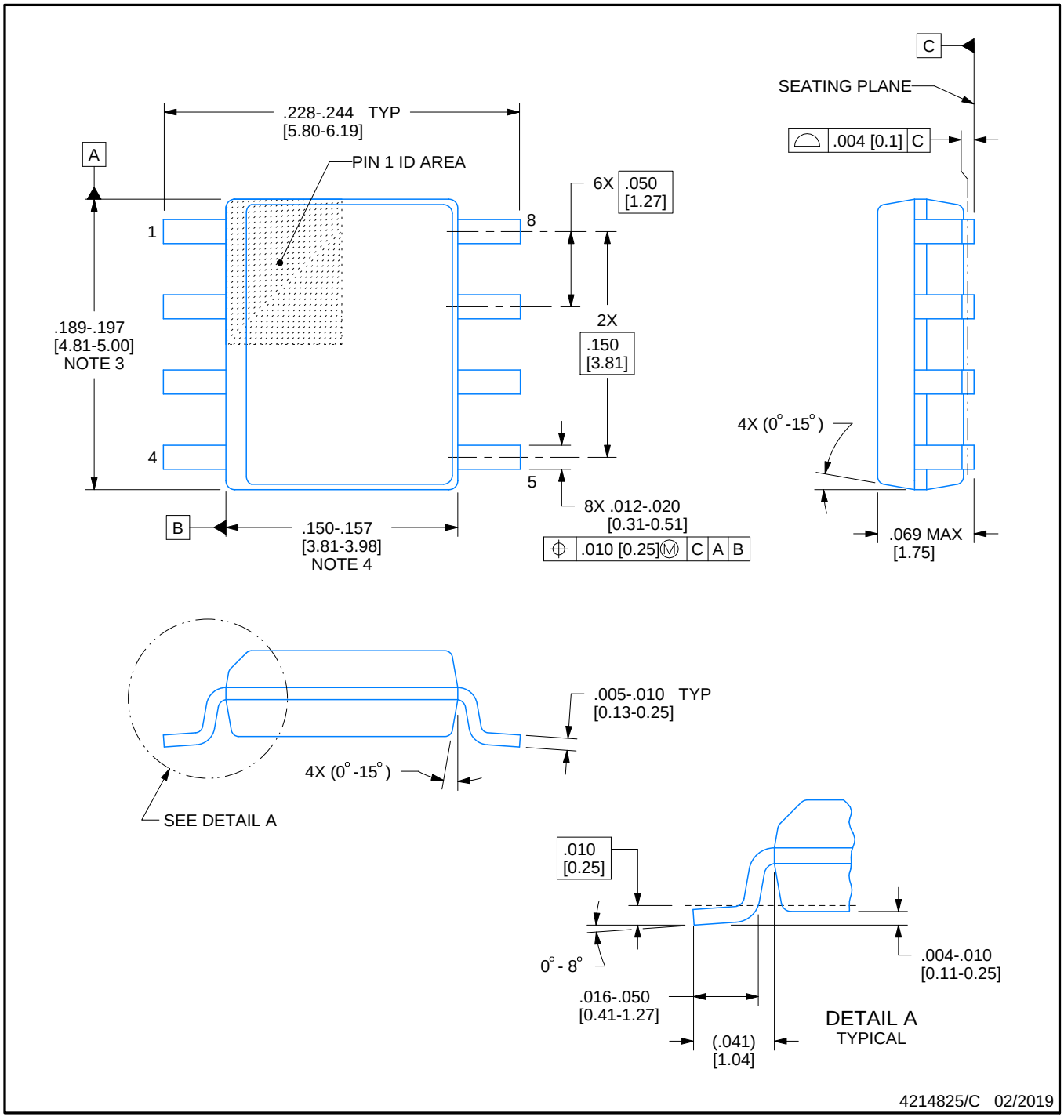


PACKAGE OUTLINE

D0008A

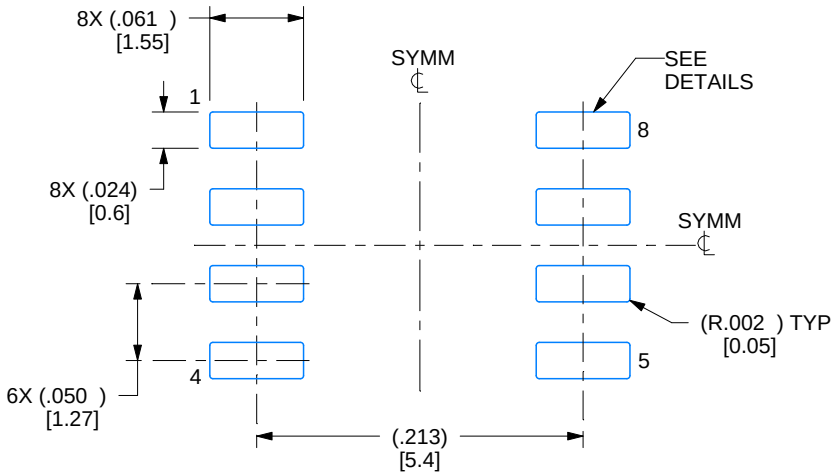
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

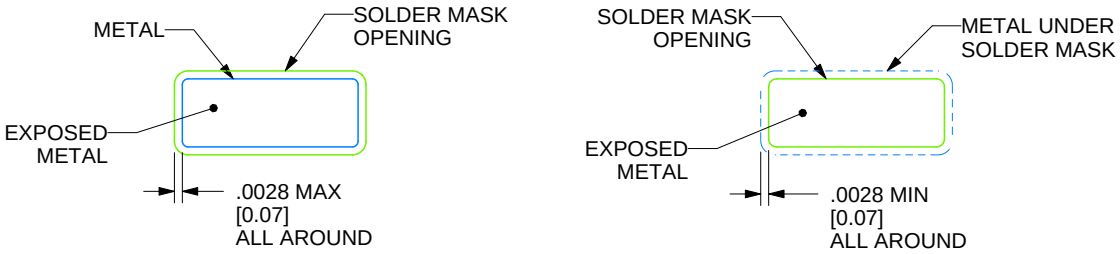


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

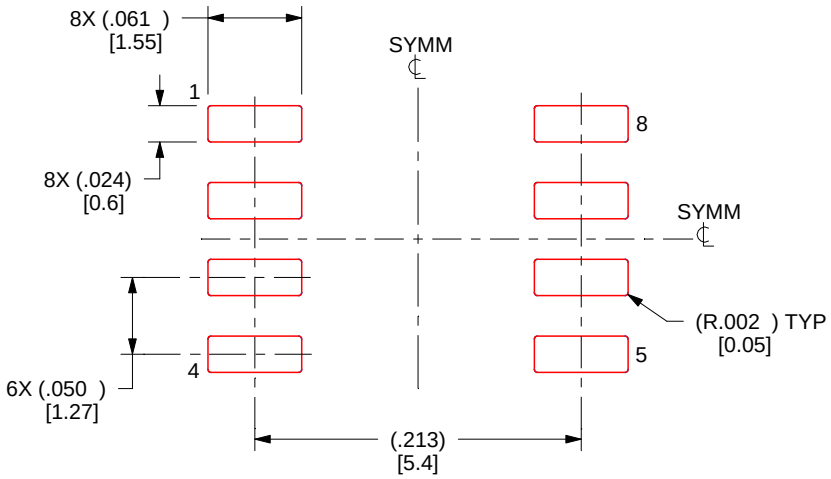
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265