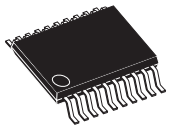
STPM01

Programmable single phase energy metering IC with tamper detection

Features

- Active, reactive, apparent energies and RMS values
- Ripple free active energy pulsed output
- Live and neutral monitoring for tamper detection
- Easy and fast digital calibration in only one point over the whole current range
- OTP for calibration and configuration
- Integrated linear VREGs for digital and analog supply
- Selectable RC or crystal oscillator
- Support 50 ÷ 60 Hz – IEC62052-11, IEC62053-2x specification
- Less than 0.1 % error
- Precision voltage reference: 1.23 V and 30 ppm/°C max



TSSOP20

Description

The STPM01 is designed for effective measurement of active, reactive and apparent energy in a power line system using Rogowski coil, current transformer and shunt sensors. This device can be implemented as a single chip monophase energy meter or as a peripheral measurement in a microcontroller based monophase or 3-phase energy meter. The STPM01 consists, essentially, of two parts: the analog part and the digital part. The former, is composed by preamplifier and 1st order $\Delta\sum$ A/D converter blocks, band gap voltage reference, low drop voltage regulator, the latter, is composed by system control, oscillator, hard wired DSP and SPI interface. There is also an OTP block, which is controlled through the SPI by means of a dedicated command set. The configured bits are used for testing, configuration and calibration purpose. From a pair of $\Delta\sum$ output signals coming from analog section, a DSP unit computes the amount of consummated active, reactive and apparent energy, RMS and instantaneous values of voltage and current. The results of computation are available as pulse frequency and states on the digital outputs of the device or as data bits in a data stream, which can be read from the device by means of SPI interface. This system bus interface is used also during production testing of the device and/or for temporary or permanent programming of bits of internal OTP. In the STPM01 an output signal with pulse frequency proportional to energy is generated, this signal is used in the calibration phase of the energy meter application allowing a very easy approach. When the device is fully configured and calibrated, a dedicated bit of OTP block can be written permanently in order to prevent accidental entering into some test mode or changing any configuration bit.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STPM01FTR	- 40 to 85 °C	TSSOP20 (tape and reel)	2500 parts per reel

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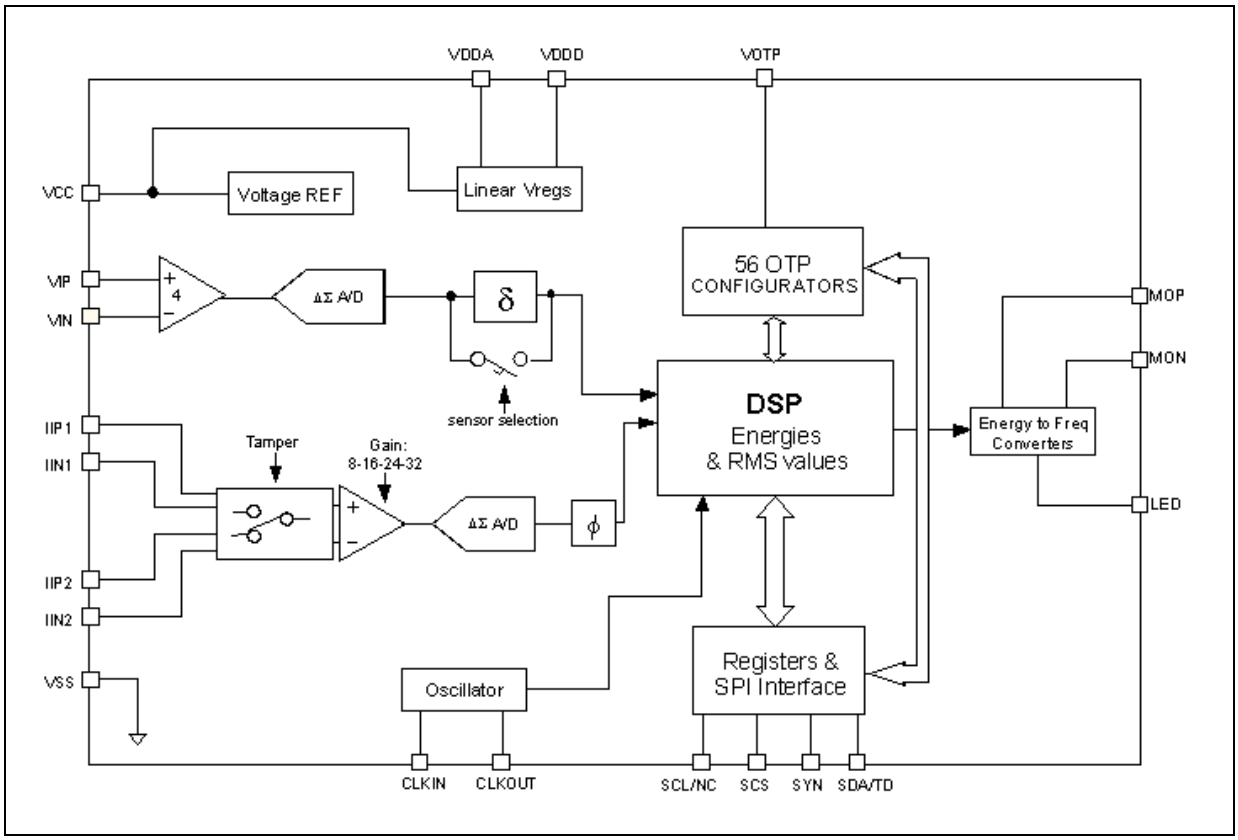
1 Schematic diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

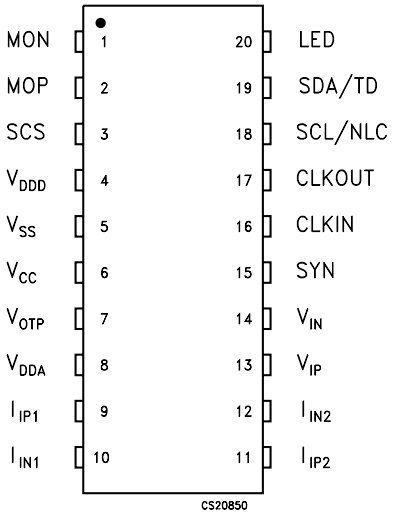


Table 2. Pin description

Pin n°	Symbol	Type (1)	Name and function
1	MON	P O	Programmable output pin, see *Table 5*
2	MOP	P O	Programmable output pin, see *Table 5*
3	SCS	D IN	Digital input/output pin, see *Table 5*
4	V_{DDD}	A OUT	1.5 V Output of internal low drop regulator which supplies the digital core
5	V_{SS}	GND	Ground
6	V_{CC}	P IN	Supply voltage
7	V_{OTP}	P INr	Supply voltage for OTP cells
8	V_{DDA}	A OUT	3 V Output of internal low drop regulator which supplies the analog part
9	I_{IP1}	A IN	Positive input of primary current channel
10	I_{IN1}	A IN	Negative input of primary current channel
11	I_{IP2}	A IN	Positive input of secondary current channel
12	I_{IN2}	A IN	Negative input of secondary current channel
13	V_{IP}	A IN	Positive input of voltage channel
14	V_{IN}	A IN	Negative input of voltage channel
15	SYN	D I/O	Programmable input/output pin, see *Table 5*
16	CLKIN	A IN	Crystal oscillator input or resistor connection if RC oscillator is selected
17	CLKOUT	A OUT	Oscillator Output (RC or crystal)
18	SCL/NLC	D I/O	Programmable input/output pin, see *Table 5*
19	SDA/TD	D I/O	Programmable input/output pin, see *Table 5*
20	LED	D O	Programmable output pin, see *Table 5*

1. A: Analog, D: Digital, P: Power

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Input voltage	-0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	± 150	mA
V_{ID}	Input voltage at digital pins (SCS, MOP, MON, SYN, SDATD, SCLNLC, LED)	-0.3 to V_{CC} + 0.3	V
V_{IA}	Input voltage at analog pins (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})	-0.7 to 0.7	V
V_{OTP}	Input voltage at OTP pin	-0.3 to 25	V
ESD	Human body model (all pins)	± 3.5	kV
T_{OP}	Operating ambient temperature	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature range	- 55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	114.5 (1)	°C/W

1. This value is referred to single-layer PCB, JEDEC standard test board.

4 Functions

Table 5. Programmable pin functions

Programmable pin	Stand-alone mode (APL register=2 or 3)	Peripheral mode (APL register=0 or 1)
MON	Output for Stepper's node (MB)	If APL=0 then Watchdog signal. If APL=1 then $\Delta\Sigma$ signal of current channel
MOP	Output for Stepper's node (MA)	If APL=0 then ZCR If APL=1 then $\Delta\Sigma$ signal of voltage channel
LED	If APL=2 then LED provides high frequency pulses proportional to Active Energy with 50% duty cycle. If APL=3 then LED provides pulses proportional to Active Energy (internal signal AW). The number of pulses per kWh can be selected according to the value of KMOT configuration bit.	If APL=0 then LED can provide Active, Reactive or Apparent Energy according to value of KMOT configuration bit. If APL=1 then LED is connected to the MUX signal generated from the tamper detection circuit. When LED=low then the primary current channel is selected, if LED=high the secondary current channel is selected.
SCLNLC	No-load indicator: when low, a no-load condition is detected	Used for SPI interface (see SPI interface section for details)
SDATD	Tamper indicator: when low tamper condition is detected	
SYN	Negative active power indicator: when low a negative active power condition is detected	
SCS	Must be high to activate SCLNLC, SDATAD and SYN indications	

Table 6. Internal signal description

Symbol	Name	Description
ZCR	Zero crossing signal	Provides positive pulse every time the line voltage crosses zero
AW	Active energy	Pulse frequency signal proportional to active energy
RW	Reactive energy	Pulse frequency signal proportional to reactive energy
SW	Apparent energy	Pulse frequency signal proportional to apparent energy
LIN	Line frequency signal	This signal is high when the voltage channel value is rising and it is low when the voltage channel is falling. Basically this signal is the sign of dv/dt.
BFR	Base frequency range	This signal is high when either the voltage line frequency is outside the nominal band or the voltage register is below 64. It is cleared when the voltage line frequency is inside the nominal band and the voltage register goes above 128.
MA	Stepper motor signals	Signal available in MOP and MON to drive a stepper motor
MB		
BIT	Tamper flag	This signal provides the information on the tamper status. If low no tamper is detected, when high a tamper condition has been detected. This signal is part of the status register but is also available on the SDATD pin when in standalone mode.
BIL	No load condition	Provides information on the load condition. This signal is part of the status register but is also available on the SCLNLC pin when in standalone mode. BIL=1 no load condition, BIL=0 normal operation.

5 Electrical characteristics

V_{CC} = 5 V, T_A = 25 °C, 100 nF to 1 uF between V_{DDA} and V_{SS}, 100 nF to 1 uF between V_{DDD} and V_{SS}, 100 nF to 1 uF between V_{CC} and V_{SS} unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Energy measurement accuracy						
f_{BW}	Effective bandwidth	Limited by digital filtering	5		400	Hz
e_{AW}	Accuracy of active power	Over 1 to 1000 of dynamic range		0.1		%
e_{RW}	Accuracy of reactive power	Over 1 to 1000 of dynamic range		0.1		%
e_{SW}	Accuracy of apparent power	Over 1 to 500 of dynamic range		0.1		%
SNR	Signal to noise ratio	Over the entire bandwidth		52		db
$PSRR_{DC}$	Power supply DC rejection	Voltage signal: 200 mV_{rms}/50Hz Current signal: 10 mV_{rms}/50Hz f_{CLK}= 4.194 MHz V_{CC}=3.3V±10%, 5V±10%			0.2	%
$PSRR_{AC}$	Power supply AC rejection	Voltage signal: 200 mV_{rms}/50Hz Current signal: 10 mV_{rms}/50Hz f_{CLK}= 4.194 MHz V_{CC}=3.3V+0.2V_{rms}1@100Hz V_{CC}=5.0V+0.2V_{rms}1@100Hz			0.1	%
General section						
V_{CC}	Operating supply voltage		3.165		5.5	V
I_{CC}	Supply current configuration registers cleared or device locked (TSTD=1)	4 MHz, V_{CC} = 5V		3	4	mA
		8 MHz, V_{CC} = 5V		5	6	
ΔI_{CC}	Increase of supply current per configuration bit, during programming	4 MHz, V_{CC} = 5V		120		µA/bit
	Increase of supply current per configuration bit with device locked	4 MHz, V_{CC} = 5V		2		
POR	Power on reset on V_{CC}			2.5		V
V_{DDA}	Analog supply voltage		2.85	3.0	3.15	V
V_{DDD}	Digital supply voltage		1.425	1.50	1.575	V
f_{CLK}	Oscillator clock frequency	MDIV bit = 0	4.000		4.194	MHz
		MDIV bit = 1	8.000		8.192	MHz
f_{LINE}	Nominal line frequency		45		65	Hz
V_{OTP}	OTP programming voltage		14		20	V

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{OTP}	OTP programming current per bit				2.5		mA
t_{OTP}	OTP programming time per bit			100		300	µs
I_{LATCH}	Current injection latch-up immunity					300	mA
Analog Inputs (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})							
V_{MAX}	Maximum input signal levels	Voltage channel		-0.3		0.3	V
		Current channels	Gain 8X	-0.15		0.15	V
			Gain 16X	-0.075		0.075	
			Gain 24X	-0.05		0.05	
			Gain 32X	-0.035		0.035	
f_{ADC}	A/D Converter bandwidth				10		kHz
f_{SPL}	A/D Sampling frequency				$F_{CLK}/4$		Hz
V_{OFF}	Amplifier offset					±20	mV
Z_{IP}	V_{IP}, V_{IN} Impedance	Over the total operating voltage range		100		400	kΩ
Z_{IN}	V_{IP1}, V_{IN1}, V_{IP2}, V_{IN2} Impedance	Over the total operating voltage range			100		kΩ
G_{ERR}	Current channels gain error				±10		%
I_{VL}	Voltage channel leakage current			-1		1	µA
I_{LEAK}	Current channel leakage current	Channel disabled (PST=0 to 3; CH2 disabled if C_{SEL}=0; CH1 disabled if C_{SEL}=1) or device off		-1		1	µA
		Input enabled		-10		10	
Digital I/O Characteristics (SDA, CLKIN, CLKOUT, SCS, SYN, LED)							
V_{IH}	Input high voltage	SDA, SCS, SYN, LED		$0.75V_{CC}$			V
		CLKIN		1.5			
V_{IL}	Input low voltage	SDA, SCS, SYN, LED				$0.25V_{CC}$	V
		CLKIN				0.8	
V_{OH}	Output high voltage	I_O = -2mA		V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O = +2mA				0.4	V
I_{UP}	Pull up current				15		µA
t_{TR}	Transition time	C_{LOAD} = 50pF			10		ns
Power I/O Characteristics (MOP, MON)							
V_{OH}	Output high voltage	I_O = -14mA		V_{CC}-0.5			V
V_{OL}	Output low voltage	I_O = +14mA				0.5	V
t_{TR}	Transition time	C_{LOAD} = 50pF		5	10		ns

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal oscillator (see circuit *Figure 20*)						
I_I	Input current on CLKIN				1	µA
R_P	External resistor		1		4	MΩ
C_P	External capacitors			22		pF
f_{CLK}	Nominal output frequency		4	4.194		MHz
			8	8.192		
RC oscillator (see circuit *Figure 20*)						
I_{CLKIN}	Settling current	f_{CLK}= 4 MHz	40		60	µA
R_{SET}	Settling resistor			12		kΩ
t_{JIT}	Frequency jitter			1		ns
On chip reference voltage						
V_{REF}	Reference voltage			1.23		V
	Reference accuracy			±1		%
T_C	Temperature coefficient	After calibration		30	50	ppm/ °C
SPI interface timing						
F_{SCLKr}	Data read speed				32	MHz
F_{SCLKw}	Data write speed				100	kHz
t_{DS}	Data setup time		20			ns
t_{DH}	Data hold time		0			ns
t_{ON}	Data driver on time				20	ns
t_{OFF}	Data driver off time				20	ns
t_{SYN}	SYN active width		$2/f_{CLK}$			s

6 Terminology

6.1 Measurement error

The error associated with the energy measurement made by the STPM01 is defined as:

Percentage error = [STPM01 (reading) - true energy] / true energy

6.2 ADC offset error

This is the error due to the DC component associated with the analog inputs of the A/D converters. Due to the internal automatic DC offset cancellation the STPM01 measurement is not affected by DC components in voltage and current channel. The DC offset cancellation is implemented in the DSP.

6.3 Gain error

The gain error is gain due to the signal channel gain amplifiers. This is the difference between the measured ADC code and the ideal output code. The difference is expressed as percentage of the ideal code.

6.4 Power supply DC and AC rejection

This parameter quantifies the STPM01 measurement error as a percentage of reading when the power supplies are varied. For the PSRRAC measurement, a reading at two nominal supplies voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when an ac (200 mV_{RMS}/100 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading.

For the PSRRDC measurement, a reading at two nominal supplies voltages (3.3 and 5V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ± 10 %. Any error introduced is again expressed as a percentage of the reading.

6.5 Conventions

The lowest analog and digital power supply voltage is named V_{SS} which represent the system ground (GND). All voltage specifications for digital input/output pins are referred to GND.

Positive currents flow into a pin. Sinking current means that the current is flowing into the pin and then it is positive. Sourcing current means that the current is flowing out of the pin and then it is negative.

Timing specifications of signal treated by a digital control part are relative to CLKOUT. This signal is provided from the crystal oscillator of 4.194 MHz nominal frequency or from the internal RC oscillator, eventually an external source of 4.194 MHz or 8.192 MHz can be used.

Timing specifications of signals of the SPI interface are relative to the SCLNLC, there is no direct relationship between the clock (SCLNLC) of the SPI interface and the clock of the DSP block. A positive logic convention is used in all equations.

7 Typical performance characteristics

Figure 3. Supply current vs. supply voltage, T_A = 25 °C

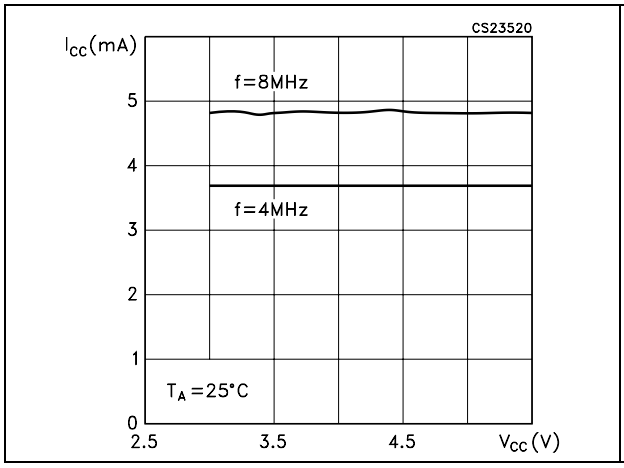


Figure 4. RC oscillator frequency vs. V_{CC}, R = 12 kΩ, T_A = 25 °C

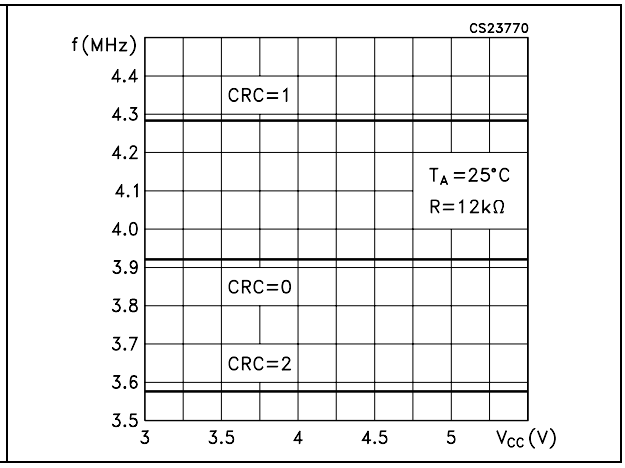


Figure 5. RC oscillator: frequency jitter vs. temperature

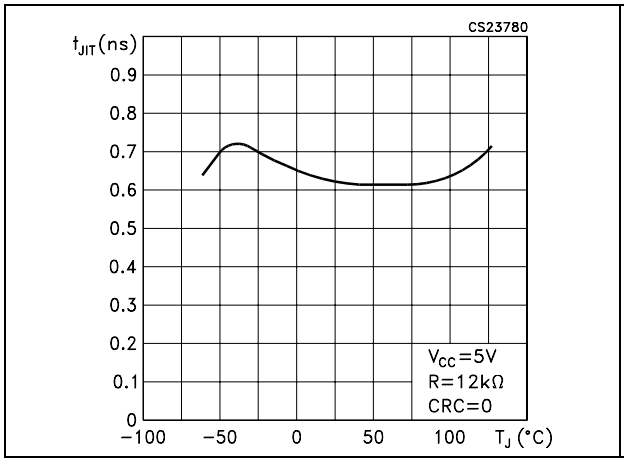


Figure 6. Analog voltage regulator: line - load regulation

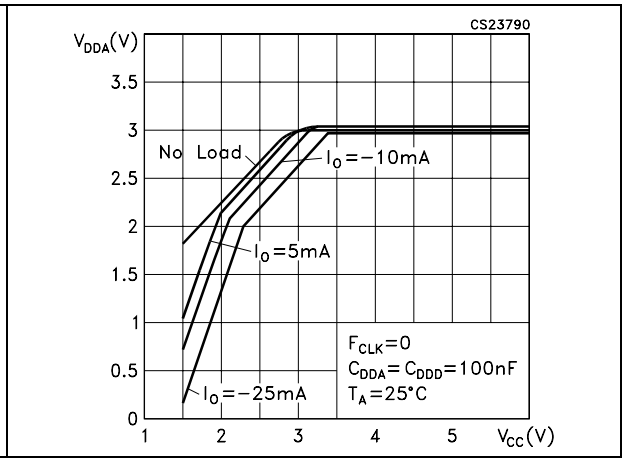


Figure 7. Digital voltage regulator: line - load regulation

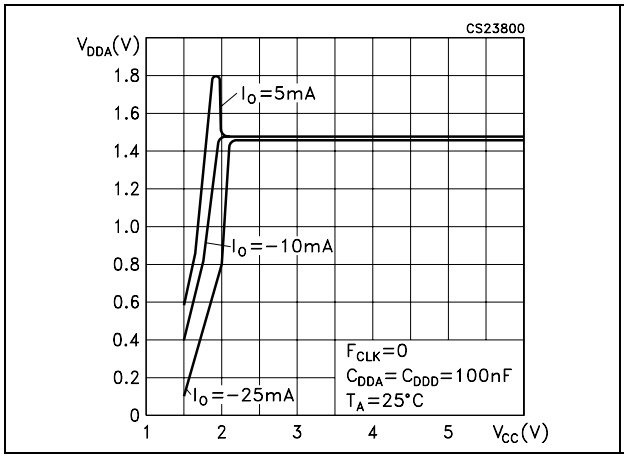


Figure 8. Voltage channel linearity at different V_{CC} voltages

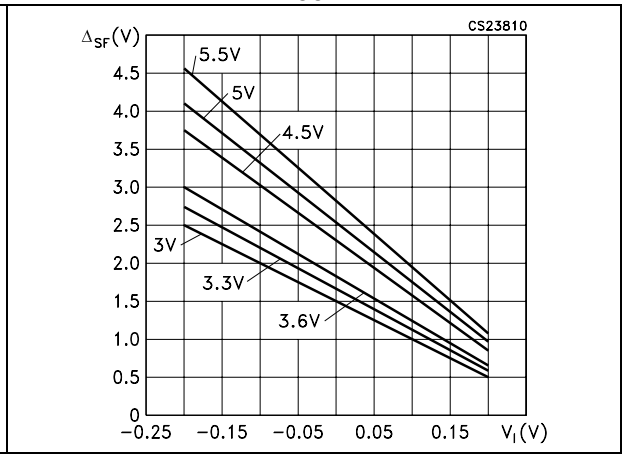


Figure 9. Power supply AC rejection vs. V_{CC}

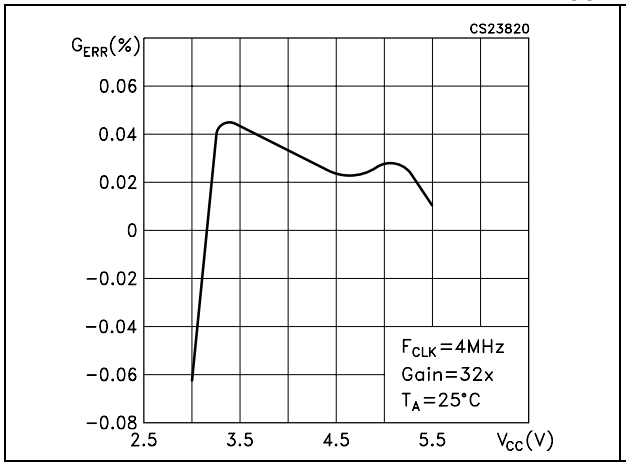


Figure 10. Power supply DC rejection vs. V_{CC}

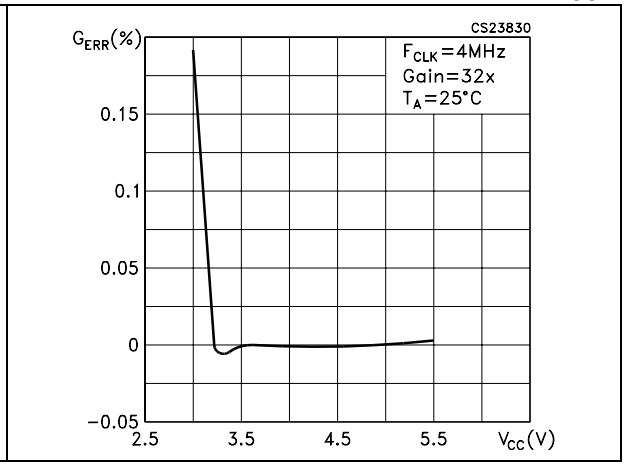


Figure 11. Error over dynamic range gain dependence

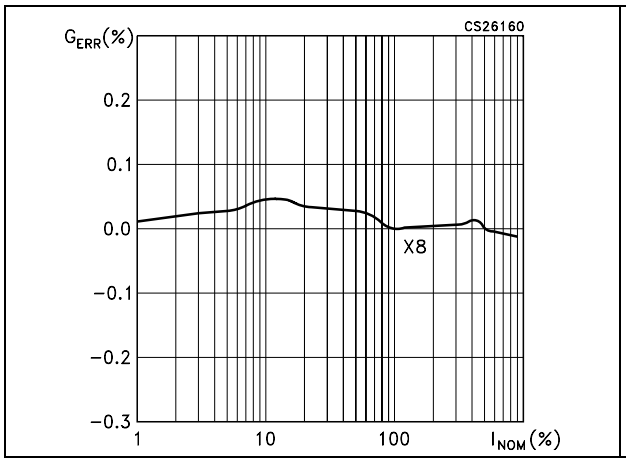


Figure 12. Primary current channel linearity at different V_{CC}

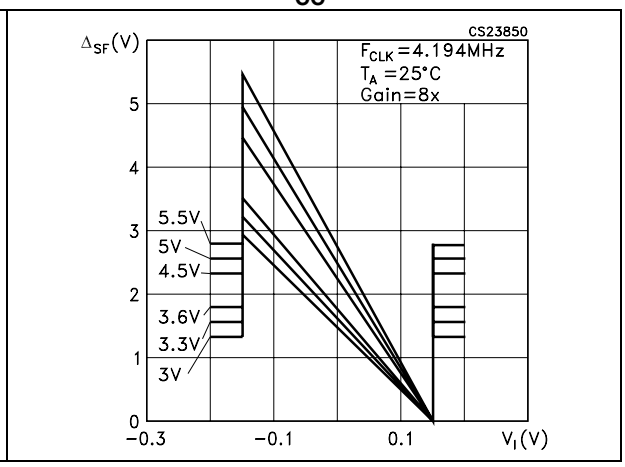
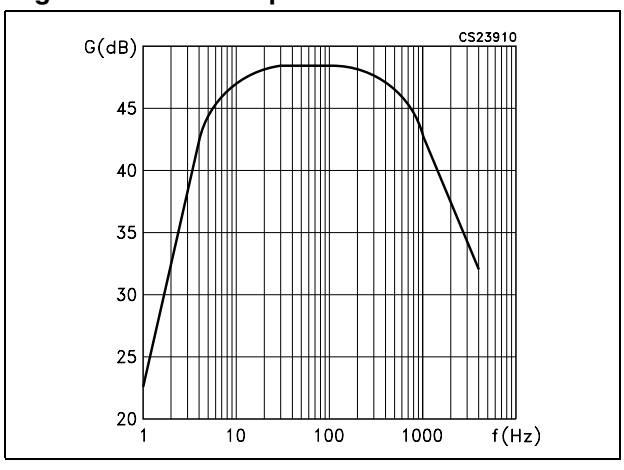


Figure 13. Gain response of ΔΣ AD converters



8 Theory of operation

8.1 General operation description

The STPM01 is able to perform active, reactive and apparent energy measurements, RMS and instantaneous values for voltage and current, line frequency information.

Most of the functions are fully programmable using internal configuration bits accessible through SPI interface. The most important configuration bits are the two application bits (APL - see *Table 16* for configuration register). Using these bits the STPM01 can be programmed as peripheral (APL = 0 or APL = 1) in microcontroller based meter systems or as standalone meter device (APL = 2 or APL = 3).

In standalone mode, the STPM01 is able to drive a stepper motor with the MOP and MON pins, while some of the SPI pins (see *Table 5*) are used to provide information on tamper, no load and negative power.

In peripheral mode, due to the fact that the stepper motor is not used, the MOP and MON pins are used to provide different information (see *Table 5*), while the SPI pins are used to communicate with the microcontroller.

The STPM01 includes internal registers that hold the useful information for the meter system. Two kinds of active energy are available: the total active energy that includes all harmonic content called type 0 and the active energy limited to the 1st harmonic called type 1. This last energy value is obtained filtering the type 0 active energy. The resolution of both the two active energies is 20-bit. Reactive and Apparent energies are also available with a 20-bit resolution.

STPM01 provides also the RMS values of voltage and current. Due to the modest dynamic variation of the voltage, the RMS value is stored with a resolution of 11 bit. While the RMS current value has a resolution of 16 bit. The momentary sampled value of voltage and current are available also with a resolution of 11 and 16 bit respectively. The line frequency value is stored with a resolution of 14 bits.

Due to the proprietary energy computation algorithm, STPM01 calibration is very easy and fast allowing calibration in only one point over the whole current range. The calibration parameters are stored permanently in the OTP (one time programmable) cells, preventing calibration tampering.

8.2 Analog inputs

Input amplifiers

The STPM01 has one fully differential voltage input channel and two fully differential current input channels.

The voltage channel consists of a differential amplifier with a gain of 4. The maximum differential input voltage for the voltage channel is ± 0.3 V.

The two current channels are multiplexed (see tamper section for details) to provide a single input to a preamplifier with a gain of 4. The output of this preamplifier is connected to the input of a programmable gain amplifier (PGA) with possible gain selections of 2, 4, 6, 8. The total gain of the current channels are then 8, 16, 24, 32. The gain selections are made by writing to the gain register and it can be different for the two current channels. In case the tamper function is not used, the secondary current can be disabled.

The maximum differential input voltage is dependent on the selected gain according to the following table.

Table 8. Gain of voltage and current channels

Voltage channels		Current channels	
Gain	**Max Input voltage (V)**	**Gain**	**Max input voltage (V)**
4	±0.30	8X	±0.15
		16X	±0.075
		24X	±0.05
		32X	±0.035

The gain register is included in the device configuration register with the address names PST and ADDG. The table below shows the gain configuration according to the register values:

Table 9. Configuration of current sensors

Primary		Secondary		Configuration Bits	
Gain	**Sensor**	**Gain**	**Sensor**	**PST (3 bits)**	**ADDG (1 bit)**
8	Rogowsky Coil	Disabled (No Tamper)		0	0
16				0	1
24				1	0
32				1	1
8	CT			2	X
32	Shunt			3	X
8	Rogowsky Coil	8	Rogowsky Coil	4	0
16		16		4	1
24		24		5	0
32		32		5	1
8	CT	8	CT	6	X
8		32	Shunt	7	X

Note: If the device is used in configuration PST = 7 (primary channel with CT, secondary channel with Shunt), the shunt Ks must always be equal to one fourth of the current transformer Ks.

Both the voltage and current channels implement an active offset correction architecture which gives the benefit to avoid any offset compensation.

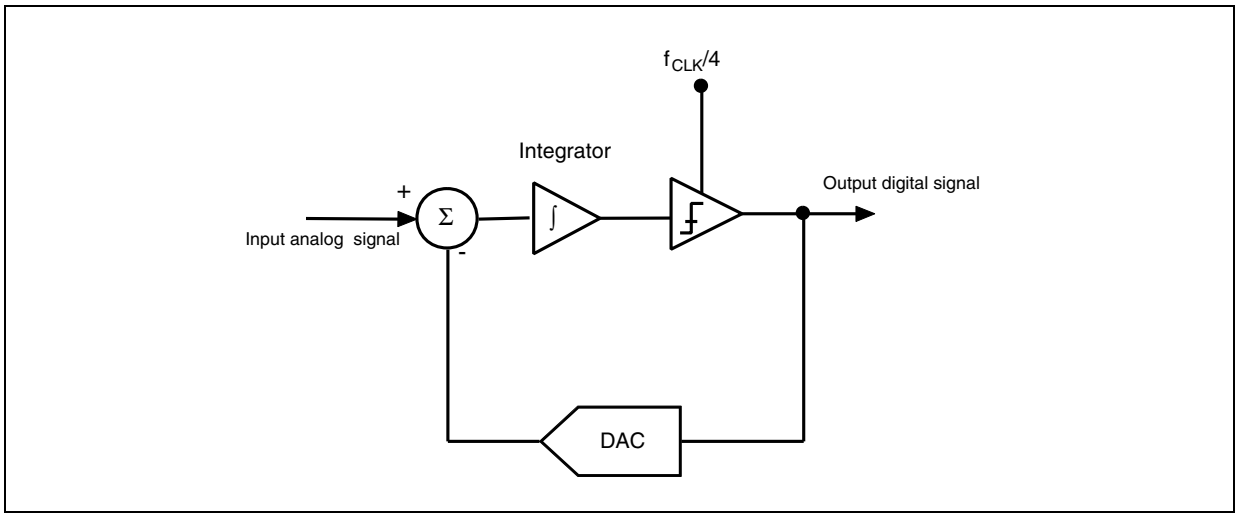
The analog voltage and current signals are processed by the $\sum \Delta$ Analog to digital converters that feed the hardwired DSP. The DSP implements an automatic digital offset cancellation that make possible avoiding any manual offset calibration on the analog inputs.

8.3 ∑Δ A/D converters

The analog to digital conversion in the STPM01 is carried out using two first order ∑ Δ converters. The device performs A/D conversions of analog signals on two independent channels in parallel. The current channel is multiplexed as primary or secondary current channel in order to be able to perform a tamper function, if it is enabled. The converted ∑ Δ signals are supplied to the internal hardwired DSP unit, which filters and integrates those signals in order to boost the resolution and to yield all the necessary signals for computations.

A ∑ Δ modulator converts the input signal into a continuous serial stream of 1 s and 0 s at a rate determined by the sampling clock. In the STPM01, the sampling clock is equal to $f_{CLK/4}$. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. When a large number of samples are averaged a very precise value of the analog signal is obtained. This averaging is carried out in the DSP section which implements decimation, integration and DC offset cancellation of the supplied ∑ Δ signals. The gain of the decimation filters is 1.004 for the voltage channel and 0.502 for the current channel. The resulting signal has a resolution of 11bits for voltage channel and 16 bits for current channel.

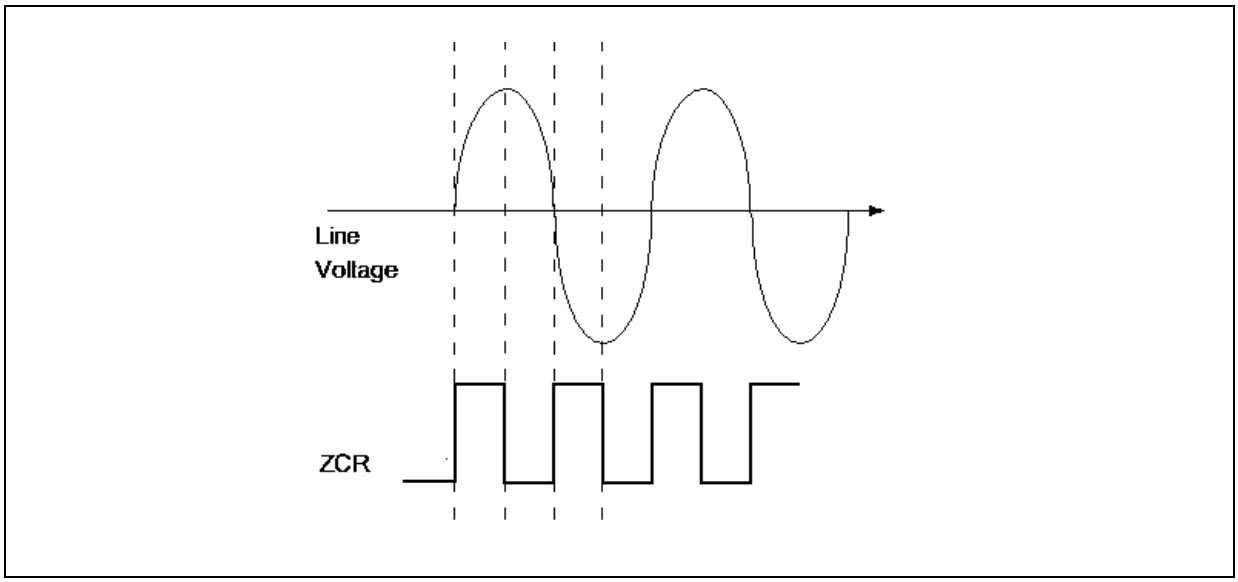
Figure 14. First order ∑ Δ A/D converter



8.4 Zero crossing detection

The STPM01 has a zero crossing detector circuit on the voltage channel which can be used by application for synchronization of some utility equipment to event of zero crossing of line voltage. This circuit produces the internal signal ZCR which has a rising edge every time the line voltage crosses zero and a negative edge every time the voltage reaches its positive or negative peak. The ZCR signal is then at twice the line voltage frequency. The ZCR signal is available on the MOP pin only when STPM01 works as peripheral with the configuration bit APL = 0.

Figure 15. ZCR signal



8.5 Period and line voltage measurement

The period module measures the period of the base frequency of the voltage channel and checks if the voltage signal frequency is within the $f_{CLK}/2^{17}$ to $f_{CLK}/2^{15}$ band. To do this, the LIN signal is produced, which is low when the line voltage is rising, and high when the line voltage is falling. This means that the LIN signal is the sign of dv/dt. With further elaboration, the ZCR signal is also produced. On the trailing edge of LIN (line frequency) the period counter starts counting up pulses of the f_{CLK} /4 reference signal. The LIN signal is available on the status bit register (see *Table 15*).

If the counted number of pulses between two trailing edges of LIN is higher than 2^{15}, or if the counting is never stopped (no LIN trailing edge) this means that the base frequency is lower than $f_{CLK}/2^{17}$ Hz and a BFR (base frequency range) error flag is set.

If the number of pulses counted between two trailing edges of LIN is lower than 2^{13}, the base frequency exceeds the limit (means it is higher than $f_{CLK}/2^{15}$. In this case, the error must be repeated three consecutive times in order to set the BFR error flag.

For example, with a 4.194304 MHz oscillator frequency and MDIV bit clear (or 8.192 MHz with MDIV set), $f_{CLK}/4$ is 1048.576 MHz. If the line frequency is 30 Hz, the counted $f_{CLK}/4$ pulses between two LIN trailing edges are 34952, more than 2^{15} (32768 pulses). The BFR low frequency limit is then:

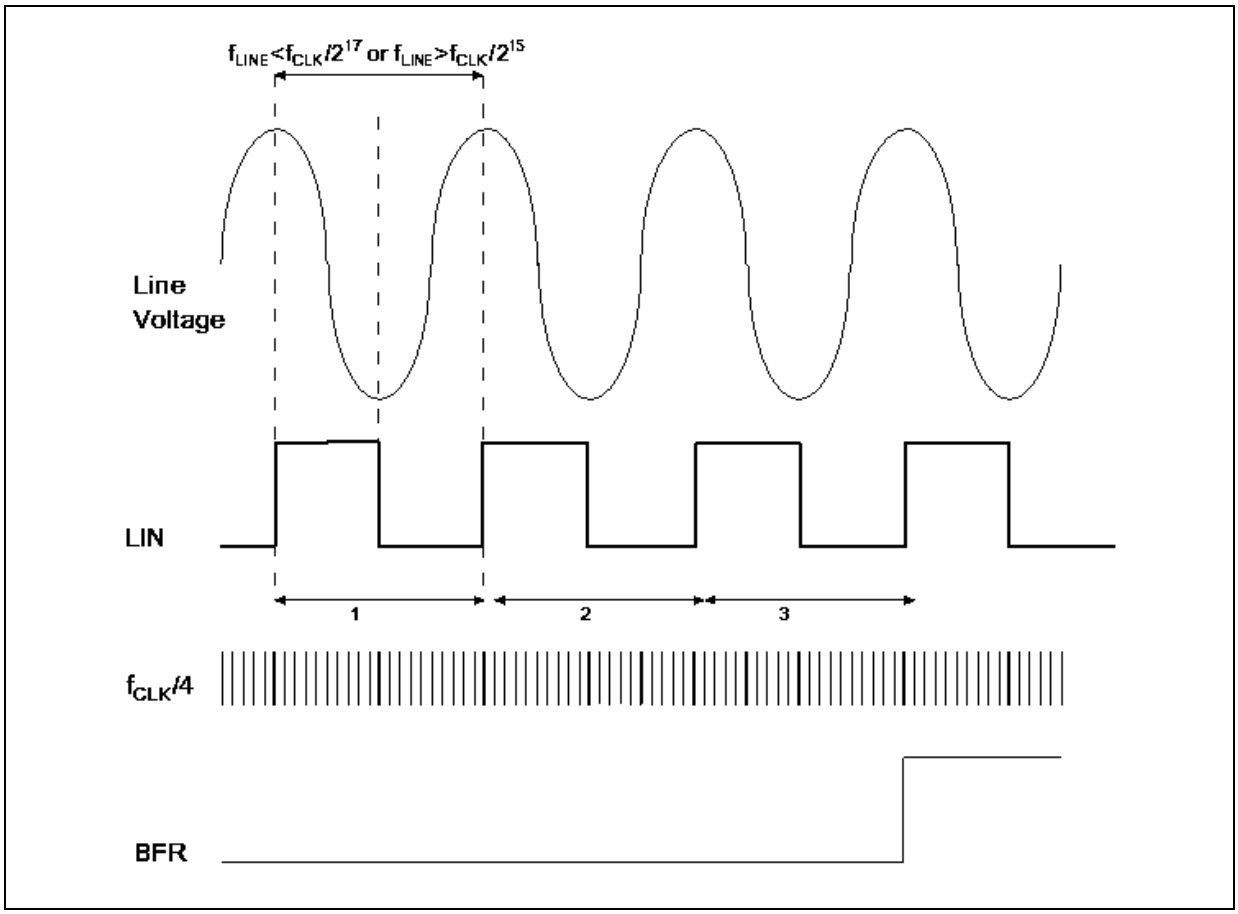
$f_{CLK}/2^{17}$ = 4194304/131072 = 32 Hz.

With the same clock frequency, if the line frequency is 130Hz, the $f_{CLK}/4$ pulses between two LIN trailing edges are 8066, more than 2^{13} (8192). The BFR high frequency limit is then:

$f_{CLK}/2^{15}$ = 4194304/32768 = 128 Hz.

When the line frequency re-enters the nominal band, the BFR flag is automatically reset. This BFR error flag is also assembled as part of the 8-bit status register (see *Table 15*).

Figure 16. LIN and BFR signal



The BFR flag is also set if the register value of the RMS voltage drops below 64. BFR is cleared when the register value goes above 128. The BFR, then, also gives information about the presence of the line voltage within the meter.

When the BFR error is set, the computation of power is zero unless the FRS bit is set or the single wire mode operation is selected (see *Section 8.6*).

In fact, the effect of the BFR bit can be overridden by setting FRS configuration bit.

It means that if FRS is set and BFR is also set, all the energy computation is carried on as BFR was cleared. In this case then p=u*i, where u could be zero or not (if BFR was set because voltage RMS register value is below 64).

In standalone mode, the MOP, MON and LED provide the energy information, their operation is not affected by FRS bit, it means that when BFR is set they stop switching regardless the FRS value.

8.6 Single wire meter mode (only Rogowsky coil sensor)

STPM01 support single wire meter (SWM) operation when working with Rogowsky coil current sensors. In SWM mode there is no available voltage information in the voltage channel. It is possible that someone has disconnected one wire (live or neutral) of the meter

for tampering purposes or in case the line voltage is very stable, it is possible to use a predefined value for computing the energy without sensing it.

In order to enable the SWM mode, the STPM01 must be configured with PST values of 4 or 5, (tamper enabled-Rogowsky coils). In this way, if the BFR error is detected, STPM01 enters in SWM. If BFR is cleared the energy calculation is performed normally, when BFR is set (no voltage information is available) the energy computation is carried out using a nominal voltage value according to the NOM configuration bits.

Since there is no more information on the phase shift between voltage and current, the apparent rather than active power is used for tamper and energy computation. The calculated apparent energy is the product between I_{RMS} (effectively measured) and an equivalent V_{RMS} that can be calculated as follows:

$V_{RMS} = V_{PK}{}^{*}K_{NOM}$,

where V_{PK} represents the maximum line voltage reading of the STPM01 and K_{NOM} is a coefficient that changes according to the following table:

Table 10. Nominal voltage values

NOM	K_{NOM}
0	0.3594
1	0.3906
2	0.4219
3	0.4531

For example, if a R_1 = 783 kΩ and R_2 = 475 Ω are used as resistor divider when the line voltage is present, the positive voltage present at the input of the voltage channel of STPM01 is:

$$VI = \frac{R_2}{R_1 + R_2} \cdot V_{RMS}\sqrt{2}$$

since the maximum voltage value applicable to the voltage channel input of STPM01 is +0.3 V, the equivalent maximum line voltage applicable is:

$V_{PK} = R_1{+}R_2/R_2 \bullet 0.3 = 494.82$

considering the case of NOM=2, the correspondent RMS values used for energy computation are:

$V_{RMS} = V_{PK} \bullet 0.4219 = 208.76$ [V]

Usually the supply voltage for the electronic meter is taken from the line voltage, in SWM, since the line voltage is not present any more, some other power source must be used in order to provide the necessary supply to STPM01 and the other electronic components of the meter.

8.7 Power supply

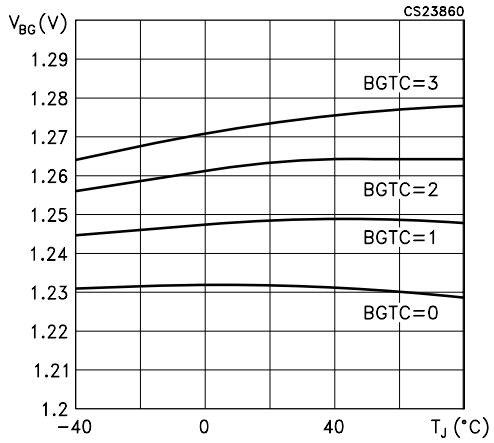
The main STPM01 supply pin is the V_{CC} pin. From the V_{CC} pin two linear regulators provide the necessary voltage for the analog part V_{DDA} (3 V) and for the digital part V_{DDD} (1.5 V). The V_{SS} pin represents the reference point for all the internal signals. 100 nF low ESR

capacitor should be connected between V_{CC} and V_{SS}, V_{DDA} and V_{SS}, V_{DDD} and V_{SS}. All these capacitors must be located very close to the device.

The STPM01 contains a power on reset (POR) detection circuit. If the V_{CC} supply is less than 2.5 V then the STPM01 goes into an inactive state, all the functions are blocked asserting a reset condition. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity to false triggering due to noisy supplies.

A bandgap voltage reference (VBG) of 1.23 V ±1 % is used as reference voltage level source for the two linear regulators and for the A/D converters. Also, this module produces several bias currents and voltages for all other analog modules and for the OTP module. The bandgap voltage can be compensated regardless to the temperature variations with the BGTC bits.

Figure 17. Bandgap temperature variation



8.8 Load monitoring

The STPM01 includes a no load condition detection circuit with adjustable threshold. This circuit monitors the voltage and the current channels and, when the measured voltage is below the set threshold, the internal signal BIL becomes high. The information about this signal is also available in the status bit BIL.

The no load condition occurs when the product between V_{RMS} and I_{RMS} register values is below a given value. This value can be set with the LTCH configuration bits.

Four different no-load threshold values can be chosen according to the two configuration bits LTCH (see *Table 11*).

Table 11. No load detection thresholds

LTCH	K_{LTCH}
0	800
1	1600
2	3200
3	6400

When a no load condition occurs (BIL=1) the integration of power is suspended and the tamper module is disabled.

In standalone mode, if a no load condition is detected, the BIL signal blocks generation of pulses for stepper and forces SCLNLC pin to be low. If APL = 2 (see *Section 8.14*) the LED pin continues providing the high frequency pulses, while if APL = 3, the pulses are stopped as happens for MOP and MON.

In peripheral mode, the BIL signal can be accessed only through the SPI interface.

8.9 Error detection

In addition to the no load condition and the line frequency band, the integration of power can be suspended also due to detected error on the source signals.

There are two kinds of error detection circuits involved. The first checks all the $\sum \Delta$ signals from the analog part if any is stacked at 1 or 0 within the 1/128 of f_{CLK} period of observation. In case of detected error the corresponding $\sum \Delta$ signal is replaced with an idle $\sum \Delta$ signal, which represents a constant value 0. All error and other resolved flags are treated as bits of a device status and can be read out by means of SPI interface.

Another error condition occurs if the MOP, MON and LED pin outputs signals are different from the internal signals that drive them. This can occur if some of this pin is forced to GND or to some other imposed voltage value. In this case the internal status bit PIN is activated providing the information that some hardware problem has been detected, for example the stepper motor has been mechanically blocked.

8.10 Tamper detection module

The STPM01 is able to measure the current in both live and neutral wire with a time domain multiplexing approach on a unique sigma delta modulator. This mechanism is adopted to implement anti-tamper function. If this function is selected (see *Table 9*), the live and neutral wire currents are monitored; when the difference between the two measurements exceeds a rated threshold the STPM01 enters the "tamper state", while in "normal state" the two measurements are below the threshold.

In particular, both channels are not observed all the time, rather a time multiplex mechanism is used. During the observation time of each channel, its active energy is calculated. A tamper condition occurs when the absolute value of the difference between the two active energy values is greater than a certain percentage of the averaged energy during the activated tamper module (see *Equation 1:*).

This percentage value can be selected between two different values (12.5 % and 6.25 %) according to the value of the configuration bit CRIT.

The tamper condition is detected when the following formula is satisfied:

Equation 1

$$EnergyCH1 - EnergyCH2 > K_{CRIT} (EnergyCH1 + EnergyCH2)/2;$$

where K_{CRIT} can be 12.5 % or 6.25 %.

The detection threshold is much higher than the accuracy difference of the current channels, which should be less than 0.2 %, but, some headroom should be left for possible transition effect, due to accidental synchronism of actual load current change with the rhythm of taking the energy samples.

The tamper circuit works if the energies associated with the two current channels are both positive or negative, if the two energies have different sign, the tamper is on all the time however, the channel with the associated higher power is selected for the final computation of energy.

In single wire mode, the apparent energy rather than the active is used for tamper detection.

When internal signals are not good enough to perform the calculations, i.e. line period is out or range or $\Delta\Sigma$ signals from analog section are stacked at high or low logic level, or no load condition is activated, the tamper module is disabled and its state is preset to normal.

8.10.1 Detailed operational description

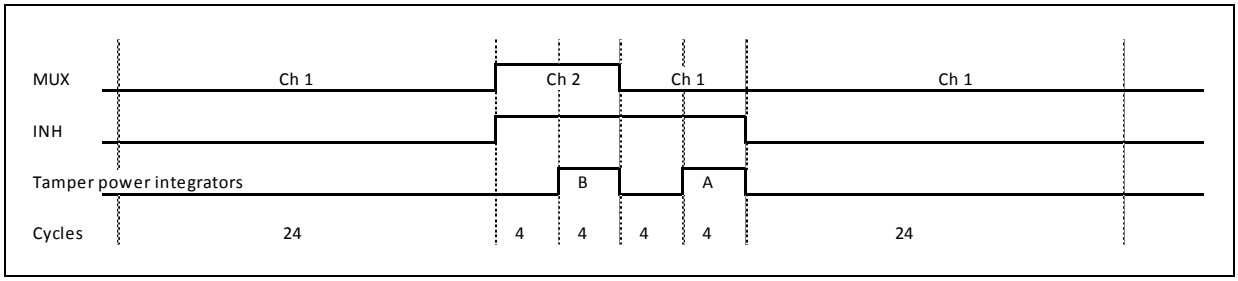
The meter is initially set to normal state, i.e. tamper not detected.In this condition the primary channel is selected for final integration of energy. In such state the values of both load currents should not differ more than the accuracy difference of the channels does. Sixty-four periods of line voltage is used as a tamper checking period.

After 24 periods of line voltage two internal signals MUX and INH are changed in order to enable secondary current channel and to freeze the last power and RMS values of primary current channel. The following 16 periods of line frequency are used for tamper detection integration. During this gap, the final energy calculation does not use the signal from selected channel but the frozen values.

Four line periods after the INH switch, the integration of power from secondary current channel is started and lasts four periods. Additional four line periods later MUX signal is switched back to primary current channel and the integration for tamper detection is started.

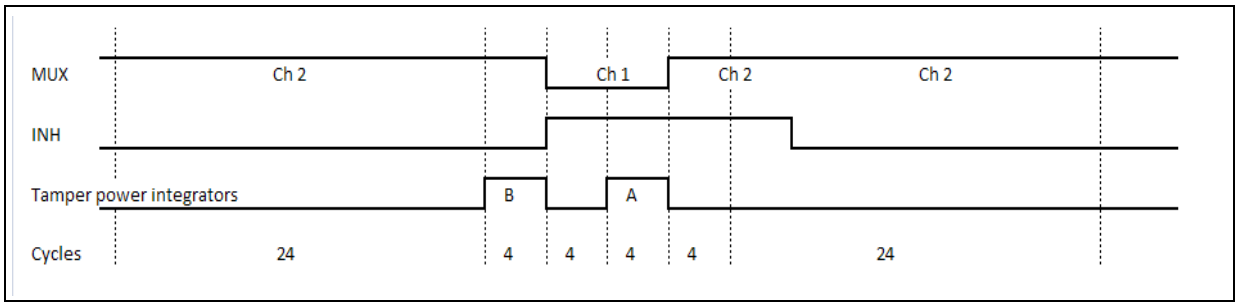
The timings of MUX and INH signals are shown in *Figure 18* below.

Figure 18. Timings of tamper module - Primary channel selected



When the secondary channel is selected to be integrated by the final energy integrator, the MUX and INH signals change according to *Figure 19* below.

Figure 19. Timings of tamper module - Secondary channel selected



This means that energy of four periods from secondary channel followed by energy of four periods from primary channel is sampled within the tamper module. From these two

samples, called B and A respectively, the criteria of tamper is calculated and the channel with higher current is selected, resulting in a new tamper state. If four consecutive new results of criteria happen, i.e. after elapsed 5.12 s at 50 Hz, the meter will enter into tamper state. Thus, the channel with the higher current will be selected for the energy calculation. If samples of power A and B would have different signs, the Tamper would be on all the time but, the channel with bigger power would be still selected for the final integration of energy.

If a tamper status has been detected, the multiplex ratio will be 56:8 if the primary channel energy is greater than the secondary one, otherwise it will be 8:56.

The detected tamper condition is stored in the BIT status bit. If BIT = 0 tamper is not detected, if BIT = 1 a tamper condition has been detected. In standalone mode the BIT flag is also available in the SDATD pin.

8.11 Phase compensation

The STPM01 is does not introduce any phase shift between voltage and current channel.

However, the voltage and current signals come from transducers, which could have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The STPM01 provides a means of digitally calibrating these small phase errors through a introducing delays on the voltage or current signal. The amount of phase compensation can be set using the 4 bits of the phase calibration register (CPH).

The default value of this register is at value of 0 which gives 0° phase compensation. When the 4 bits give a CPH of 15 (1111) the introduced compensation is +0.576°. This compensates the phase shift usually introduced by the current sensor, while the voltage sensor, normally a resistor divider, does not introduce any delay. The resolution step of the phase compensation is 0.038°.

8.12 Clock generator

All the internal timing of the STPM01 is based on the CLKOUT signal. This signal can be generated in three different ways:

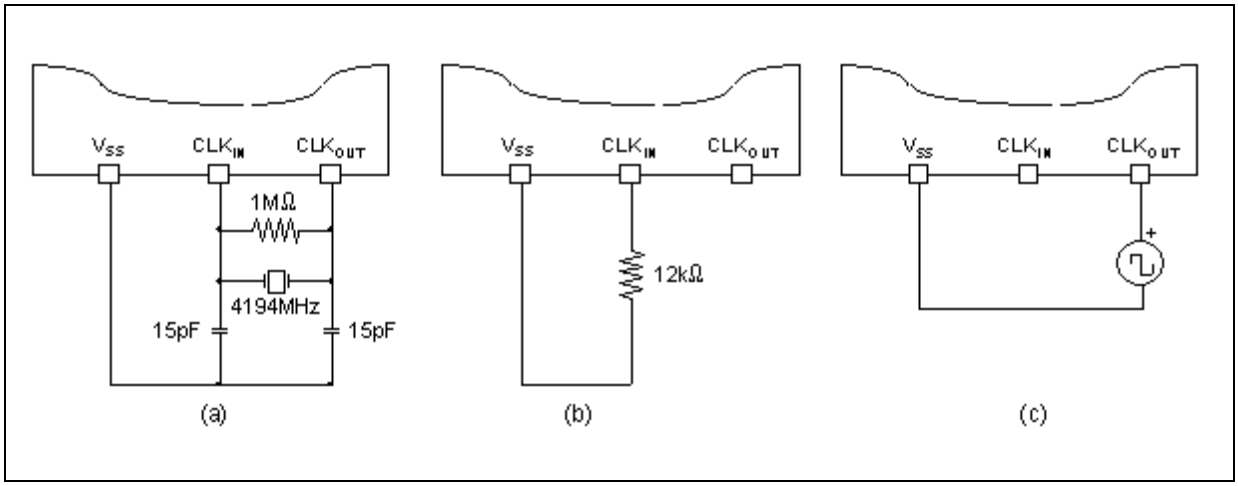
1. RC: this oscillator mode can be selected using the RC configuration bit. If RC = 1 the STPM01 will run using the RC oscillator. A resistor connected between CLKIN and ground will set the RC current. For 4 MHz operation the suggested settling resistor is 12 kΩ; The oscillator frequency can be compensated using the CRC configuration bit (see *Table 16*)
2. Quartz: If RC = 0 the oscillator will work with an external crystal. The suggested circuit is depicted in *Figure 20*;
3. External clock: keeping RC=0, it is also possible to feed the CLKOUT pin with an external oscillator signal

The clock generator is powered from analog supply and is responsible for two tasks. The first one is to retard the turn on of some function blocks after POR in order to help smooth start of external power supply circuitry by keeping off all major loads.

The second task of the clock generator is to provide all necessary clocks for analog and digital parts. Within this task, the MDIV configuration bit is used to inform the device about

the nominal frequency value of CLKOUT. Two nominal frequency ranges are expected, from 4.000 MHz to 4.194 MHz (MDIV = 0) or from 8.000 MHz to 8.192 MHz (MDIV = 1).

Figure 20. Different oscillator circuits (a): with quartz; (b): internal oscillator; (c): with external source



8.12.1 RC Startup procedure

To use the device with RC oscillator the configuration bit RC (see *Table 16*) must be set.

Since the default configuration is for a crystal oscillator, when a RC oscillator is used instead and the device is supplied for the very first time it is not internally clocked and consequently the DSP is inactive. In this condition it is not possible to set RC or any other configuration bit.

The following SPI procedure can be run in order to set the RC bit and provide the clock to the device:

- Set the mode signal BANK;
- Perform a software reset;
- Read the registers: BANK mode signal should be checked and the records should show something (not 000000F0);
- Set the mode signal RD;
- Read the registers through SPI just to check that RD mode signal has been set;
- Clear the mode signal BANK;
- DO NOT perform a reading, and write configuration bit RC;

In this way the RC oscillator is started. If the registers are read again, it can be seen that RD and RC bits are set, and BANK is cleared.

Once the RC startup procedure is complete, the device is clocked and active and it is possible to permanently write the RC bit.

For details on mode signals refer to *Chapter 8.20*, for SPI operations refer to *Chapter 8.21*.

8.13 Resetting the STPM01

The STPM01 has no reset pin. The device is automatically reset by the POR circuit when the V_{CC} crosses the 2.5 V value but it can be reset also through the SPI interface giving a dedicated command (see SPI section for remote reset command details).

In case of reset caused by POR circuit all clocks and both DC buffers in the analog part are kept off for about 30 ms and all blocks of digital part, except for SPI interface, which is hold in a reset state for about 125 ms after a reset condition.

When the reset is performed through SPI no delayed turn on is generated.

Resetting the STPM01 causes all the functional modules of STPM01 to be cleared including the OTP shadow latches (see paragraph 16 for OTP shadow latches description).

The reset through SPI (remote reset request) will normally take place during production testing or in an application of meter with some on-board microprocessor when some malfunction of metering device will be detected.

8.14 Energy to frequency conversion (standalone)

When used in standalone mode the STPM01 provides energy to frequency conversion both for calibration and energy readout purposes. In fact one convenient way to verify the meter calibration is to provide a pulse train signal with 50 % duty cycle whose frequency signal is proportional to the active energy under steady load conditions. In this case the user will choose a certain number of pulses on the LED pin that will corresponds to 1 kWh. We will name this value as P.

The active energy frequency-based signal is available in the LED pin when APL = 2 or APL = 3.

If APL = 2 the LED is driven from internal signal AW (active energy) whose frequency is proportional to the active energy. The signal AW is taken from the 11^{th} bit of the active energy register, consequently a relationship between the LSB value of the active energy register and the number of pulses provided per each kWh (P) can be defined as.

$k_{AW} = 1000/(2^{11} \bullet P)$ [Wh]

If APL = 3 the LED pin provides active energy frequency-based signal dependent on the value of the KMOT configuration bit according to the following table. In this case the pulses will have a fixed width of 31.25 ms.

Table 12. Different settings for LED signal

KMOT (2 Bits)	APL=2	APL=3
	Pulses	Pulses
0	P	P/64
1		P/128
2		P/32
3		P/256

Due to the innovative and proprietary power calculation algorithm the frequency signal is not affected by any ripple at twice the line frequency, this feature strongly reduces the calibration time of the meter.

In a practical example where APL = 2, and the desired P is 64000 pulses/kWh (= 17.7 Hz*kW), we have:

K_{AW} = 7.63*10-6 Wh

This means that the reading of 0x00001 in the active energy register represents 7.63 µWh, while 0xFFFFF represents 8 Wh.

8.15 Driving a stepper motor (standalone)

When used in standalone mode (APL = 2 or APL = 3), the STPM01 is able to directly drive a stepper motor. From signal AW, a stepper driving signals MA and MB are generated by means of internal divider, mono-flop and decoder. The MA and MB signals are brought to the MOP and MON pins that are able to drive the stepper motor. Several kinds of selections are possible for the driving signals according to the configuration bits LVS and KMOT. The numbers of pulses per kWh (PM) in the MOP and MON outputs are linked with the number of pulses of the LED P (see previous paragraph) pin with the following relationship:

Table 13. Configuration of MOP and MON pins

LVS (1 Bit)	KMOT (2 Bits)	Pulses length	PM
0	0	31.25 ms	P/64
0	1	31.25 ms	P/128
0	2	31.25 ms	P/32
0	3	31.25 ms	P/256
1	0	156.25 ms	P/640
1	1	156.25 ms	P/1280
1	2	156.25 ms	P/320
1	3	156.25 ms	P/2560

The mono-flop limits the length of the pulses according to the LVS bit value.

The decoder distributes the pulses to MA and MB alternatively, which means that each of them has only a half of selected frequency.

Negative power is computed with its own sign, and the MOP and MON signals invert their logic state in order to make the backward rotation direction of the motor. See the diagram below.

Figure 21. Positive energy stepper driving signals

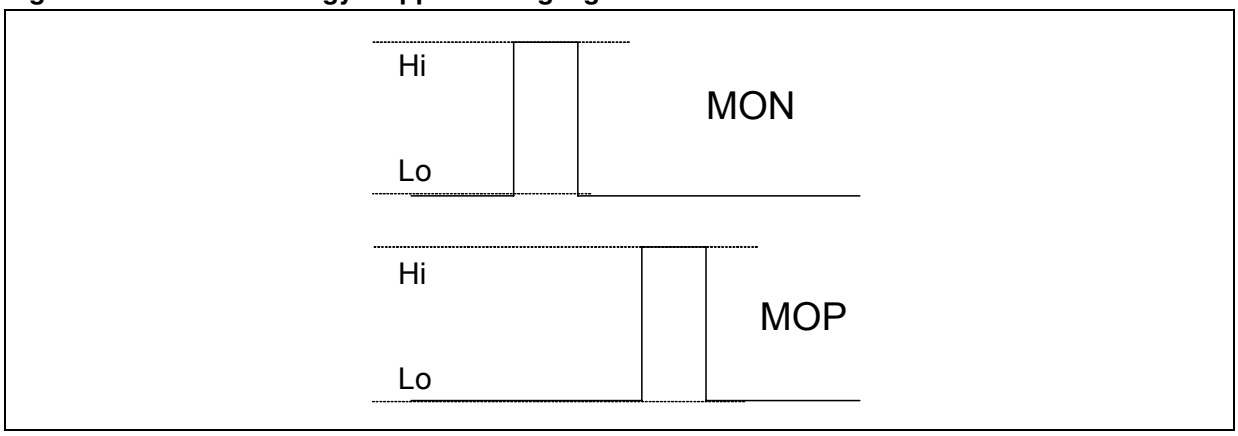
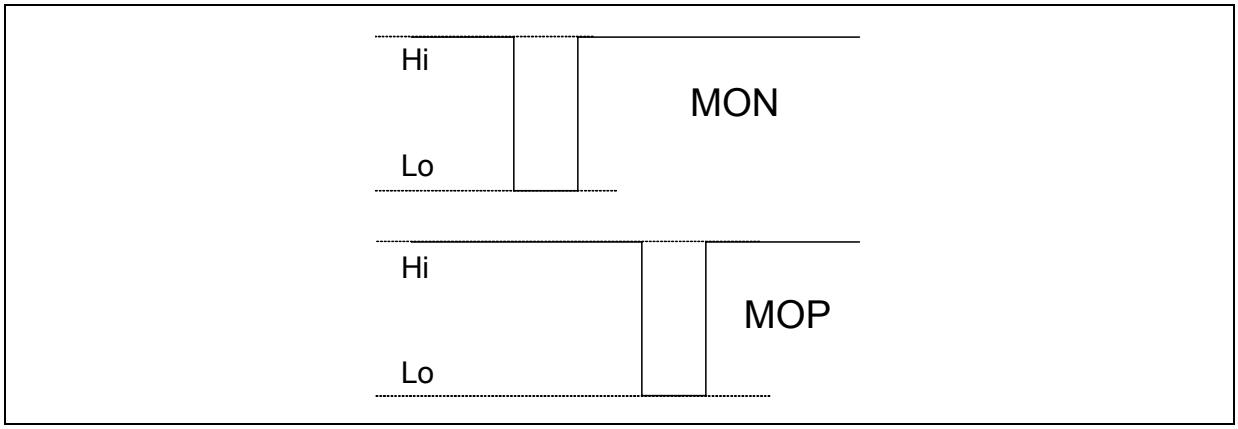


Figure 22. Negative energy stepper driving signals



When a no-load condition is detected MOP and MON are held low.

8.16 Using STPM01 in microcontroller based meter (peripheral)

The higher flexibility of STPM01 allows its use in very high end microcontroller based energy meters. In this case the STPM01 must be programmed to work in peripheral mode, all the SPI pins (SCS, SCLNCL, SDATD, SYN) are used only for communication purposes allowing the microcontroller to write and read the internal STPM01 registers. The peripheral mode has two further different configuration modes according to the status of the APL configuration bit. The APL bit status changes the function of MOP, MON and LED pins according to the description below.

APL = 0:

In the MOP pin, the ZCR signal is available (see paragraph 3 for details about ZCR signal);

The pin MON provides the DOG signal. The DOG signal generates a 16 ms long positive pulse every 1.6 seconds. Generation of these pulses can be suspended if data are read in intervals shorter than 1.6 s. The DOG signal is actually a watchdog reset signal which can be used to control an operation of an on-board microcontroller. It is set to high whenever the V_{DDA} voltage is below 2.5 V, but after V_{DDA} goes above 2.5 V this signal starts to run.

It is expected that an application microcontroller should access the data in the metering device on regular basis at least 1/s (recommended is 32/s). Every latching of results in the metering device requested from the microcontroller also resets the watchdog. If latching requests does not follow each other within 1.6 second, an active high pulse on MON is produced, because device assumes that microcontroller does not operate properly. An application can use this signal either to control the RESET pin of its microcontroller or it can be tied to some interrupt pin. The last possibility is recommended for a battery backup application which can enter some sleep mode due to power down condition and should not be reset by metering device because it would exit from the sleep mode.

The LED pin can be driven from AW wide band (active energy as in standalone mode), AW limited at fundamental, RW (reactive energy) or SW (apparent energy) according to the value of KMOT bit.

Table 14. LED pin configuration in peripheral mode

KMOT (2 Bits)	Signal available in LED pin	# of Pulses
0	AW Type 0 (1)	P [kWh]
1	AW Type 1 (1)	P [kWh]
2	RW	P [kVARh]
3	SW	P [kVAh]

1. * Type0 is the Wide band Active Energy and Type1 is the fundamental Active Energy if FUND=0, if FUND=1 they are swapped.

In this case, since the LED pin is driven by signals different from AW, some other relationship between the LSB of the register and must be defined:

$K_{AWFund} = 4*K_{AW}$ [Wh]

$K_{RW} = 2*K_{AW}$ [VARh]

$K_{SW} = K_{AW}$ [VAh]

APL = 1:

MOP provides the $\sum \Delta$ signal generated from the analog voltage input;

MON provides the $\sum \Delta$ signal generated from the analog current input, according to the selection of the tamper module

LED provides the information about the selection of the current channel made by the tamper module. If LED is low it means the primary channel is selected, if LED is high the secondary channel is actually selected.

8.17 Status bits

The STPM01 includes 8 status bits that provide several information on the current meter status. The status bits are the following:

Table 15. Status bit description

Bit #	Name	Description	Condition
0	BIL	No load condition	BIL=0: No load condition not detected
			BIL=1: No load detected
1	BCF	$\sum \Delta$ signals status	BCF=0: $\sum \Delta$ signals alive
			BCF=1: one or both $\sum \Delta$ signals are stacked
2	BFR	Line frequency range	BFR=0: Line frequency inside the 45Hz-65Hz range
			BFR=1: Line frequency out of range
3	BIT	Tamper condition	BIT=0: Tamper not detected;
			BIT=1: Tamper detected;
4	MUX	Current channel selection	MUX=0: Primary current channels selected by the tamper module;
			MUX=1: Secondary current channels selected by the tamper module;
5	LIN	Trend of the line voltage	LIN=0: line voltage is going from the minimum to the maximum value. ($\Delta v/\Delta t > 0$);
			LIN=1: line voltage is going from the maximum to the minimum value. ($\Delta v/\Delta t < 0$);
6	PIN	Output pins check	PIN=0: the output pins are consistent with the data
			PIN=1: the output pins are different with the data, this means some output pin is forced to 1 or 0.
7	HLT	Data Validity	HLT=0: the data records reading are valid.
			HLT=1: the data records are not valid. A reset occurred and a restart is in progress.

When STPM01 is used in peripheral mode all these signal can be read through the SPI interface. See paragraph 16 for details on the Status bit location in the STPM01 data records.

In standalone mode the BIL signal is available in SCLNLC pin and the BIT signal in the SDATD pin. All the other signals can be read only through SPI interface.

8.18 Programming the STPM01

Data records

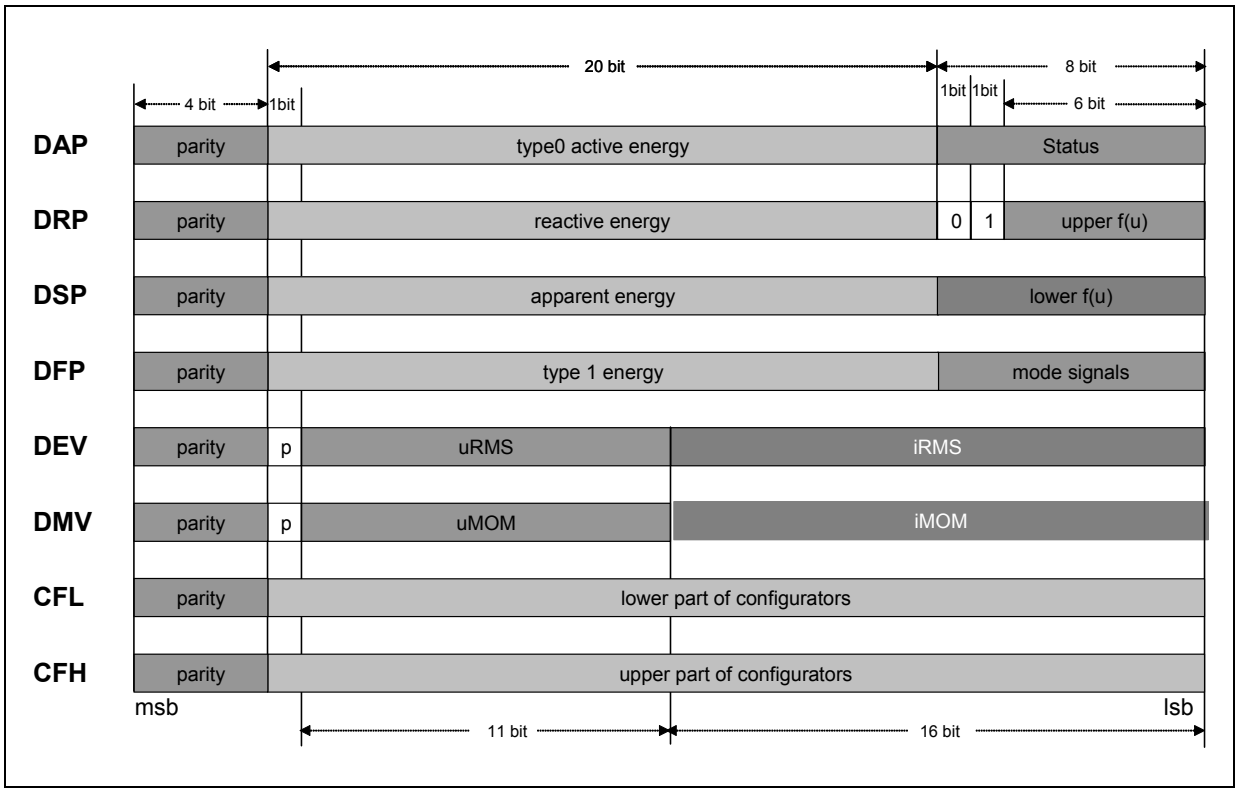
The STPM01 has 8 internal data records registers. Every data record consists of 4-bit parity code and 28-bit data value where the parity code is computed from the data value, which makes total of 32 bits or 4 bytes.

The figure below shows the data records structure with the name of the contained information.

Each bit of parity nibble is defined as odd parity of all seven corresponding bits of data nibbles.

The first 6 registers are read-only except for the 8 bit mode signals in the DFP register (the mode signals will be described later in this paragraph). The last two registers CFL and CFH can be also written because they contain the configuration bits. Among these last 64 bits (32 of CFL and 32 of CFH), 8 bits are used for parity nibbles, then only 56 bits are used for configuring and programming the STPM01.

Figure 23. STPM01 data records map



8.19 Configuration bits

All the configuration bits that control the operation of the device (CFL and CFH data records) can be written in a temporary or permanent way. In case of temporary writing the configuration bits value are written in the so called shadow registers which are simple latches that hold the configuration data. In case of permanent writing the configuration bits are stored in the OTP (one time programmable) cells that keep the information for an undefined period of time even if the STPM01 is without supply, but, once written, they cannot be changed anymore.

The shadow registers are cleared whenever a reset condition occurs (both POR and remote reset).

As indicated in the data records table, the configuration bits are 56. Each of them consists of paired elements, one is latch, the OTP shadow, and another is the OTP antifuse element. When the STPM01 is released in the market, all antifuses represents logic low state but they can be written by the user in order to configure the STPM01.This means that STPM01 can retain 56 bits of information even if it has been unsupplied for an undefined time. That's why the CFG signals are used to keep certain configuration and calibration values of device.

The very first CFG bit, called TSTD, is used to disable any change of system signals after it was permanently set. During the configuration phase, each bit set to logic level 1 will increase the supply current of STPM01 of about 120 µA, until the TSTD bit is set to 1. The residual increase of supply current is 2 µA per each bit set to 1. It is then recommended to set the TSTD bit to 1 after the configuration procedure in order to keep the supply current as low as possible.

The STPM01 can work either using the data stored in the OTP cells either the data available in the shadow latches. This can be chosen according to the value RD Mode signal (see mode signal paragraph for description). If the RD is set, the CFG bits originates from corresponding OTP shadow latches otherwise, if the RD is cleared, the CFG bits originates from corresponding OTP antifuses. This way one can temporary sets up certain configuration or calibration of device then verify it and then change it, if it is necessary. For example, this is extensively exercised during production tests.

Each configuration bit can be written sending a byte command to STPM01 through its SPI interface. The procedure to write the configuration bits is described in the SPI section.

After the TSTD bit has been set, the only write commands accepted will be the precharge and the remote reset, this implies that the shadow latches cannot be used as source of configuration data anymore.

Table 16. Configuration bits map

Address		Name	n. of bits	Description (1)
6-bit binary	DEC			
000000	0	TSTD	1	Test mode and OTP write disable: - TSTD=0: testing and continuous pre-charge of OTP when in read mode, - TSTD=1:normal operation and no more writes to OTP
000001	1	MDIV	1	Measurement frequency range selection: - MDIV=0: 4.000MHz to 4.194MHz, - MDIV=1: 8.000MHz to 8.192MHz
000010	2	RC	1	Type of internal oscillator selection: - RC=0:crystal oscillator, - RC=1:RC oscillator
000011	3	APL	2	Peripheral or Standalone mode: - APL=0: peripheral, MON=WatchDOG; MOP=ZCR, LED=pulses, - APL=1: peripheral, MOP=ΔΣ Voltage; MON=ΔΣ current; LED=Mux (current) - APL=2: standalone, MOP,MON=stepper, LED=pulses, SCLNLC=no load condition, SDATD=tamper detected, SYN=negative active power direction - APL=3: standalone, MOP:MON=stepper, LED=pulses according to KMOT, SCLNLC=no load condition, SDATD=tamper detected, SYN=negative active power direction
000100	4 (1)			

Table 16. Configuration bits map (continued)

Address		Name	n. of bits	Description (1)
6-bit binary	DEC			
000101	5	PST	3	Current channel sensor type, gain and tamper selection: - PST=0: primary is coil x8 (x16 if ADDG=1), secondary is not used, no tamper - PST=1: primary is coil x24 (x32 if ADDG=1), secondary is not used, no tamper - PST=2: primary is CT x8, secondary is not used, no tamper - PST=3: primary is shunt x32, secondary is not used, no tamper - PST=4: primary is coil x8 (x16 if ADDG=1), secondary is coil x8 (x16 if ADDG=1), tamper - PST=5: primary is coil x24 (x32 if ADDG=1), secondary is coil x24 (x32 if ADDG=1), tamper - PST=6: primary is CT x8, secondary is CT x8, tamper - PST=7: primary is CT x8, secondary is shunt x32, tamper
000110	6			
000111	7 (1)			
001000	8	FRS	1	Power calculation when BFR=1 and PST≠4,5 (no single wire mode) - FRS=0: energy accumulation is frozen, power is set to zero; - FRS=1: normal energy accumulation and power computation (p=u*i);
001001	9	MSBF	1	Bit sequence output during record data reading selection: - MSBF=0: msb first - MSBF=1: lsb first
001010	10	FUND	1	This bit swap the information stored in the type0 (first 20 bits of DAP register) and type1 (first 20 bits of DFP register) active energy. - FUND = 0: type 0 contains wide band active energy, type1 contains fundamental active energy - FUND = 1: type 0 contains fundamental active energy, type1 contains wide band active energy
001011	11		1	RESERVED
001100	12	LTCH	2	No load condition threshold as product between V_{RMS} and I_{RMS}: LTCH=0 800 LTCH=1 1600 LTCH=2 3200 LTCH=3 6400
001101	13 (1)			
001110	14	KMOT	2	Constant of stepper pulses/kWh (see par. 16) selection when APL=2 or 3: If LVS=0, KMOT=0 P/64 KMOT=1 P/128 KMOT=2 P/32 KMOT=3 P/256
				If LVS=1, KMOT=0 P/640 KMOT=1 P/1280 KMOT=2 P/320 KMOT=3 P/2560
001111	15 (1)			Selection of pulses for LED when APL=0: KMOT=0 Type0 Active Energy KMOT=1 Type1 Active Energy KMOT=2 Reactive Energy KMOT=3 Apparent Energy

Table 16. Configuration bits map (continued)

Address		Name	n. of bits	Description (1)
6-bit binary	DEC			
010000	16		2	RESERVED
010001	17 (1)			
010010	18	BGTC	2	Bandgap Temperature compensation bits. See *Figure 17* for details.
010011	19 (1)			
010100	20	CPH	4	4-bit unsigned data for compensation of phase error, 0°+0.576°. 16 values are possible with a compensation step of 0.0384°. When CPH=0 the compensation is 0°, when CPH=15 the compensation is 0.576°.
010101	21			
010110	22			
010111	23 (1)			
011000	24	CHV	8	8-bit unsigned data for voltage channel calibration. 256 values are possible. When CHV is 0 the calibrator is at -12.5 % of the nominal value. When CHV is 255 the calibrator is at +12.5 %. The calibration step is then 0.098%.
011001	25			
011010	26			
011011	27			
011100	28			
011101	29			
011110	30			
011111	31 (1)			
100000	32	CHP	8	8-bit unsigned data for primary current channel calibration. 256 values are possible. When CHP is 0 the calibrator is at -12.5 % of the nominal value. When CHP is 255 the calibrator is at +12.5 %. The calibration step is then 0.098%.
100001	33			
100010	34			
100011	35			
100100	36			
100101	37			
100110	38			
100111	39 (1)			
101000	40	CHS	8	8-bit unsigned data for secondary current channel calibration. 256 values are possible. When CHS is 0 the calibrator is at -12.5 % of the nominal value. When CHS is 255 the calibrator is at +12.5 %. The calibration step is then 0.098 %.
101001	41			
101010	42			
101011	43			
101100	44			
101101	45			
101110	46			
101111	47 (1)			

Table 16. Configuration bits map (continued)

Address		Name	n. of bits	Description (1)
6-bit binary	DEC			
110000	48	CRC	2	2-bit unsigned data for calibration of RC oscillator. CRC=0, or CRC=3 cal=0% CRC=1, cal=+10%; CRC=2, cal=-10%.
110001	49 (1)			
110010	50	NOM	2	2-bit modifier of nominal voltage for Single Wire Meter. NOM=0: K_{NOM}=0.3594 / NOM=1: K_{NOM}=0.3906 / NOM=2: K_{NOM}=0.4219 / NOM=3: K_{NOM}=0.4531;
110011	51 (1)			
110100	52	ADDG	1	Selection of additional gain on current channels: ADDG=0: Gain+=0 / ADDG=1: Gain+=8
110101	53	CRIT	1	Selection of tamper threshold: CRIT =0: 12,5% / CRIT =1: 6,25%
110110	54	LVS	1	Type of stepper selection: LVS=0: pulse width 31.25 ms, 5V, / LVS=1: pulse width, 156.25 ms, 3V
110111	55		1	Reserved

1. IMPORTANT: This bit represents the MSB of the decimal value indicated in the description column.

As it is indicated above, the STPM01 includes 56 CFG bits. Normally, some of these bits should be permanently set during production of application of STPM01 in order to protect the application from power fails. Of course, if an application would include an on-board microcontroller, it could reload the configuration and calibration values after power on restart and so, the permanent set of STPM01 would not be necessary. But this is not very safe way to do it, because due to some EMI even imposed to tamper the meter, the microcontroller may become lost and during such state, it can change some system signals in the STPM01 or somebody can change the calibration and configuration by changing the software of on-board microcontroller.

8.20 Mode signals

The STPM01 includes 8 mode signals located in the DFP data record, 3 of these are used only for internal testing purposes while 5 are useful to change some of the operation of the STPM01. The mode signals are not retained when the STPM01 supply is not available and then they are cleared when a POR occurs but they are not cleared when a remote reset command (RRR) is sent through SPI.

The mode signals bit can be written using the normal writing procedure of the SPI interface (see SPI section).

Of course, we can clear the RD by clearing all system signals. The first way is to generate POR signal but this way we clear and reset the whole device. An alternative way is to set the TSTD bit in the shadow latches. This setting becomes effective after SCS goes to idle state when the TSTD clears all system signals including itself but, it does not reset the whole device.

Table 17. Mode signals description

Bit #	Signal name	Bit value	Status	Binary command	Hex command
0	BANK	0	Used for RC startup procedure	0111000x	70 or 71
		1		1111000x	F0 or F1
1	PUMP	0	MOP and MON operates normally	0111001x	72 or 73
		1	MOP and MON provides the driving signals to implement a charge-pump DC-DC converter	1111001x	F2 or F3
2	Reserved				
3	Reserved				
4	CSEL	0	Current Channel 1 selected when tamper is disabled	0111100x	78 or 79
		1	Channel 2 selected when tamper is disabled	1111100x	F8 or F9
5	RD	0	The 56 Configuration bits originated by OTP antifuses	0111101x	7A or 7B
		1	The 56 Configuration bits originated by shadow latches	1111101x	FA or FB
6	WE	0	Any writing in the configuration bits is recorded in the shadow latches	0111110x	7C or 7D
		1	Any writing in the configuration bits is recorded both in the shadow latches and in the OTP antifuse elements	1111110x	FC or FD
7	Precharge	1	Swap the 32 bits data records reading. From 1,2,3,4,5,6,7,8, to 5,6,7,8,1,2,3,4 and viceversa	1111111x	FF

– **RD** mode signal has been already described in the SPI section but there is another implied function of the signal RD. When it is set, each sense amplifier is disconnected from corresponding antifuse element and this way, its 3 V NMOS gate is protected from the high voltage of VOTP during permanent write operation. This means that as long as the VOTP voltage reads more than 3 V, the signal RD should be set.
– **PUMP**: when set, the PUMP mode signal transform the MOP and MON pins to act as driving signals to implement a charge-pump DC-DC converter (see schematic page 36). This feature is useful in order to boost the V_{CC} supply voltage of the STPM01 to generate the VOTP voltage (14 V to 20 V) needed to program the OTP antifuse elements.
– **CSEL** In normal operation, if the anti-tamper module is not activated (see PST configuration bits) the STPM01 will select the channel 1 as source of current information. For debug or calibration purposes it is possible to select channel 2 as source of current channel signal when the tamper module is disabled. This is done setting CSEL mode bit.
– **WE** (write enable): This mode signal is used to permanently write to the OTP antifuse element. When this bit is not set, any write to the configuration bit is recorded in the shadow latches. When this bit is set the writing is recorded both in the shadow latch and in the OTP antifuse element.
– **Precharge**: this command swaps the sequence of data record read, allowing the reading of the last four data records as first and the first four as second. The reading sequence will be 5, 6, 7, 8, 1, 2, 3, 4. Differently from the other mode signals, the precharge command is not retained inside the STPM01, in fact it should be sent each time before the reading of the data records. This is the only command that can be sent to STPM01 when the TSTD bit has been set.

– **BANK**: it is used to activate RC oscillator (see *Chapter 8.12.1*).

8.21 SPI interface

The SPI interface supports a simple serial protocol, which is implemented in order to enable a communication between some master system (microcontroller or PC) and the device. Three tasks can be performed with this interface:

- remote resetting the device,

- reading data records,

- writing the Mode bits and the configuration bits (temporarily or permanently);

Four pins of the device are dedicated to this purpose: SCS, SYN, SCLNCN, SDATD. SCS, SYN and SCLNLC are all input pins while SDATD can be input or output according if the SPI is in write or read mode. A high level signal for these pins means a voltage level higher than 0.75 x V_{CC}, while a low level signal means a voltage value lower than 0.25 x V_{CC}.

The internal register are not directly accessible, rather a 32 bit of transmission latches are used to pre-load the data before being read or written to the internal registers.

The condition in which SCS, SYN and SCLNLC inputs are set to high level determines the idle state of the SPI interface and no data transfer occurs.

– **SCS:** as already described in the document, when STPM01 is in standalone mode, the SYN, SCLNLC and SDATD are used also for providing information on the meter status (see *Table 5*) and are not used for SPI communication. The SCS pin allows using the above pins for SPI communication even when the STPM01 is working in standalone mode, in fact SCS pin enables SPI operation when low. In this section, the SYN, SCLNLC and SDATD operation as part of the SPI interface is described.
– **SYN**: this pin operates different functions according to the status of SCS pin. When SCS is low the SYN pin status select if the SPI is in read (SYN=1) or write mode (SYN=0). When SCS is high and SYN is also high the results of the input or output data are transferred to the transmission latches.
– **SCLNLC**: it is basically the clock pin of the SPI interface. This pin function is also controlled by the SCS status. If SCS is low, SCLNCL is the input of serial bit synchronization clock signal. When SCS is high, SCLNLC is also high determining the idle state of the SPI.
– **SDATD** is the Data pin. If SCS is low, the operation of SDATD is dependent on the status of SYN pin. if SYN is high SDATD is the output of serial bit data (read mode) if SYN is low SDATD is the input of serial bit data signal (write mode). If SCS is high SDATD is input of idle signal.

Any pin above has internal weak pull up device of nominal 15 µA. This means that when some pin is not forced by external signals, the state of pin is logic high. A high state of any input pin above is considered as an idle (not active) state. For the SPI to operate correctly the STPM01 must be correctly supplied as described in the power supply section. Idle state of SPI module is recognized when the signals of pins SYN, SCS, SCLNLC and SDATD are in a logic high state. Any SPI operations should start from such idle state. The exception to this rule is when STPM01 has been put into mode of standalone application. In such mode it can happen that states of pins SCLNLC, SDATD and SYN are not high due to states of corresponding internal status bits.

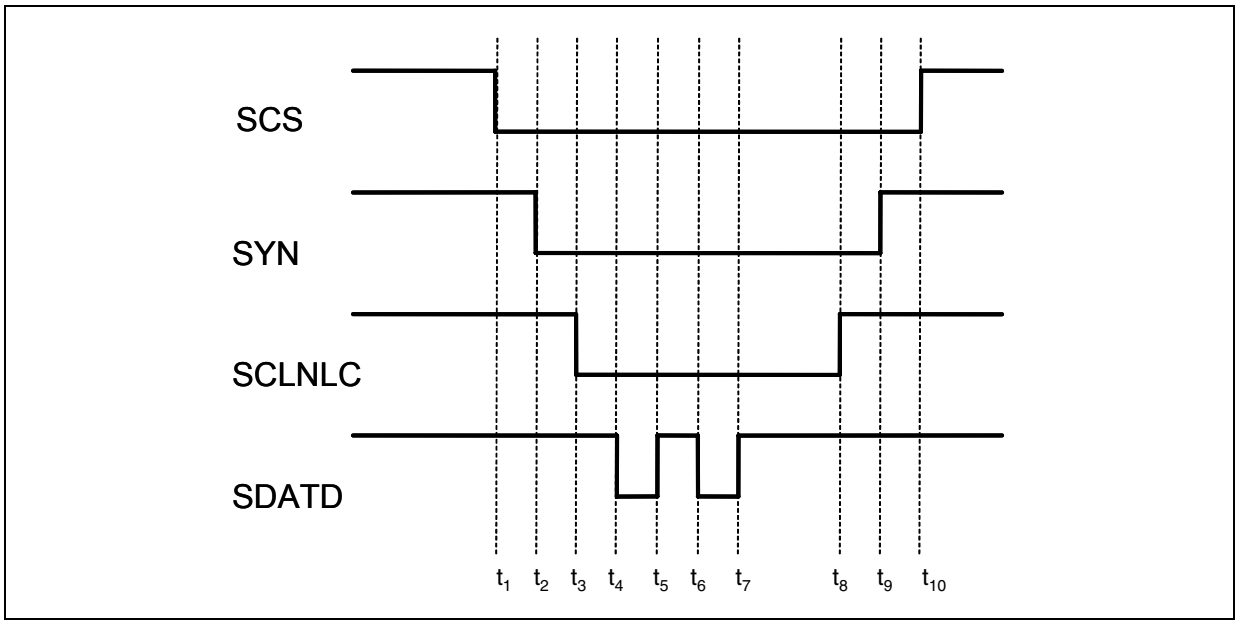
When SCS is active (low), signal SDATD should change its state at trailing edge of signal SCLNLC and the signal SDATD should be stable at next leading edge of signal SCLNLC. The first valid bit of SDATD is always started with activation of signal SCLNLC.

8.21.1 Remote reset

The timing diagram of the operation is shown on the *Figure 24*. The time step can be as short as 30 ns.

The internal reset signal is named RRR. Unlike the POR, the RRR signal does not cause the 30 ms retard restart of analog module and the 120 ms retard restart of digital module. This signal doesn't clear the mode signals.

Figure 24. Timing for providing remote reset request (1)



1. All the time intervals must be longer than 30 ns. $t_7 \rightarrow t_8$ is the reset time, this interval must be longer than 30 ns as well.

8.22 Reading data records

Data records reading will take place most often when there will be an on-board microcontroller in an application. Such microcontroller will be able to read all measurement results and all system signals (configuration, calibration, status, mode). Again, the time step can be as short as 30 ns. There are two phases of reading, called latching and shifting.

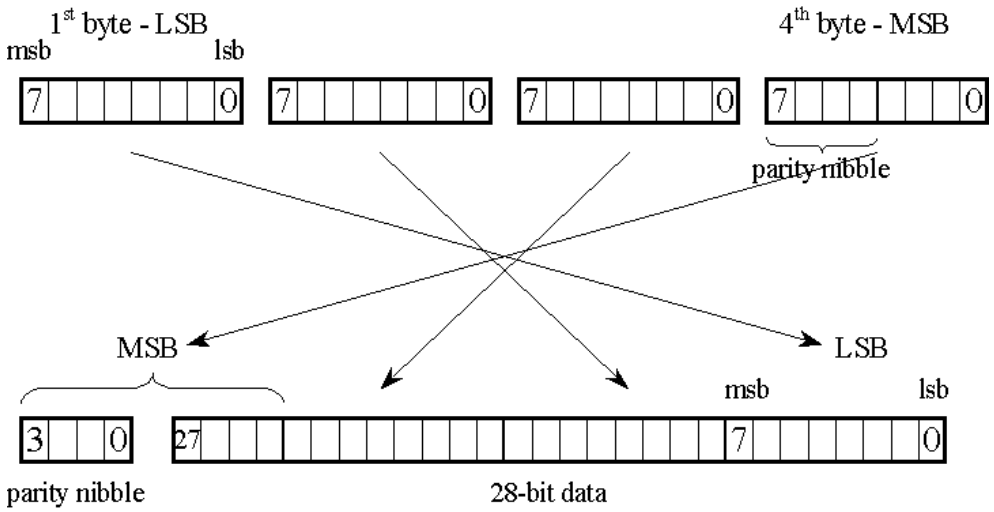
Latching is used to sample results into transmission latches. The transmission latches are the flip-flops that hold the data in the SPI interface. This is done with the active pulse on SYN when SCS is idle. The length of pulse on SYN must be longer than 2 periods of measurement clock, i.e. more than 500 ns at 4 MHz.

The shifting starts when SCS become active. In the beginning of this phase another, but much shorter pulse (30 ns) on SYN should be applied in order to ensure that an internal transmission serial clock counter is reset to zero. An alternative way is to extend the pulse on SYN into the second phase of reading. After that reset is done, a 32 serial clocks per data record should be applied. Up to 8 data records can be read this way. This procedure can be aborted at any time by deactivation of SCS (see *Figure 24*).

The first read out byte of data record is least significant byte (LSB) of data value and of course, the fourth byte is most significant byte (MSB) of data value. Each byte can be further divided into a pair of 4-bit nibbles, most and least significant nibble (MSN, LSN). This

division makes sense with the MSB of data value because the MSN of it holds the parity code rather than useful data.

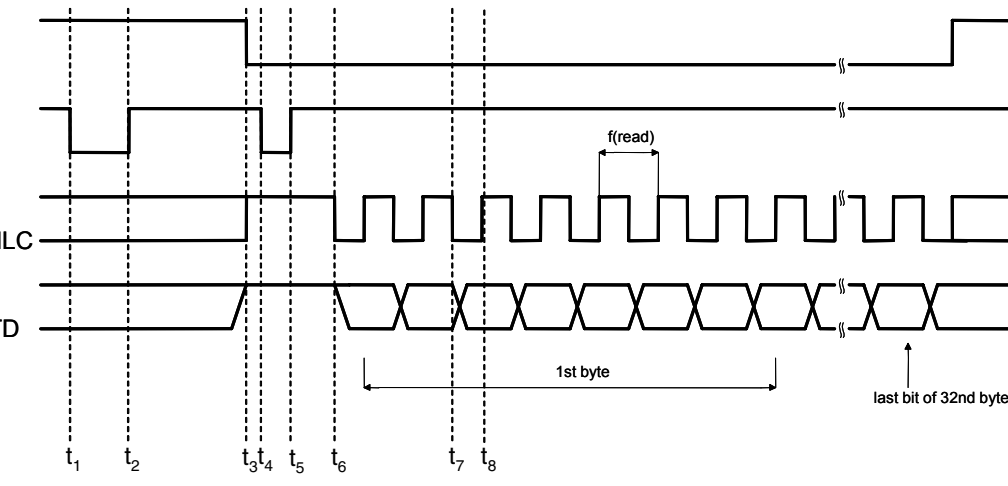
Figure 25. Data records reconstruction



The sequence of data record during the reading operation is fixed. Normally, an application will read 1st,.., 6th data record, the 7th and 8th data record would read only when it need to fetch the configuration data. However, an application may apply a precharge command (see *Table 17*) prior reading phase. This command forces the device to respond with the sequence 5th,.., 8th, 1st,.., 4th. Such change of sequence can be used to skip the first four data records.

The timing diagram of the reading operation is shown on the *Figure 26*. One can see the latching and beginning of shifting phase of the first byte (0x5F) of the first data record and end of reading. Also, both alternatives to reset the internal transmission serial clock counter is shown in signal SYN.

Figure 26. Timing for data records reading



$t_1 \rightarrow t_2$: Latching phase. Interval value > $2/f_{CLK}$

$t_2 \rightarrow t_3$: Data latched, SPI idle. Interval value > 30 ns

$t_3 \rightarrow t_4$: Enable SPI for read operation. Interval value > 30 ns

$t_4 \rightarrow t_5$: Serial clock counter is reset. Interval value > 30 ns

$t_5 \rightarrow t_6$: SPI reset and enabled for read operation. Interval value > 30 ns

t_7: Internal data transferred to SDATD

t_8: SDATD data is stable and can be read

The system that reads the data record from the STPM01 should check the integrity of each data record. If the check fails, the reading should be repeated, but this time only the shifting should be applied otherwise a new data would be latched into transmission latches and incorrectly read one would be lost.

Normally, each byte is read out as most significant bit (MSB) first. But this can be changed by setting the MSBF configuration bit in the STPM01 CFL data record. If this is done, each byte is read out as least significant bit (LSB) first.

8.23 Writing procedure

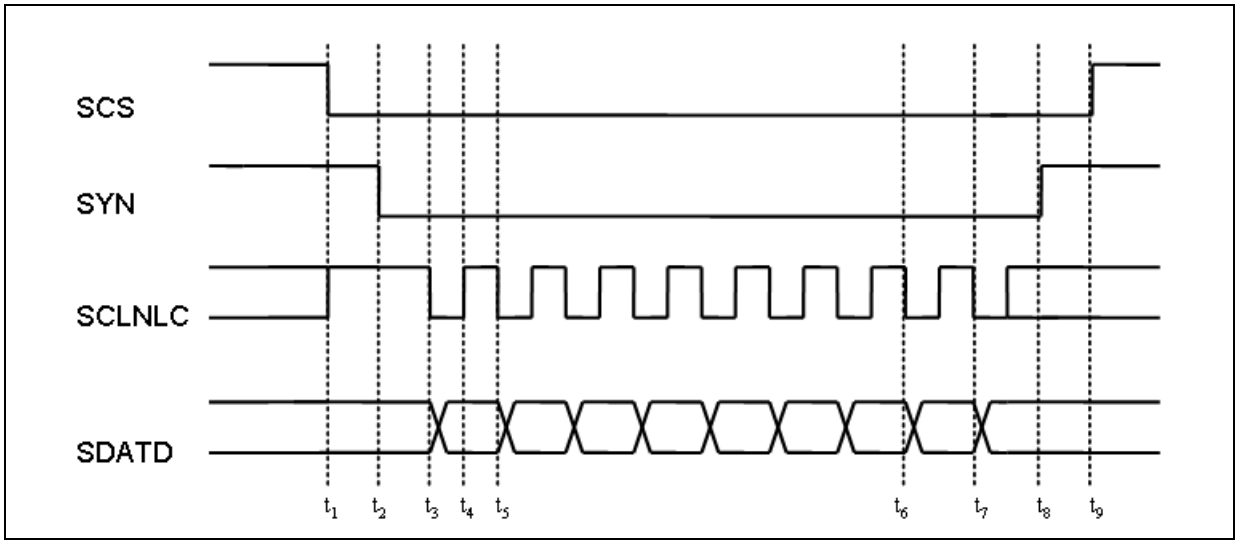
Each writable bit (configuration and mode bits) has its own 6-bit absolute address. For the configuration bits, the 6-bit address value corresponds to its decimal value, while for the mode bits the addresses are the ones indicated in the Mode Signal paragraph.

In order to change the state of some latch one must send to STPM01 a byte of data which is normal way to send data via SPI. This byte consists of 1-bit data to be latched (MSB), followed by 6-bit address of destination latch, followed by 1-bit don't care data (LSB) which makes total 8 bits of command byte.

For example, if we would like to set the configuration bit 47 (part of the secondary current channel calibrator) to 0, we must convert the decimal 47 to its 6-bit binary value: 101111. The byte command will be then composed like this:

1 bit DATA value+6-bits address+1 bit (0 or 1) as depicted in *Figure 27*. In this case the binary command will be 01011111 (0x5F) which is the one depicted in the figure or 01011110 (0x5E).

Figure 27. Timing for writing configuration and mode bits



$t_1 \rightarrow t_2$ (> 30 ns): SPI out of idle state
$t_2 \rightarrow t_3$ (> 30 ns): SPI enabled for write operation
t_3: data value is placed in SDA
t_4: SDA value is stable and shifted into the device
$t_3 \rightarrow t_5$ (> 10 µs): writing clock period
$t_3 \rightarrow t_5$: 1 bit data value
$t_5 \rightarrow t_6$: 6 bits address of the destination latch
$t_6 \rightarrow t_7$: 1 bit EXE command
t_8: end of SPI writing
t_9: SPI enters idle state

The same procedure should be applied for the mode signals, but in this case the 6-bits address must be taken from the *Table 17*.
The LSB of command is also called EXE bit because instead of data bit value, the corresponding serial clock pulse is used to generate the necessary latching signal. This way the writing mechanism does not need the measurement clock in order to operate, which makes the operation of SPI module of STPM01 completely independent from the rest of device logic except from the signal POR.
Commands for changing system signals should be sent during active signals SCS and SYN as it is shown in the *Figure 27*. The SYN must be put low in order to disable SDATD output driver of STPM01 and make the SDATD as an input pin. A string of commands can be send within one period of active signals SCS and SYN or command can be followed by reading the data record but, in this case, the SYN should be deactivated in order to enable SDATD output driver and a SYN pulse should be applied before activation of SCS in order to latch the data.
Interfacing the standard 3-wire SPI with STPM01 SPI.
Due to the fact a 2-wire SPI is implemented in STPM01 it is clear that sending any command from a standard 3-wire SPI would require 3-wire to 2-wire interface, which should produce a proper signal on SDATD from host signals SDI, SDO and SYN. A single gate 3-state buffer could be omitted by an emulation of SPI just to send some command. On a microcontroller this would be done by the following steps:

1. disable the SPI module;
2. set SDI pin which is connected to SDATD to be output;
3. activate SYN first and then SCS;
4. apply new bit value to SDI and activate SCL;
5. deactivate SCL;
6. repeat the last two steps seven times to complete one byte transfer;
7. repeat the last three steps for any remaining byte transfer;
8. set SDI pin to be input;
9. deactivate SCS and the SYN;
10. enable the SPI module;

In case of precharge command (0xFF), emulation above is not necessary. Due to the pull up device on the SDATD pin of the STPM01 the processor needs to perform the following steps:

1. activate SYN first in order to latch the results;
2. after at least 1µs activate SCS;
3. write one byte to the transmitter of SPI (this will produce 8 pulses on SCL with SDI=1);
4. deactivate SYN;
5. optionally read the data records (the sequence of reading will be altered;
6. deactivate SCS;

Permanent writing of the CFG bits
In order to make a permanent set of some CFG bits, the following procedure should be conducted:

1. collect all addresses of CFG bits to be permanently set into some list;
2. clear all OTP shadow latches;
3. set the system signal RD;
4. connect a current source of at least +14 V, 1 mA to 3 mA to VOTP;
5. wait for VOTP voltage is stable;
6. set one OTP shadow latch from the list;
7. set the system signal WE;
8. wait for 300 µs;
9. clear the system signal WE;
10. clear the OTP shadow latch which was set in step 6;
11. until all wanted CFG bits are permanently set, repeat steps 5 to 11;
12. disconnect the current source;
13. wait for VOTP voltage is less than 3 V;
14. clear the system signal RD;
15. read all data records, in the last two of them there is read back of CFG bits;
16. if verification of CFG bits fails and there is still chance to pass, repeat steps 1 to 16.

For steps of set or clear apply the timing shown in *Figure 27* with proper signal on the SDATD. For step 15 apply the timing shown in *Figure 26*.
For permanent set of the TSTD bit, which will cause no more writing to the Configuration bits, the procedure above must be conducted in such way that steps 6 to 13 are performed in series during single period of active SCS because the idle state of SCS would make the signal TSTD immediately effective which in turn, would abort the procedure and possibly destroy the device due to clearing of system signal RD and so, connecting all gates of 3V NMOS sense amplifiers of already permanently set CFG bits to the V_{OTP} source.

8.24 Energy calculation algorithm

Inside the STPM01 the computing section of the measured active power uses a completely new signal patented process approach. This approach allows the device to reach high performances in terms of accuracy.

The signals, coming from the sensors, for the instantaneous voltage:

Equation 2

$v(t) = V \bullet \sin \omega t$; where V is the peak voltage and ω is related to the line frequency

and the instantaneous current:

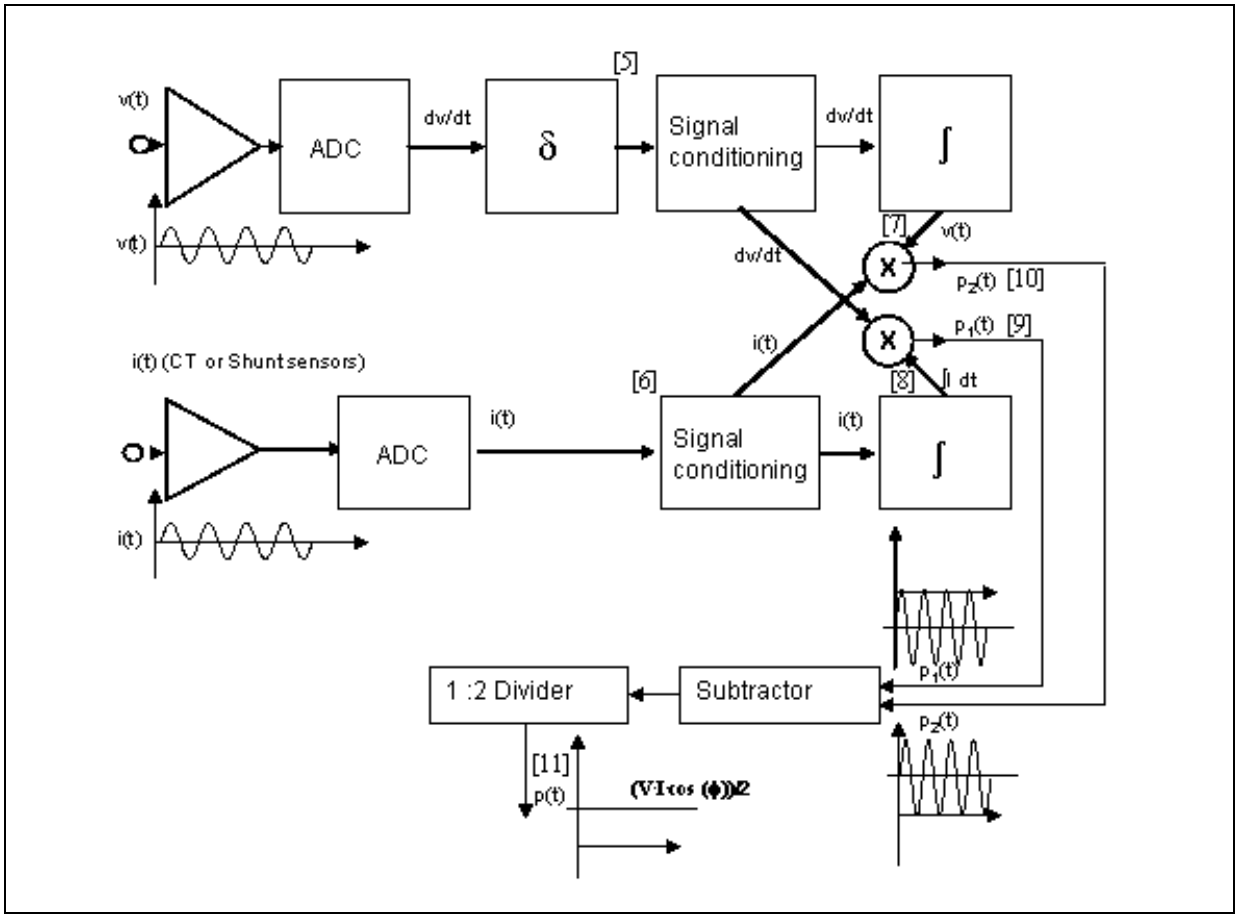
Equation 3

$i(t) = I \bullet \sin(\omega t + \varphi)$;

where I is the peak current, ω is related to the line frequency and φ is the phase difference between voltage and current.

8.24.1 Active power

Figure 28. Active energy computation diagram



In the STPM01, after the pre-conditioning and the A/D conversion, the digital voltage signal (which is dynamically more stable with respect to the current signal) is processed by a differentiated stage which transforms:

Equation 4

$v(t) \rightarrow v'(t) = dv/dt = V \cdot \omega \cdot \cos \omega t$ – [see *Figure 28* - 5]

The resulted signal, together with the pre-processed and digitalized current signal:

Equation 5

$i(t) = I \cdot \sin(\omega t + \varphi)$; [see *Figure 28* - 6]

are then available for the calculation process. These digital signals are also provided into two additional stages which perform the integration of themselves, obtaining:

Equation 6

dv/dt → v(t) = V ·sin ωt; [see *Figure 28* - 7]

i(t) →

$$I(t) = \int i(t) \cdot dt = -\frac{I}{\omega} \cdot \cos(\omega t + \varphi)$$

[see *Figure 28* - 8]

Now four signals are available. Combining (pairing) them by means of two multiplying stages two results are obtained:

Equation 7

$$p_1(t) = \frac{dv}{dt} \cdot \int i(t) \cdot dt = -\frac{V \cdot I \cdot \cos\varphi}{2} - \frac{V \cdot I \cdot \cos(2\omega t + \varphi)}{2}$$

[see *Figure 28* - 9]

Equation 8

$$p_2(t) = v(t) \cdot i(t) = \frac{V \cdot I \cdot \cos\varphi}{2} - \frac{V \cdot I \cdot \cos(2\omega t + \varphi)}{2}$$

[see *Figure 28* - 10]

After these two operations, another stage performs the subtraction between the results p2 and p1 and a division by 2, obtaining the active power:

Equation 9

$$p(t) = \frac{(p_2(t) - p_1(t))}{2} = \frac{V \cdot I \cdot \cos\varphi}{2}$$

[see *Figure 28* - 11]

In this way, the AC part V•I•cos(2ωt + φ)/2 has been then removed from the instantaneous power.

In the case of current sensors like “Rogowski coils”, which provide the rate of the instantaneous current signal (di/dt), the initial voltage signal differentiated stage will be switched off. In this case the signals coming from the A/D conversion and their consequent integrations will be:

Equation 10

v(t) = V•sin ωt

$$i'(t) = \frac{di(t)}{dt} = -I \cdot \omega \cdot \cos(\omega t + \varphi)$$

Equation 11

$$V(t) = \int v(t) \cdot dt = -\frac{V}{\omega} \cdot \cos \omega t$$

Equation 12

[

$$(t) = \int i'(t) \cdot dt = i(t) = -I \cdot \sin(\omega t + \varphi)$$

The signals process flow will be the same as shown in the previous case, and even with the formulas above, the result will be the same.

The absence of any AC component allows a very fast calibration procedure: it requires just to set (using the internal device programming registers) the voltage and current sensor conversion constants, using the effective voltage and current (V_{RMS}, I_{RMS}) readings provided by the device built-in communication port, avoiding the time-averaged readings of the active power or need for line synchronization.

8.24.2 Reactive power

The reactive power is produced using the already computed signals. In case of shunt sensor the voltage signal is derived while the current signal is not. A first computation is to multiply DS value of integrated voltage channel with the value of integrated current channel, which yields:

Equation 13

$$Q_1(t) = \int v'(t)dt \cdot I(t) = v(t) \cdot I(t) = (V \sin \omega t) \cdot \left(-\frac{I}{\omega} \cos(\omega t + \varphi \right) = \frac{VI}{2\omega} \cdot (\sin \varphi - \sin(2\omega t + \varphi))$$

The second is to multiply filtered DS value of voltage channel with the value of filtered current channel,

Equation 14

$$Q_2(t) = v'(t) \cdot i(t) = V\omega \cos \omega t \cdot I \sin(\omega t + \varphi) = \frac{VI}{2} \cdot \omega \cdot (\sin \varphi + \sin(2\omega t + \varphi))$$

From the above results, Q1(t) is proportional to 1/ω while Q2(t) is proportional to ω. The correct reactive power would result from the following formula:

Equation 15

$$Q = \frac{1}{2} \cdot Q_1(t) \cdot \omega + Q_2(t) \cdot \frac{1}{\omega} = \frac{VI}{2} \sin \varphi$$

Since the above computation would need significant additional circuitry, the Reactive Power in the STPM01 is calculated using only the Q1(t) multiplied by ω, it means:

Equation 16

$$Q_3(t) = \frac{1}{2} \cdot Q_1(t) \cdot \omega = \frac{VI}{2} \cdot (\sin\varphi - \sin(2\omega t + \varphi))$$

The reactive power will present then a ripple at twice the line frequency. Since the average value of a sinusoid is 0, this ripple does not contribute to the reactive energy calculation over time, moreover, in the STPM01 the reactive power is not used for meter calibration or to generate the stepper pulses, then this ripple will not affect the overall system performances.

In case of Rogowsky coil, the same procedure is applied, but the current channel will be proportional to the derived of the current and the differentiated is bypassed in the voltage channel, so we have:

Equation 17

$$Q_1(t) = \int v(t)dt \cdot \int i'(t)dt = V(t) \cdot i(t) = \left(-\frac{V}{\omega}\cos(\omega t) \right) \cdot (-I\sin(\omega t + \varphi)) = \frac{VI}{2\omega}(\sin\varphi + \sin(2\omega t + \varphi))$$

Equation 18

$$Q_1(t) = v(t) \cdot i'(t) = V\sin\omega t(t) \cdot (-I\omega\cos(\omega t + \varphi)) = -\frac{VI}{2} \cdot \omega \cdot (\sin\varphi - \sin(2\omega t + \varphi))$$

The reactive power is then calculated:

Equation 19

$$Q_3(t) = \frac{1}{2} \cdot Q_1(t) \cdot \omega = \frac{VI}{2} \cdot (\sin\varphi + \sin(2\omega t + \varphi))$$

8.24.3 Apparent power and RMS values

The RMS values are calculated starting from the following formulas.

Shunt or current transformer

Equation 20

$$\sqrt{\frac{1}{T}\int_0^T I^2(t)dt} = \frac{I}{\omega \cdot \sqrt{2}}$$

multiplying *Equation 20* by ω, the I_{RMS} value is obtained:

Equation 21

$$I_{RMS} = \frac{I}{\sqrt{2}}$$

The RMS voltage value is obtained as:

Equation 22

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dt} = \frac{V}{\sqrt{2}}$$

For the apparent power another value is produced:

Equation 23

$$\sqrt{\frac{1}{T}\int_0^T v'^2(t)dt} = \frac{V \cdot \omega}{\sqrt{2}}$$

Multiplying *Equation 20:* and *Equation 23:* , the apparent power is produced:

Equation 24

$$S = \frac{I}{\omega \cdot \sqrt{2}} \cdot \frac{V \cdot \omega}{\sqrt{2}} = \frac{VI}{2}$$

Rogowsky coil

In this case we have:

Equation 25

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i''^2(t)dt} = \frac{I}{\sqrt{2}}$$

while V_{RMS} is calculated as in *Equation 22:* .

The apparent power is simple calculated multiplying *Equation 25:* and *Equation 22:* .

The DSP then performs the integration of the computed powers into energies. These integrators are implemented as up/down counters and they can rollover. 20-bit output buses of the counters are assigned as most significant part of energy data records. It is a responsibility of an application to read the counters at least every second not to miss any rollover.

9 STPM01 calibration

Energy meters based on STPM01 device are calibrated in a fast and easy way. The calibration is essentially based on the single calibration of the voltage and current channel considering their RMS values rather than on the frequency of output pulse signal. When the two channel are calibrated all the other measurement are calibrated too. This allows the calibration to be performed in only one point shortening the production time of the meter. This procedure is possible due to the below key points:

- Device is compound of two independent meter channels for line voltage and current respectively. Each channel includes its own digital calibrator, to adjust the RMS in the range of ±12.5 % in 256 steps, and digital filter, to remove any signal DC component. All final results are not subject to calibration procedure because they are achieved from such corrected signals by mathematical modules implemented by hardwired DSP.
- Device computes different kind of energies: active, reactive and apparent. The active energy is produced without 2nd harmonic of line frequency. It also computes RMS values of measured voltage and current.
- Device produces an energy output pulse signal but information can also be read through serial port interface, SPI, and communication channel.
- Device has an embedded memory, 56 bits, used for configuration and calibration purposes. The value of these bits can be read or they can be changed temporarily or permanently through SPI communication channel.

Let's consider the basic information needed to start the calibration procedure:

Table 18. Working point settings

Line RMS voltage	V_n	(230V)
Line RMS current	I_n	(5A)
Power sensitivity	P	(LED: P=128000 pulses/kWh, stepper motor: PM=P/64= 2000 pulses/kWh)
Shunt sensor	K_S	0,42 mv/A

The following typical STPM01 parameters and constants are also known:

Table 19. Device constants

Parameter		Value	Tolerance
Internal reference voltage	V_{BG}	1.23 V	± 2%
Internal calculation frequency	f_M	2^{23} Hz	± 50 ppm
Amplification of voltage ADC	A_V	4	± 1%
Amplification of current ADC	A_I	8, 16, 24, 32	± 2%
Gain of differentiator	G_{DIF}	0,6135	
Gain of integrator	G_{INT}	0,815	
Gain of decimation filter	G_{DF}	1.004	
RMS voltage register length	B_V	2^{11}	
RMS current register length	B_I	2^{16}	
Constant	D_{UD}	2^{17}	

As shown in *Table 18*, only analog parameter are object of calibration because introduce a certain error. Voltage ADC amplification Av is constant, while Ai is chosen according to used sensors.

The calibration algorithm will firstly calculate the voltage divider ratio and, as final result, the correction parameters, called Kv and Ki, which applied to STPM01 voltage and current measures compensate small tolerances of analog components that affect energy calculation.

Since Kv and Ki calibration parameters are the decimal representation of the corresponding configuration bytes CHV and CHP or CHS (respectively voltage channel, primary current channel and secondary current channel calibration bytes), at the end of calibration CHV and CHP or CHS (according to the current channel under calibration, primary or secondary respectively) bits' values are obtained.

In the following procedure CHV, CHP and CHS will be indicated as Cv and Ci.

Through hardwired formulas Kv and Ki tune measured values varying from 0,75 to 1 in 256 steps, according to the value of Cv and Ci (from 0 to 255).

To obtain the greatest correction dynamic initially calibrators are set in the middle of the range, thus obtaining a calibration range of 12.5 % per voltage or current channel:

Calibrator's value

$$Kv = Ki = 0.875$$

$$Ci = Cv = 128$$

In this way it is possible to tune Kv and Ki having a precise measured: for example Cv = 0 generates a correction factor of -12.5 % (Kv = 0.75) and Cv = 255 determines a correction factor of +12.5 % (Kv = 1), and so on.

According to what pointed out above, the following formulas, which relate Kv, i and Cv, i are obtained:

$$Kv,i = (Cv,i/128) * 0.125 + 0.75$$

$$Cv,i = 1024 * Kv,i - 768.$$

The calibration procedure will output Cv and Ci values that will allow the above power sensitivity of the meter.

This sensitivity is used to calculate target frequency at LED pin for nominal voltage and current values:

$$X_F = f * 64;$$

with:

$$f = PM * In * Vn / 3600000;$$

From values above and for both chosen amplification factor A_I=32 and initial calibration data, the following target values can be calculated:

Target RMS reading for given In:

$$X_I = In * K_S * A_I * Ki * G_{INT} * G_{DF} * G_{DIF} * B_I / (V_{BG} * 1000) = 1573$$

Target RMS reading for given Vn:

$$X_V = f * B_V * B_I * D_{UD} / (f_M * X_I) = 852$$

The output of the voltage divider is then:

$$V_{DIV} = (X_V * V_{BG})/ (2 * G_{DIF} * A_V * Kv * G_{DF} * G_{INT} * B_V)= 145,6 \text{ mV}$$

Choosing R2 = 500 Ω (connected between V_I and V_{SS}), the R1 resistor (connected between V_{LINE} and V_{IP}) value is obtained:

$$R1 = R2 * (Vn - V_{DIV}) / V_{DIV} = 789,3\ \Omega$$

Indicating with I_A and V_A the real readings on the STPM01 RMS registers of voltage and current, and with X_I and X_V ideal values of RMS current and voltage readings already calculated, the final values for calibrators can be calculated as:

$$X_V = (Kv * V_A) / 0.875$$

$$X_I = (Ki * I_A) / 0.875$$

If the computed final calibration data would fall out of calibration data range, the energy meter should be recognized as bad or the given presumptions and calculations above should be checked. Otherwise, if the final data of calibrators would be written into energy meter, the RMS readings should be very close to target values I and V and the frequency of LED output should be very close to target value f.

10 Application design

The choice of the external components in the transduction section of the application is a crucial point in the application design, affecting the precision and the resolution of the whole system.

Among the several considerations, a compromise has to be found between the following needs:

1. Maximize the signal to noise ratio in the voltage channel,
2. Choose the current to voltage conversion ratio Ks and the voltage divider ratio in a way that calibration can be achieved (please refer to AN2299)
3. Choose Ks to take advantage of the whole current dynamic range according to desired maximum current and resolution.

To maximize the signal to noise ratio of the current channel the voltage divider resistors ratio should be as close as possible to those shown in *Table 20*.

Table 20. Resistor divider ratio

Function	Component	Parameter	Value	Unit
Line voltage interface	Resistor divider	R to R ratio V_{RMS}=230V	1650	V/V
		R to R ratio V_{RMS}=110V	830	

The *Figure 29* below shows a reference schematic for an application with the following properties:

- P = 64000 imp/KWh
- I_{NOM} = 5 A
- I_{MAX} = 60 A.

Typical values for the current sensors sensitivity, also used in the reference schematic below, are shown in *Table 21*.

Table 21. Current channel typical components

Function	Component	Parameter	Value	Unit
Line current interface	Current shunt	Current to voltage conversion ratio Ks	0.425	mV/A
	Current transformer		1.7	
	Rogowsky coil		0.13	

Note: If the device is used in configuration PST = 7 (primary channel with CT, secondary channel with Shunt), the shunt Ks must always be equal to one fourth of the current transformer Ks.

Additional considerations on the application design, suggestions for noise and crosstalk reduction can be found in the AN2317.

Figure 29. STPM01 reference schematic with one current transformer and one shunt

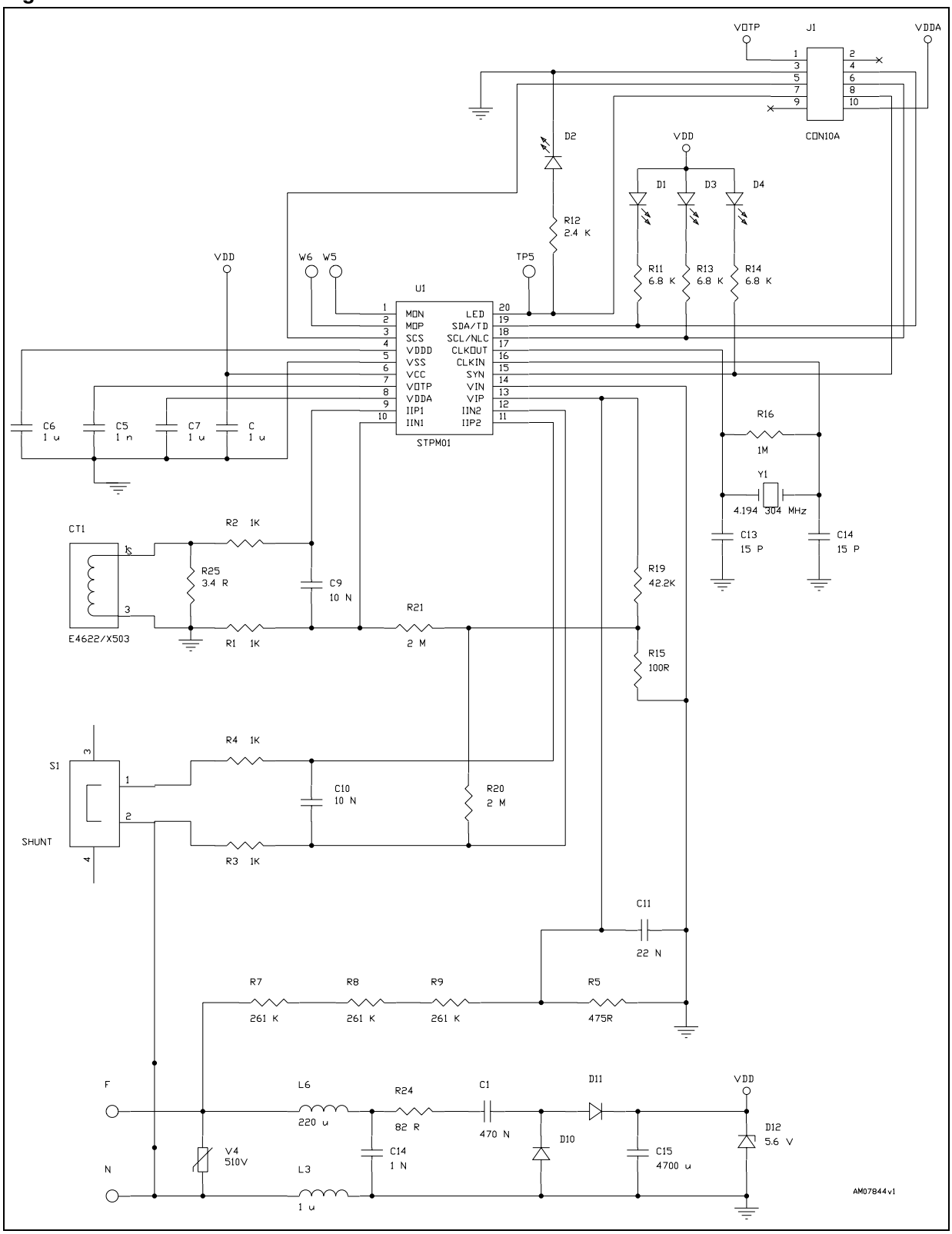
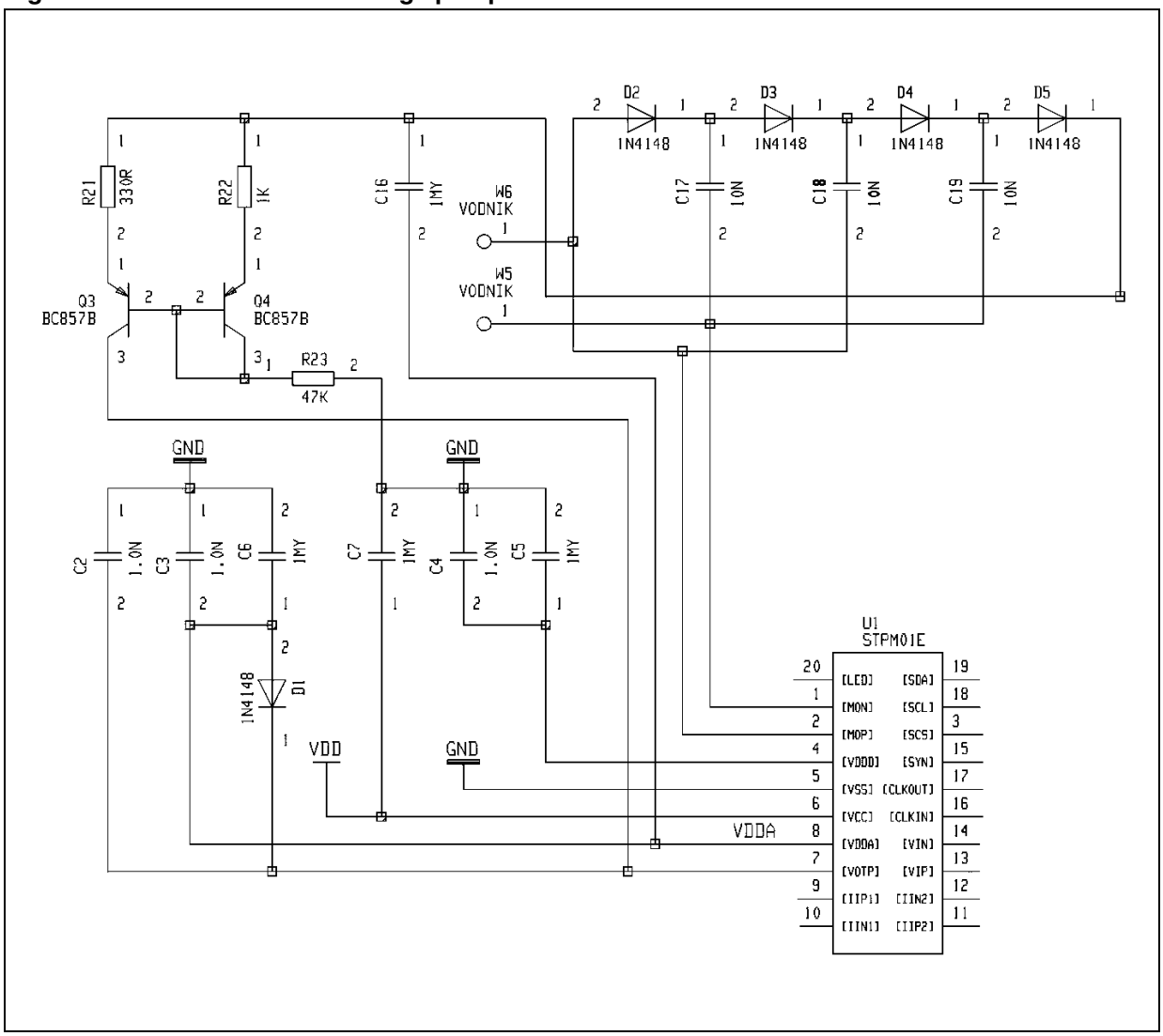


Figure 30. STPM01 with 3X charge pump DC-DC converter

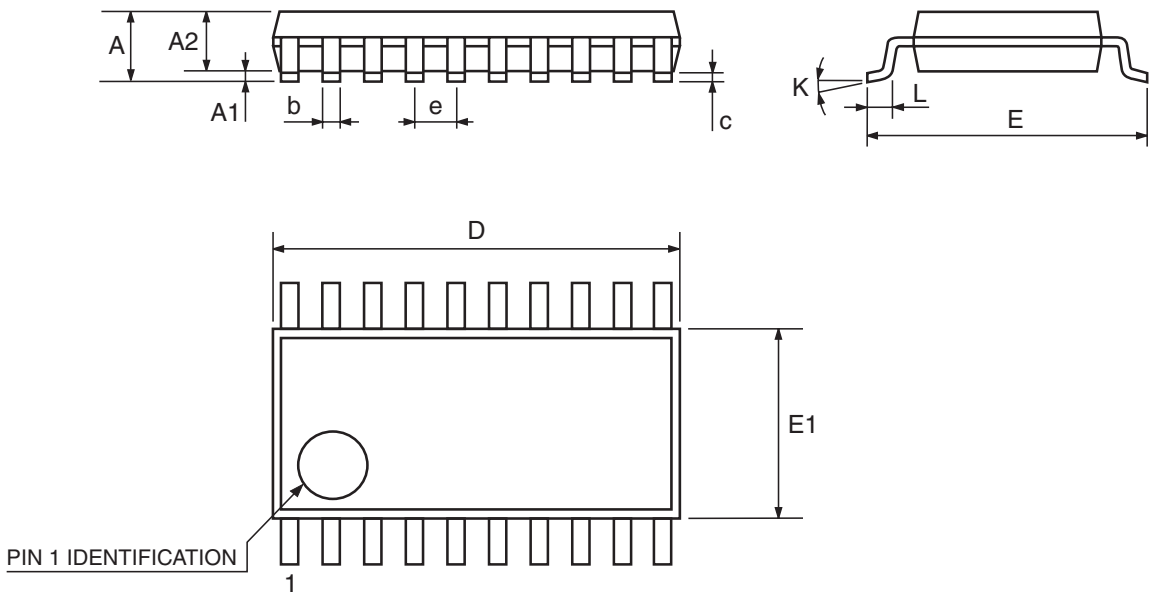


11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

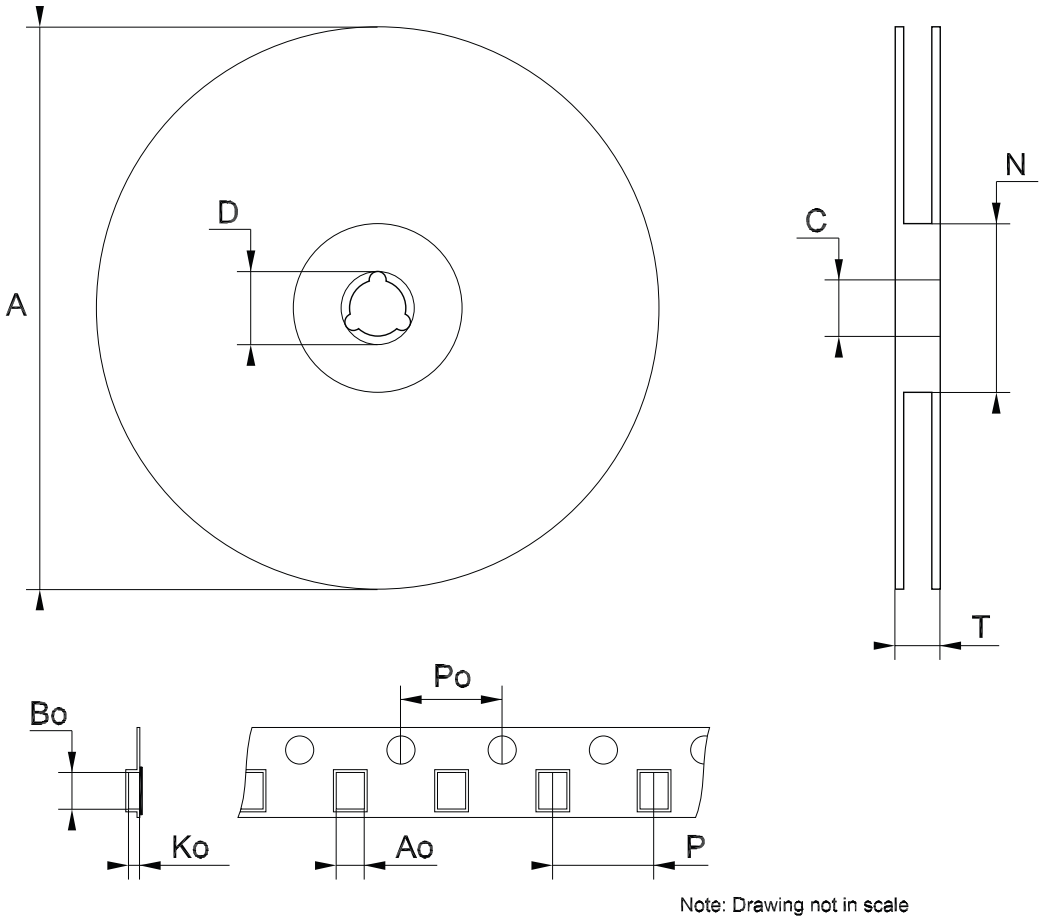
TSSOP20 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & reel TSSOP20 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

12 Revision history

Table 22. Document revision history

Date	Revision	Changes
28-Sep-2004	1	Preliminary data.
22-Dec-2005	2	Document updated.
24-Oct-2006	3	The chapter 9 updated.
06-Feb-2006	4	Modified *Figure 11*.
12-Jan-2009	5	Modified address 11 *Table 16 on page 34*.
03-Apr-2009	6	Modified *Figure 20 on page 27*.
19-Oct-2010	7	Added *Chapter 8.12.1: RC Startup procedure on page 27*, *Chapter 10: Application design on page 53*, modified *Chapter 8.10: Tamper detection module on page 24*, *Chapter 8.5: Period and line voltage measurement on page 20*.
09-Jun-2011	8	Modified: *Table 7 on page 11*.

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