# A4940

# Automotive Full Bridge MOSFET Driver

## Not for New Design

These parts are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: December 5, 2018

**Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales*

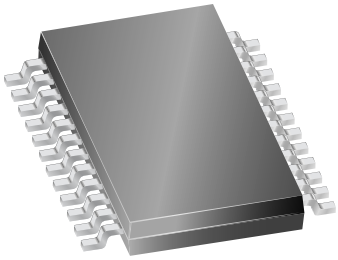
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

# Automotive Full Bridge MOSFET Driver

## FEATURES AND BENEFITS

- High current gate drive for N-channel MOSFET full bridge
- Independent control of each MOSFET
- Charge pump for low supply voltage operation
- Cross-conduction protection with adjustable dead time
- 5.5 to 50 V supply voltage range
- Diagnostics output
- Low current sleep mode

## PACKAGE: 24-pin TSSOP with exposed thermal pad (suffix LP)



*Not to scale*

## DESCRIPTION

The A4940 is a full-bridge controller for use with external N-channel power MOSFETs and is specifically designed for automotive applications with high-power inductive loads such as brush DC motors.

A unique charge pump regulator provides full ( >10 V ) gate drive for battery voltages down to 7 V and allows the A4940 to operate with a reduced gate drive, down to 5.5 V.

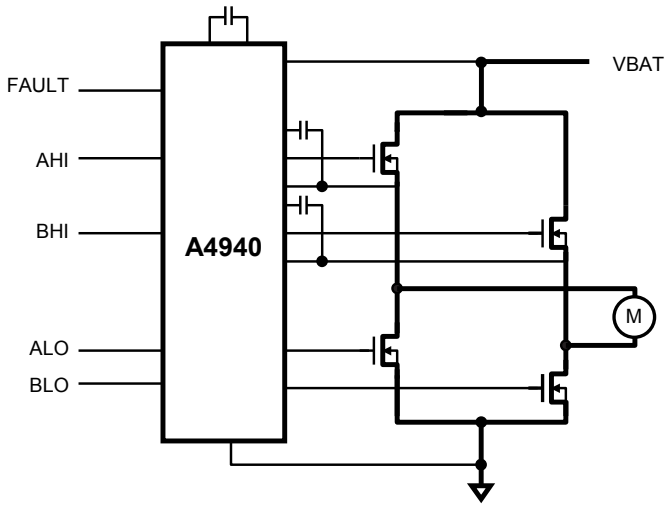
A bootstrap capacitor is used to provide the above battery supply voltage required for N-channel MOSFETs. A unique bootstrap charge management system ensures that the bootstrap capacitor is always sufficiently charged to supply the high-side gate drive circuit.

Each of the power MOSFETs is controlled independently but all are protected from shoot-through by dead time that is user-configured by an external resistor.

Integrated diagnostics provide indication of undervoltage and overtemperature faults.

The A4940 is supplied in a 24-pin TSSOP power package with an exposed pad for enhanced thermal dissipation (package type LP). It is lead (Pb) free, with 100% matte tin leadframe plating (suffix –T).

## Typical Application



## Selection Guide

| Part Number | Packing |
|---|---|
| A4940KLPTR-T | 4000 pieces per reel |

## Absolute Maximum Ratings*

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Load Supply Voltage | $V_{BB}$ | | –0.3 to 50 | V |
| Logic Supply Voltage | $V_{DD}$ | | –0.3 to 7 | V |
| Logic Inputs | $V_I$ | | –0.3 to 6.5 | V |
| Logic Outputs | $V_O$ | | –0.3 to 6.5 | V |
| Pin VREG | $V_{VREG}$ | | –0.3 to 16 | V |
| Pins CP1, CP2 | $V_{CPX}$ | | –0.3 to 16 | V |
| Pin RDEAD | $V_{RDEAD}$ | | –0.3 to 6.5 | V |
| Pins SA, SB | $V_{SX}$ | | –5 to 55 | V |
| Pins GHA, GHB | $V_{GHX}$ | | $V_{SX}$ to $V_{SX}$ + 15 | V |
| Pins GLA, GLB | $V_{GLX}$ | | –5 to 16 | V |
| Pins CA, CB | $V_{CX}$ | | –0.3 to $V_{SX}$+15 | V |
| ESD Rating, Human Body Model | | AEC Q100-002, all pins | 2000 | V |
| ESD Rating, Charged Device Model | | AEC Q100-011, all pins | 1000 | V |
| Ambient Operating Temperature Range | $T_A$ | Range K | –40 to 150 | °C |
| Continuous Junction Temperature | $T_J$(max) | | 150 | °C |
| Transient Junction Temperature | $T_{Jt}$ | Overtemperature event not exceeding 10 s, lifetime duration not exceeding 10 hr, guaranteed by design characterization | 175 | °C |
| Storage Temperature Range | $T_{stg}$ | | –55 to 150 | °C |

*With respect to ground

**Thermal Characteristics** may require derating at maximum conditions, see application information

| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | On 4-layer PCB based on JEDEC standard | 28 | ºC/W |
| | | On 2-layer PCB with 3.8 in.$^2$ of copper area each side | 100 | ºC/W |
| Package Thermal Resistance, Junction to Pad | $R_{\theta JP}$ | | 2 | ºC/W |

*Additional thermal information available on the Allegro website



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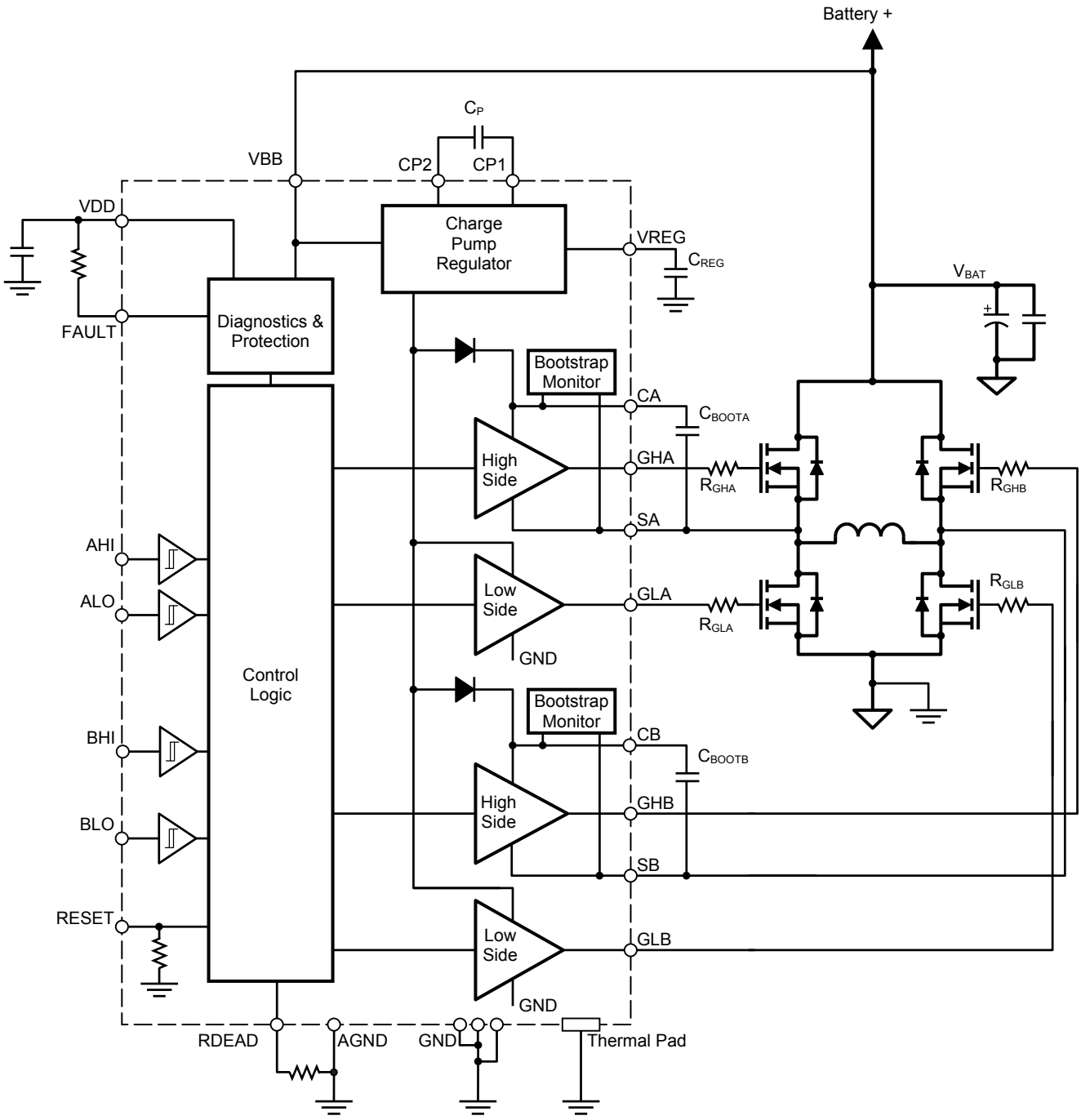
## Functional Block Diagram



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**ELECTRICAL CHARACTERISTICS** Valid at $T_J$ = –40°C to 150°C, $V_{BB}$ = 7 to 50 V, $V_{DD}$ = 3 to 5.5 V; unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply and Reference** | | | | | | |
| $V_{BB}$ Functional Operating Range[1] | $V_{BB}$ | | 5.5 | – | 50 | V |
| $V_{DD}$ Range | $V_{DD}$ | | 3 | – | 5.5 | V |
| $V_{BB}$ Quiescent Current | $I_{BBQ}$ | RESET = high, GHx, GLx = low, $V_{BB}$ = 12 V | – | 1 | 2 | mA |
| | $I_{BBS}$ | RESET= low, $V_{BB}$ = 12 V | – | – | 10 | µA |
| $V_{DD}$ Quiescent Current | $I_{VDDQ}$ | RESET = high, outputs low | – | 2 | 4 | mA |
| | $I_{VDDS}$ | RESET = low | – | – | 10 | µA |
| VREG Output Voltage | $V_{REG}$ | $V_{BB}$ > 9 V, $I_{REG}$ = 0 to 8 mA | 12.65 | 13 | 13.9 | V |
| | | 7.5 V < $V_{BB}$ ≤ 9 V, $I_{REG}$ = 0 to 6 mA | 12.65 | 13 | 13.9 | V |
| | | 6 V < $V_{BB}$ ≤ 7.5 V, $I_{REG}$ = 0 to 5 mA | $2 \times V_{BB}$ – 2.5 | – | – | V |
| | | 5.5 V < $V_{BB}$ ≤ 6 V, $I_{REG}$ < 4 mA | 8.5 | 9.5 | – | V |
| Bootstrap Diode Forward Voltage | $V_{fBOOT}$ | $I_D$ = 10 mA | 0.4 | 0.7 | 1.0 | V |
| | | $I_D$ = 100 mA | 1.5 | 2.2 | 2.8 | V |
| Bootstrap Diode Resistance | $r_D$ | $r_{D(100mA)}$ = ($V_{fBOOT(150mA)} – V_{fBOOT(50mA)}$) / 100 mA | 6 | 10 | 20 | Ω |
| Bootstrap Diode Current Limit | $I_{DBOOT}$ | | 250 | 500 | 750 | mA |
| **Gate Output Drive** | | | | | | |
| Turn-On Time | $t_r$ | $C_{LOAD}$ = 1 nF, 20% to 80% points | – | 35 | – | ns |
| Turn-Off Time | $t_f$ | $C_{LOAD}$ = 1 nF, 80% to 20% points | – | 20 | – | ns |
| Pull-up On Resistance | $R_{DS(on)UP}$ | $T_J$ = 25°C, $I_{GHX}$ = –150 mA | 8 | 11 | 16 | Ω |
| | | $T_J$ = 150°C, $I_{GHX}$ = –150 mA | 13 | 18.5 | 24 | Ω |
| Pull-down On Resistance | $R_{DS(on)DN}$ | $T_J$ = 25°C, $I_{GLX}$ = –150 mA | 3 | 6 | 8 | Ω |
| | | $T_J$ = 150°C, $I_{GLX}$ = –150 mA | 6 | 9 | 12 | Ω |
| GHx Output Voltage | $V_{GH}$ | Bootstrap capacitor fully charged | $V_{CX}$ – 0.2 | – | – | V |
| GLx Output Voltage | $V_{GL}$ | | $V_{REG}$ – 0.2 | – | – | V |
| Turn-Off Propagation Delay[2] | $t_{p(off)}$ | Input change to unloaded gate output change | 60 | 90 | 150 | ns |
| Turn-On Propagation Delay[2] | $t_{p(on)}$ | Input change to unloaded gate output change | 60 | 90 | 150 | ns |
| Propagation Delay Matching - Phase to Phase | $\Delta t_{PP}$ | Same phase change | – | 10 | – | ns |
| Propagation Delay Matching - On to Off | $\Delta t_{OO}$ | Single phase | – | 10 | – | ns |
| Dead Time[2] | $t_{DEAD}$ | RDEAD tied to GND | – | 0 | – | ns |
| | | $R_{DEAD}$ = 3 kΩ | – | 180 | – | ns |
| | | $R_{DEAD}$ = 30 kΩ | 815 | 960 | 1150 | ns |
| | | $R_{DEAD}$ = 240 kΩ | – | 3.5 | – | µs |
| | | RDEAD tied to VDD | – | 6 | – | µs |

*Continued on the next page…*



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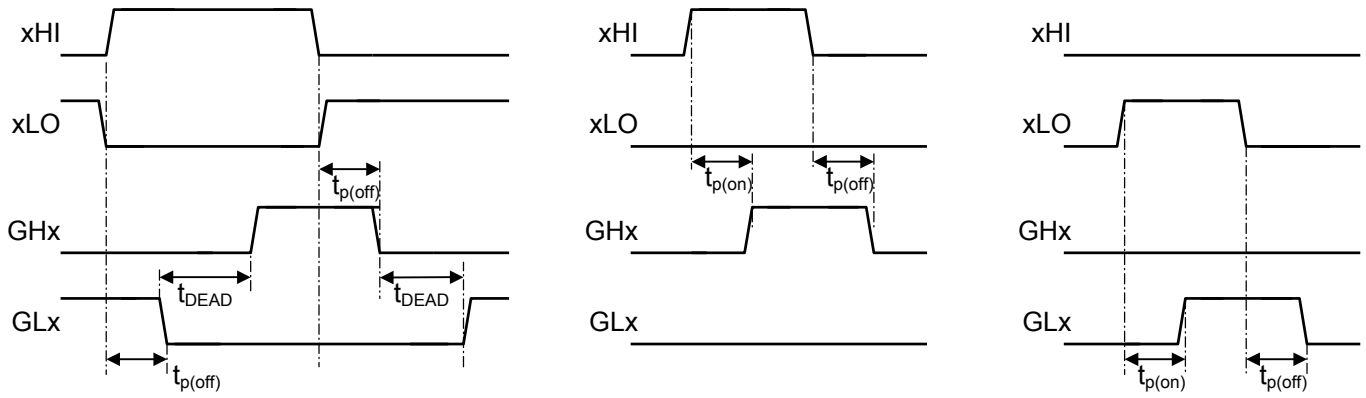
**ELECTRICAL CHARACTERISTICS (continued)** Valid at $T_J$ = –40°C to 150°C, $V_{BB}$ = 7 to 50 V, $V_{DD}$ = 3 to 5.5 V; unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Logic Inputs and Outputs** | | | | | | |
| FAULT Output (Open drain) | $V_{OL}$ | $I_{FAULTOL}$ = 1 mA, fault present | – | – | 0.4 | V |
| FAULT Output Leakage Current[3] | $I_{OH}$ | $V_{FAULTO}$ = 5 V, fault not present | –1 | – | 1 | µA |
| RDEAD Current[3] | $I_{DEAD}$ | RDEAD = GND | –200 | – | –70 | µA |
| Input Low Voltage | $V_{IL}$ | | – | – | $0.3 \times V_{DD}$ | V |
| Input High Voltage | $V_{IH}$ | | $0.7 \times V_{DD}$ | – | – | V |
| Input Hysteresis | $V_{IHYS}$ | | 300 | 500 | – | mV |
| Input Current (Except RESET)[3] | $I_{IN}$ | $0 V < V_{IN} < V_{DD}$ | –1 | – | 1 | µA |
| Input Pull-down Resistor (RESET) | $R_{PD}$ | | – | 50 | – | kΩ |
| RESET Pulse Time | $t_{RES}$ | | 0.1 | | 3.5 | µs |
| **Protection** | | | | | | |
| VREG Undervoltage Lockout | $V_{REGUVON}$ | $V_{REG}$ rising | 7.5 | 8 | 8.5 | V |
| | $V_{REGUVOFF}$ | $V_{REG}$ falling | 6.6 | 7.1 | 7.6 | V |
| Bootstrap Undervoltage | $V_{BOOTUV}$ | $V_{BOOT}$ falling, $V_{CX} – V_{SX}$ | 59 | – | 69 | $\%V_{REG}$ |
| Bootstrap Undervoltage Hysteresis | $V_{BOOTUVHYS}$ | | – | 20 | – | $\%V_{REG}$ |
| VDD Undervoltage Turn-Off | $V_{DDUV}$ | $V_{DD}$ falling | 2.45 | 2.7 | 2.85 | V |
| VDD Undervoltage Hysteresis | $V_{DDUVHYS}$ | | 50 | 100 | 150 | mV |
| Overtemperature Flag | $T_{JF}$ | Temperature increasing | 150 | 170 | – | ºC |
| Overtemperature Hysteresis | $T_{JFHYS}$ | Recovery = $T_{JF} – T_{JFHYS}$ | – | 15 | – | ºC |

[1]Function is correct, but parameters are not guaranteed below the general limit (7 V).
[2]See Gate Drive Timing.
[3]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

## Gate Drive Timing Diagrams




Complementary High side only Low side only



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## Functional Description

The A4940 is a full-bridge MOSFET driver (pre-driver) requiring an unregulated supply of 7 to 50 V and a logic supply from 3 to 5.5 V.

The four gate drives can drive a wide range of N-channel power MOSFETs and are configured as two high-side drives and two low-side drives. The A4940 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external MOSFETs are above 10 V, at supply voltages down to 7 V. For extreme battery voltage drop conditions, correct functional operation is guaranteed at supply voltages down to 5.5 V, but with a reduced gate drive voltage.

The A4940 provides the interface between the logic level outputs of a microcontroller and the high current, high voltage gate drive for N-channel power MOSFETs in a full-bridge configuration. Typically, the power full bridge will be used for brush DC motor control or other high current inductor loads. Each MOSFET in the bridge is controlled by an independent logic level input compatible with 3.3 or 5 V logic outputs. Cross-conduction (shoot-through) in the external bridge is avoided by an adjustable dead time.

A low power sleep mode allows the A4940, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The A4940 provides a single fault flag to indicate undervoltage and overtemperature conditions.

### Power Supplies

Two power supply connections are required, one for the logic interface, and one for the analog and output drive sections. The logic supply, connected to VDD, allows the flexibility of a 3.3 or 5 V logic interface. The main power supply should be connected to VBB through a reverse voltage protection circuit. Both supplies should be decoupled with ceramic capacitors connected close to the supply and ground pins.

The A4940 operates within specified parameters with a VBB supply from 7 to 50 V and will function correctly with a supply down to 5.5 V. This provides a very rugged solution for use in the harsh automotive environment.

### Gate Drives

The A4940 is designed to drive external, low on-resistance, power N-channel MOSFETs. It supplies the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the MOSFET during switching. The charge and discharge rate can be controlled using an external resistor in series with the connection to the gate of the MOSFET.

**Gate Drive Voltage Regulation** The gate drives are powered by an internal regulator, which limits the supply to the drives and therefore the maximum gate voltage. When the VBB supply is greater than about 16 V, the regulator is a simple linear regulator. Below 16 V, the regulated supply is maintained by a charge pump boost converter, which requires a pump capacitor connected between the CP1 and CP2 pins. This capacitor must have a minimum value of 220 nF and is typically 470 nF.

The regulated voltage, 13 V typical, is available on the VREG pin. A sufficiently large storage capacitor must be connected to this pin to provide the transient charging current to the low-side drives and the bootstrap capacitors.

**GLA and GLB Pins** These are the low-side gate drive outputs for the external N-channel MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby providing some control of the di/dt and dv/dt of the SA and SB outputs. GLx going high turns on the upper half of the drive, sourcing current to the gate of the low-side MOSFET in the external power bridge, turning it on. GLx going low turns on the lower half of the drive, sinking current from the external MOSFET gate circuit to GND pin, turning off the MOSFET.

**SA and SB Pins** Directly connected to the motor, these terminals sense the voltages switched across the load. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drives. The discharge current from the high-side MOSFET gate capacitance flows through these connections, which should have low impedance circuit connections to the MOSFET bridge.

**GHA and GHB Pins** These terminals are the high-side gate drive outputs for the external N-channel MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the SA and SB outputs. GHx going high turns



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on the upper half of the drive, sourcing current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx going low turns on the lower half of the drive, sinking current from the external MOSFET gate circuit to the corresponding Sx pin, turning off the MOSFET.

**CA and CB Pins** These are the high-side connections for the bootstrap capacitors and are the positive supply for the high-side gate drives. The bootstrap capacitors are charged to approximately $V_{REG}$ when the associated output Sx terminal is low. When the Sx output swings high, the charge on the bootstrap capacitor causes the voltage at the corresponding Cx terminal to rise with the output to provide the boosted gate voltage needed for the high-side MOSFETs.

**RDEAD Pin** This pin controls internal generation of dead time during MOSFET switching. Cross-conduction is prevented by the gate drive circuits, which introduce a dead time, $t_{DEAD}$, between switching one MOSFET off and the complementary MOSFET on.

- When an external resistor greater than 3 kΩ is connected between RDEAD and AGND, the dead time is derived from the resistor value.
- When RDEAD is connected directly to VDD, $t_{DEAD}$ defaults to a value of 6 µs typical.

### Logic Control Inputs

Four low voltage-level digital inputs provide control for the gate drives. These logic inputs all have a typical hysteresis of 500 mV to improve noise performance. They provide individual direct control over each power MOSFET, subject to cross-conduction prevention, and can be used together to provide fast decay or slow decay with high-side or low-side recirculation.

**AHI, ALO, BHI and BLO Pins** These directly control the gate drives. The xHI inputs control the high-side drives and the xLO inputs control the low-side drives. Internal lockout logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously. Table 1 shows the logic truth table.

**RESET Pin** This is an active-low input, and when active it allows the A4940 to enter sleep mode. When RESET is held low, the regulator and all internal circuitry are disabled and the A4940 enters sleep mode. Before fully entering sleep mode, there is a short delay while the regulator decoupling and storage capacitors discharge. This typically takes a few milliseconds, depending on the application conditions and component values.

During sleep mode, current consumption from the VBB supply is reduced to a minimal level. In addition, latched faults and the corresponding fault flags are cleared. When the A4940 is coming out of sleep mode, the protection logic ensures that the gate drive outputs are off until the charge pump reaches its correct operating condition. The charge pump stabilizes in approximately 3 ms under nominal conditions.

RESET can be used also to clear latched fault flags without entering sleep mode. To do so, hold RESET low for the reset pulse time, $t_{RES}$. This clears the latched bootstrap capacitor undervoltage fault that disables the outputs.

Note that the A4940 can be configured to start without any external logic input. To do so, pull up the RESET pin to $V_{BB}$ by means of an external resistor. The resistor value should be between 20 and 33 kΩ.

### Diagnostics

Several diagnostic features are integrated into the A4940 to provide indication of fault conditions. In addition to system wide faults such as undervoltage and overtemperature, the A4940 integrates individual bootstrap voltage monitors for each bootstrap capacitor.

**Table 1. Input Logic**

| Pin Setting | | | | | | Mode of Operation |
|---|---|---|---|---|---|---|
| RESET | xHI | xLO | GHx | GLx | Sx | |
| H | H | L | H | L | H | High side MOSFET conducting |
| H | L | H | L | H | L | Low Side MOSFET conducting |
| H | H | H | L | H | L | Low Side MOSFET conducting – cross-conduction prevention |
| H | L | L | L | L | Z | High side and low side off |
| L | x | x | Z | Z | Z | All gate drives inactive, all MOSFETs off |



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**FAULT Pin** This is an open drain output fault flag, which indicates a fault condition by its state, as shown in table 2. It must be pulled to $V_{DD}$ with an external resistor, typically 10 to 47 kΩ.

### Fault States

**Overtemperature** If the junction temperature exceeds the over-temperature threshold, 170°C typical, the A4940 will enter the overtemperature fault state and FAULT will go low. The overtemperature fault state, and FAULT, will only be cleared when the temperature drops below the recovery level defined by $T_{JF} - T_{JFHYS}$.

No circuitry will be disabled. External control circuits must take action to limit the power dissipation in some way so as to prevent overtemperature damage to the A4940 chip and unpredictable device operation.

**VREG Undervoltage** VREG supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are sufficiently high before enabling any of the outputs. If the voltage at VREG, $V_{REG}$, drops below the falling VREG undervoltage lockout threshold, $V_{REGUVOFF}$, then the A4940 will enter the VREG undervoltage fault state. In this fault state FAULT will be low, and the outputs will be disabled. The VREG undervoltage fault state and the fault flags will be cleared when VREG rises above the rising VREG undervoltage lockout threshold, $V_{REGUVON}$.

The VREG undervoltage monitor circuit is active during power-up, and the A4940 remains in the VREG undervoltage fault state until VREG is greater than the rising VREG undervoltage lockout threshold, $V_{REGUVON}$.

**Bootstrap Capacitor Undervoltage** The A4940 monitors the voltage across the individual bootstrap capacitors to ensure they have sufficient charge to supply the current pulse for the high-side drive. Before a high-side drive can be turned on, the voltage across the associated bootstrap capacitor must be higher than the turn-on voltage limit. If this is not the case, then the A4940 will start a bootstrap charge cycle by activating the complementary low-side drive. Under normal circumstances, this will charge the bootstrap capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled.

The bootstrap voltage monitor remains active while the high-side drive is active and, if the voltage drops below the turn-off voltage, a charge cycle will be initiated.

In either case, if there is a fault that prevents the bootstrap capacitor charging, then the charge cycle will timeout, FAULT will be low, and the outputs will be disabled. The bootstrap undervoltage fault state remains latched until RESET is set low.

**VDD Undervoltage** The logic supply at VDD is monitored to ensure correct logical operation. If the voltage at VDD, $V_{DD}$, drops below the falling VDD undervoltage lockout threshold, $V_{DDUVOFF}$, then the A4940 will enter the VDD undervoltage fault state. In this fault state, FAULT will be low, and the outputs will be disabled. In addition, because the state of other reported faults cannot be guaranteed, all fault states are reset and replaced by a VDD undervoltage fault state. For example, a VDD undervoltage will reset an existing boostrap undervoltage fault condition and replace it with a VDD undervoltage fault. The VDD undervoltage fault state and the fault flag will be cleared when $V_{DD}$ rises above the rising VDD undervoltage lockout threshold defined by $V_{DDUVOFF} + V_{DDUVHYS}$.

The VDD undervoltage monitor circuit is active during power-up, and the A4940 remains in the VDD undervoltage fault state until $V_{DD}$ is greater than the rising VDD undervoltage lockout threshold, $V_{DDUVOFF} + V_{DDUVHYS}$.

**Table 2. Fault Definitions**

| FAULT Pin Setting | Fault Description | Disable Outputs* | Fault Latched |
|---|---|---|---|
| High | No Fault | No | – |
| Low | Overtemperature | No | No |
| Low | VDD undervoltage | Yes | No |
| Low | VREG undervoltage | Yes | No |
| Low | Bootstrap undervoltage | Yes | Yes |

*Yes indicates all gate drives low, and all MOSFETs off.



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## Application Information

### Dead Time

To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead time delay, $t_{DEAD}$, between a high-side or low-side turn-off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time; for example, when using synchronous rectification or after a bootstrap capacitor charging cycle. In the A4940, the dead time for both phases is set by a single dead-time resistor, $R_{DEAD}$, between the RDEAD and AGND pins.

For $R_{DEAD}$ between 3 and 240 kΩ at 25°C, the value of $t_{DEAD}$ (ns), can be approximated by:

$$t_{DEAD} \approx 50 + \frac{7200}{1.2 + (200 / R_{DEAD})}$$

where $R_{DEAD}$ is in kΩ. Figure 1 illustrates the relationship of $t_{DEAD}$ and $R_{DEAD}$, with the greatest accuracy obtained for values of $R_{DEAD}$ between 6 and 60 kΩ.

The $I_{DEAD}$ current can be estimated by:

$$I_{DEAD} \approx \frac{1.2}{R_{DEAD}}$$

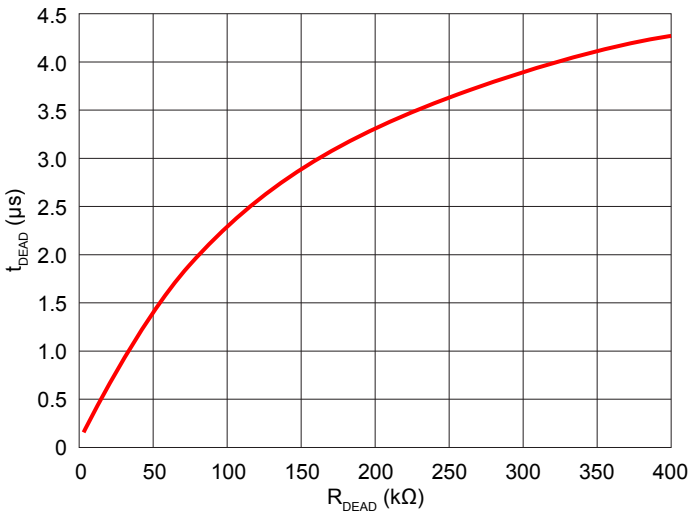


Figure 1. Dead time versus values of $R_{DEAD}$ (full range).

The maximum dead time of 6 µs typical can be set by connecting the RDEAD pin directly to VDD.

Alternatively, the dead time in the A4940 can be disabled by connecting the RDEAD pin directly to GND. In this case the required dead time must be supplied by the external controller.

The choice of power MOSFET and external series gate resistance determine the selection of the dead-time resistor, $R_{DEAD}$. The dead time should be long enough to ensure that one MOSFET in a phase has stopped conducting before the complementary MOSFET starts conducting. This should also take into account the tolerance and variation of the MOSFET gate capacitance, the series gate resistance, and the on-resistance of the A4940 internal drives.

Dead time will be present only if the on-command for one MOSFET occurs within $t_{DEAD}$ after the off-command for its complementary MOSFET. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time will not occur. In this case the gate drive will turn on within the specified propagation delay after the corresponding phase input goes high. (Refer to the Gate Drive Timing diagrams.)

### Braking

The A4940 can be used to perform dynamic braking by forcing all low-side MOSFETs on and all high-side MOSFETs off (ALO=BLO=1, AHI=BHI=0) or, conversely, by forcing all low-side off and all high-side on (ALO=BLO=0, AHI= BHI=1). This effectively short-circuits the back EMF of the motor, creating a breaking torque.

During braking, the load current can be approximated by:

$$I_{BRAKE} \approx \frac{V_{bemf}}{R_L}$$

where $V_{bemf}$ is the voltage generated by the motor and $R_L$ is the resistance of the phase winding.

Care must be taken during braking to ensure that maximum ratings of the power MOSFETs are not exceeded. Dynamic braking is equivalent to slow decay with synchronous rectification.



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### Bootstrap Capacitor Selection

The bootstrap capacitors, CBOOTx, must be correctly selected to ensure proper operation of the A4940. If the capacitances are too high, time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and the PWM frequency. If the capacitances are too low, there can be a large voltage drop at the time the charge is transferred from CBOOTx to the MOSFET gate, due to charge sharing.

To keep this voltage drop small, the charge in the bootstrap capacitor, $Q_{BOOT}$, should be much larger than the charge required by the gate of the MOSFET, $Q_{GATE}$. A factor of 20 is a reasonable value, and the following formula can be used to calculate the value for $C_{BOOT}$:

$$\begin{aligned} Q_{BOOT} &= C_{BOOT} \times V_{BOOT} \\ &= Q_{GATE} \times 20 \end{aligned}$$

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where $V_{BOOT}$ is the voltage across the bootstrap capacitor.

The voltage drop across the bootstrap capacitor as the MOSFET is being turned on, ΔV, can be approximated by:

$$\Delta V \approx \frac{Q_{GATE}}{C_{BOOT}}$$

So for a factor of 20, ΔV would be approximately 5% of $V_{BOOT}$.

The maximum voltage across the bootstrap capacitor under normal operating conditions is $V_{REG}$(max). In most applications, with a good ceramic capacitor the working voltage can be limited to 16 V.

### Bootstrap Charging

It is good practice to ensure the high side bootstrap capacitor is completely charged before a high side PWM cycle is requested. The time required to charge the capacitor, $t_{CHARGE}$ (µs), is approximated by:

$$t_{CHARGE} \approx \frac{C_{BOOT} \times \Delta V}{100}$$

where $C_{BOOT}$ is the value of the bootstrap capacitor, in nF, and ΔV is the required voltage of the bootstrap capacitor.

At power-up and when the drives have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx pin is pulled low and current flows from VREG through the internal bootstrap diode circuit to CBOOT.

### Bootstrap Charge Management

The A4940 provides automatic bootstrap capacitor charge management. The bootstrap capacitor voltage for each phase is continuously checked to ensure that it is above the bootstrap under-voltage threshold, $V_{BOOTUV}$. If the bootstrap capacitor voltage drops below this threshold, when the corresponding high-side is active, the A4940 will turn on the necessary low-side MOSFET, and continue charging until the bootstrap capacitor exceeds the undervoltage threshold plus the hysteresis, $V_{BOOTUV} + V_{BOOTUVHYS}$.

If the bootstrap capacitor voltage is below the threshold, when the corresponding high-side is commanded to turn on, the A4940 will not attempt to turn on the high-side MOSFET, but will turn on the necessary low-side MOSFET to charge the bootstrap capacitor until it exceeds the undervoltage threshold plus the hysteresis.

The minimum charge time is typically 7 µs, but may be longer for very large values of bootstrap capacitor (>1000 nF). If the bootstrap capacitor voltage does not reach the threshold within approximately 200 µs, an undervoltage fault will be flagged.

### VREG Capacitor Selection

The internal reference, $V_{REG}$, supplies current for the low-side gate drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn on the MOSFET quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator, and must be supplied by an external capacitor connected to the VREG pin.

The turn-on current for the high-side MOSFET is similar in value to that for the low-side MOSFET, but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from the VREG regulator output. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This requires that the value of the capacitor connected between VREG and AGND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge. A value of 20 × $C_{BOOT}$ is a reasonable value. The maximum working voltage will never exceed $V_{REG}$, so the capacitor can be rated as low as 15 V. This capacitor should be placed as close as possible to the VREG pin.



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### Supply Decoupling

Because this is a switching circuit, there are current spikes from all supplies at the switching points. As with all such circuits, the power supply connections should be decoupled with a ceramic capacitor, typically 100 nF, between the supply pin and ground. These capacitors should be connected as close as possible to the device supply pins, VDD and VBB, and the ground pin, GND.

### Power Dissipation

In applications where a high ambient temperature is expected the on-chip power dissipation may become a critical factor. Careful attention should be paid to ensure the operating conditions allow the A4940 to remain in a safe range of junction temperature.

The power consumed by the A4940, $P_D$, can be estimated by :

$$P_D = P_{BIAS} + P_{CPUMP} + P_{SWITCHING}$$

given

$$P_{BIAS} = V_{BB} \times I_{BB}$$

$$P_{CPUMP} = [(2 \times V_{BB}) - V_{REG}) \times I_{av} \quad \text{for } V_{BB} < 15 \text{ V}$$

$$P_{CPUMP} = (V_{BB} - V_{REG}) \times I_{av} \quad \text{for } V_{BB} > 15 \text{ V}$$

$$I_{av} = Q_{GATE} \times N \times f_{PWM}$$

$$P_{SWITCHING} = Q_{GATE} \times V_{REG} \times N \times f_{PWM} \times \text{Ratio}$$

$$\text{Ratio} = 10 / (R_{GATE} + 10)$$

where N is the quantity of MOSFETs switching during a PWM cycle. N = 1 for slow decay with diode recirculation, N = 2 for slow decay with synchronous rectification or fast decay with diode recirculation, and N = 4 for fast decay with synchronous rectification.

### Layout Recommendations

Careful consideration must be given to PCB layout when designing high frequency, fast switching, high current circuits. The following are recommendations regarding some of these considerations:

- The A4940 ground, GND, and the high-current return of the external MOSFETs should return separately to the negative side of the motor supply filtering capacitor. This minimizes the effect of switching noise on the device logic and analog reference.
- The exposed thermal pad should be connected to the GND pin and may form part of the Controller Supply ground (see figure 2).
- Minimize stray inductance by using short, wide copper traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.
- Consider the use of small (100 nF) ceramic decoupling capacitors across the sources and drains of the power MOSFETs to limit fast transient voltage spikes caused by the inductance of the circuit trace.
- The ground connection to RDEAD should be connected independently directly to the AGND pin. This sensitive component should never be connected directly to the supply common or to a common ground plane. It must be referenced directly to the AGND pin.
- Supply decoupling for VBB, VREG, and VDD should be connected to the Controller Supply ground which is independently connected close to the GND pin. The decoupling capacitors should also be connected as close as possible to the relevant supply pin.

Note that the above are only recommendations. Each application is different and may encounter different sensitivities. A driver running a few amps will be less susceptible than one running with 150 A and each design should be tested at the maximum current to ensure any parasitic effects are eliminated.

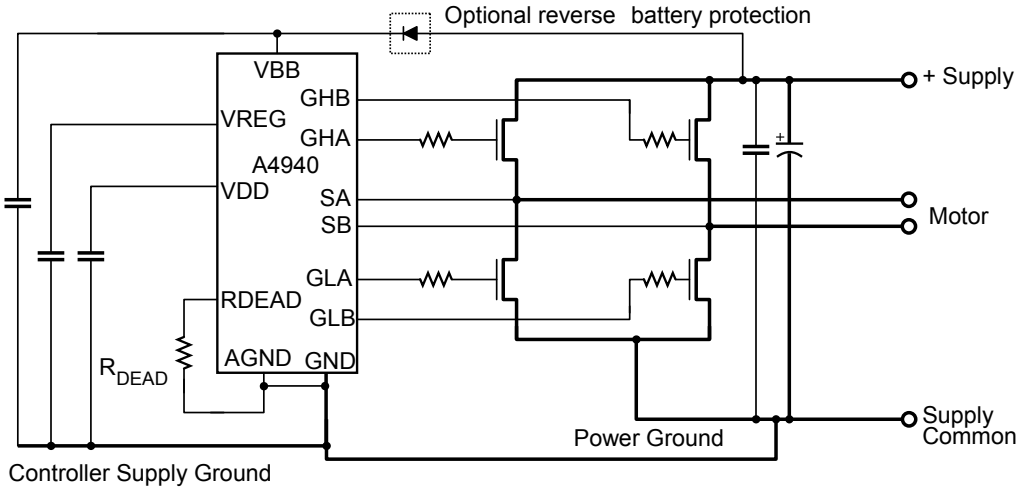


Figure 2. Supply routing suggestions



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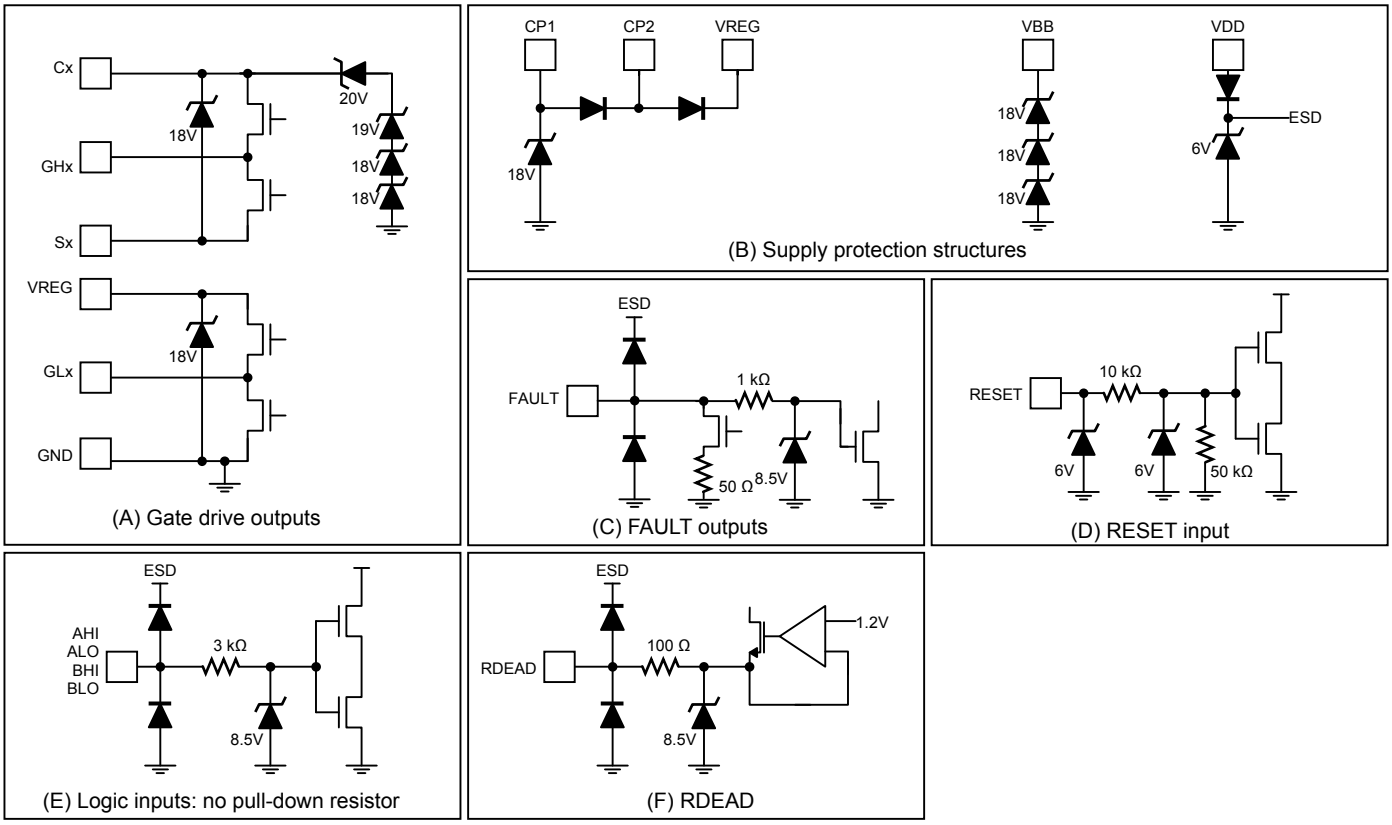
## Input and Output Structures



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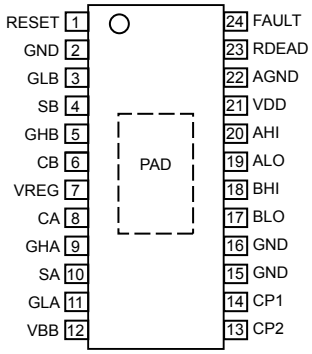
## Pin-out Diagram




### Terminal List

| Number | Name | Function |
|---|---|---|
| AGND | 22 | Ground Reference |
| AHI | 20 | Control Input A High Side |
| ALO | 19 | Control Input A Low Side |
| BHI | 18 | Control Input B High Side |
| BLO | 17 | Control Input B Low Side |
| CA | 8 | Bootstrap Capacitor A |
| CB | 6 | Bootstrap Capacitor B |
| CP1 | 14 | Pump Capacitor |
| CP2 | 13 | Pump Capacitor |
| FAULT | 24 | Fault Output |
| GHA | 9 | High-side Gate Drive A |
| GHB | 5 | High-side Gate Drive B |
| GLA | 11 | Low-side Gate Drive A |
| GLB | 3 | Low-side Gate Drive B |
| GND | 2,15,16 | Ground |
| PAD | – | Exposed pad for thermal dissipation, connect to GND |
| RDEAD | 23 | Dead time setting input |
| RESET | 1 | Reset Input |
| SA | 10 | Load Connection A |
| SB | 4 | Load Connection B |
| VBB | 12 | Main Supply |
| VDD | 21 | Logic Supply |
| VREG | 7 | Regulated 13 V |



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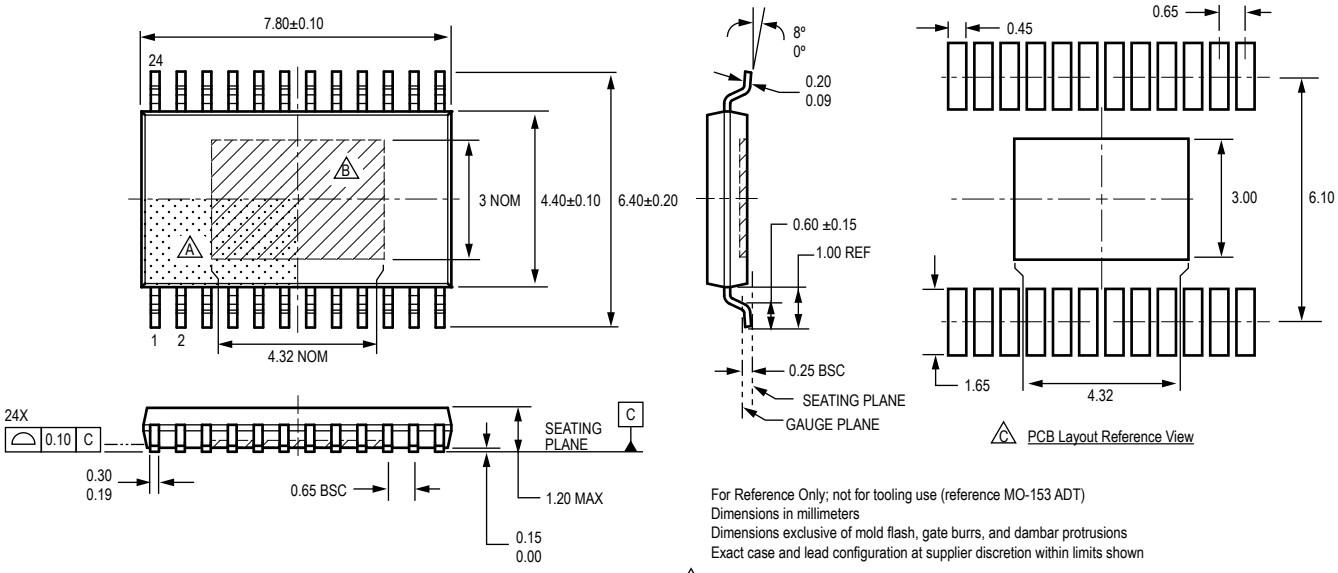
## Package LP 24-Pin TSSOP with Exposed Thermal Pad




For Reference Only; not for tooling use (reference MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)



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## Revision History

| Number | Date | Description |
|---|---|---|
| 2 | February 1, 2019 | Product status changed to Not for New Design |
| 3 | February 13, 2020 | Minor editorial updates |





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