



SY898530U

500MHz 1:16 3.3V-to-2.5/3.3V LVPECL
Fanout Buffer

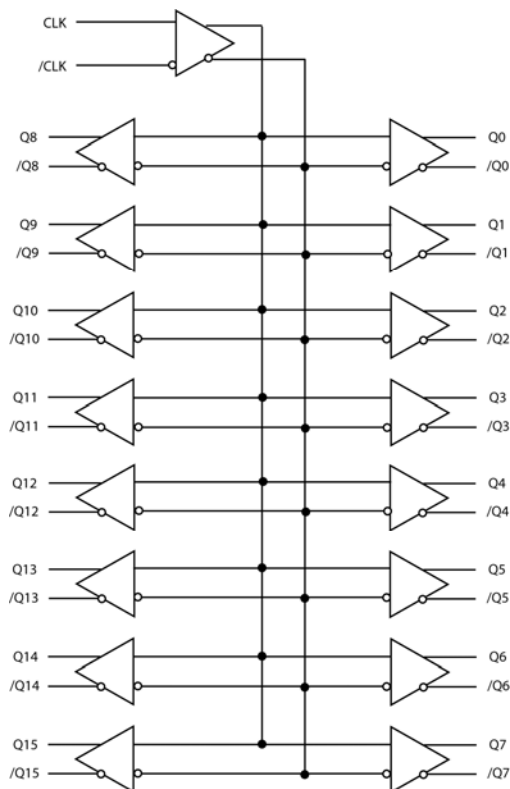
General Description

The SY898530U is a 1:16 Fanout buffer which can accept most standard differential logic levels and outputs the signal as a differential 2.5V or 3.3V LVPECL signal. The part can amplify input signals as small as 150mVpp to the full LVPECL output swing. The SY898530U is well suited for clock distribution applications which demand versatility and low-skew performance. It is pin-to-pin compatible with IDT's ICS8530 fanout buffer.

The SY898530U operates from a 3.3V $\pm 5\%$ core power supply and a 2.5V $\pm 5\%$ or a 3.3V $\pm 5\%$ output supply. The SY898530U is guaranteed over the full commercial temperature range (0°C to +70°C). It is available in a 48-pin TQFP lead-free package.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Functional Block Diagram



Precision Edge is a registered trademark of Micrel, Inc.

Features

- 16 Differential 2.5V/3.3V LVPECL outputs
- Differential CLK inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL logic levels
- Translates any single-ended input signal to 2.5/3.3V LVPECL levels with a resistor bias on /CLK input
- 500MHz maximum output frequency
- <50ps output skew
- <250ps part-to-part skew
- <2ns propagation delay
- 3.3V Core, 2.5/3.3V output operating supply
- 0°C to +70°C operating temperature
- Available in 48-pin TQFP package
- Pin-to-pin compatible with ICS8530

Applications

- Data distribution
- High-performance PCs
- Communications
- Parallel processor-based systems

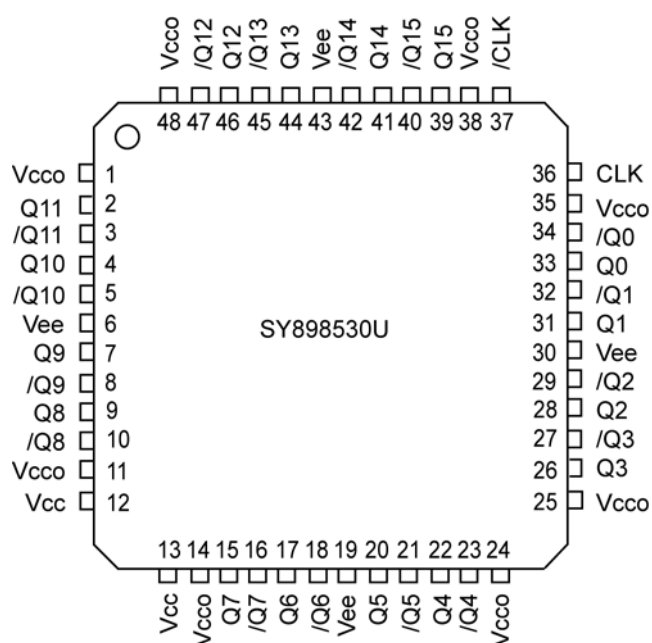
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---------------------------------|--------------|-----------------|---|-------------|
| SY898530UTZ | TQFP-48 | Commercial | SY898530UTZ with Pb-Free bar-line indicator | Matte-Sn |
| SY898530UTZTR ⁽²⁾ | TQFP-48 | Commercial | SY898530UTZ with Pb-Free bar-line indicator | Matte-Sn |
| SY898530UTZTX ^(2, 3) | TQFP-48 | Commercial | SY898530UTZ with Pb-Free bar-line indicator | Matte-Sn |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. EIA specification orientation.

Pin Configuration



48-Pin TQFP (TQFP-48)

Pin Description

| Pin Number | Pin Name | Pin Function |
|---|--|--|
| 36, 37 | CLK, /CLK | Differential Clock Inputs. Accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL logic levels. CLK is internally connected to a pull-down resistor, /CLK is internally connected to a pull-up resistor. See "Pin Characteristics" for typical values. |
| 33, 34 31, 32 28, 29 26, 27 22, 23 20, 21 17, 18 15, 16 9, 10 7, 8 4, 5 2, 3 46, 47 44, 45 41, 42 39, 40 | Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 Q6, /Q6 Q7, /Q7 Q8, /Q8 Q9, /Q9 Q10, /Q10 Q11, /Q11 Q12, /Q12 Q13, /Q13 Q14, /Q14 Q15, /Q15 | LVPECL Differential Output Pairs. Differential buffered copies of the input signal. The output swing is typically 740mV. See Interface Applications for termination information. |
| 1, 11, 14, 24, 25, 35, 38, 48 | VCCO | Output Power Supply: Bypass with 0.1 μ F//0.01 μ F low ESR capacitors as close to the VCCO pins as possible. Supplies the output buffers. |
| 12, 13 | VCC | Core Power Supply: Bypass with 0.1 μ F//0.01 μ F low ESR capacitors as close to the VCC pins as possible. Supplies input and core circuitry. |
| 6, 19, 30, 43 | VEE | Ground |

Pin Characteristics

| Symbol | Description | Min. | Typ. | Max. | Units |
|-----------------------|--------------------------|------|------|------|------------|
| C _{IN} | Input Capacitance | | 4 | | pF |
| R _{PULLUP} | Input Pull Up Resistor | | 50 | | K Ω |
| R _{PULLDOWN} | Input Pull Down Resistor | | 30 | | K Ω |

Clock Input Function Table

| Inputs | | Outputs | | Input to Output Mode | Polarity |
|-----------------------|-----------------------|---------|------|------------------------------|---------------|
| CLK | /CLK | Qx | /Qx | | |
| 0 | 1 | Low | High | Differential to Differential | Non-Inverting |
| 1 | 0 | High | Low | Differential to Differential | Non-Inverting |
| 0 | Biased ⁽¹⁾ | Low | High | Single-Ended to Differential | Non-Inverting |
| 1 | Biased ⁽¹⁾ | High | Low | Single-Ended to Differential | Non-Inverting |
| Biased ⁽¹⁾ | 0 | High | Low | Single-Ended to Differential | Inverting |
| Biased ⁽¹⁾ | 1 | Low | High | Single-Ended to Differential | Inverting |

Note:

1. Refer to Interface Applications for Single-Ended Interfaces.

Absolute Maximum Ratings⁽¹⁾

| | |
|--------------------------------------|--------------------------|
| Supply Voltage (V_{CC}) | 4.6V |
| Input Voltage (V_{IN}) | -0.5V to $V_{CC} + 0.5V$ |
| LVPECL Output Current (I_{OUT}) | |
| Continuous | 50mA |
| Surge | 100mA |
| Lead Temperature (soldering, 20sec.) | 260°C |
| Storage Temperature (T_s) | -65°C to +150°C |

Operating Ratings⁽²⁾

| | |
|---|------------------|
| Supply Voltage (V_{CC}) | 3.135V to 3.465V |
| Output Supply Voltage (V_{CCO}) | 2.375V to 3.465V |
| Ambient Temperature (T_A) | 0°C to +70°C |
| Package Thermal Resistance ⁽³⁾ | |
| TQFP | |
| Still-air (θ_{JA}) | 48°C/W |
| Junction-to-Case (θ_{JC}) | 13°C/W |

DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 3.135V$ to $3.465V$, $V_{CCO} = 2.375V$ to $3.465V$, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-----------|----------------------------|---------------------------|-------------------------------------|------|-----------------|-------|
| V_{CC} | Power Supply Voltage Range | | 3.135 | 3.3 | 3.465 | V |
| V_{CCO} | Output Power Supply | | 2.375 | | 3.465 | V |
| I_{EE} | Power Supply Current | Max. V_{CC} , V_{CCO} | | | 125 | mA |
| I_{IH} | Input HIGH Current | CLK | $V_{CC} = V_{IN} = 3.465V$ | | 150 | uA |
| | | /CLK | | | 5 | uA |
| I_{IL} | Input LOW Current | CLK | $V_{CC} = 3.465V$, $V_{IN} = 0.5V$ | -5 | | uA |
| | | /CLK | | -150 | | uA |
| V_{PP} | Peak-to-Peak Input Swing | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage | Note 4, 5 | 0.5 | | $V_{CC} - 0.85$ | V |

PECL Outputs DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 3.135V$ to $3.465V$, $V_{CCO} = 2.375V$ to $3.465V$, $T_A = 0^\circ C$ to $+70^\circ C$, Outputs terminated with 50Ω to $V_{CCO} - 2V$ unless otherwise stated.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-----------|----------------------|-----------|-----------------|------|-----------------|-------|
| V_{OH} | Output HIGH Voltage | | $V_{CCO} - 1.1$ | | $V_{CCO} - 0.7$ | V |
| V_{OL} | Output LOW Voltage | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.4$ | V |
| V_{OUT} | Output Voltage Swing | | 0.55 | | 0.93 | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. θ_{JA} and θ_{JC} values are determined for a 4-layer board in still-air.
4. For single-ended applications, the maximum input voltage for CLK, /CLK is $V_{CC} + 0.3V$.
5. Common mode voltage is defined as V_{IH} .
6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

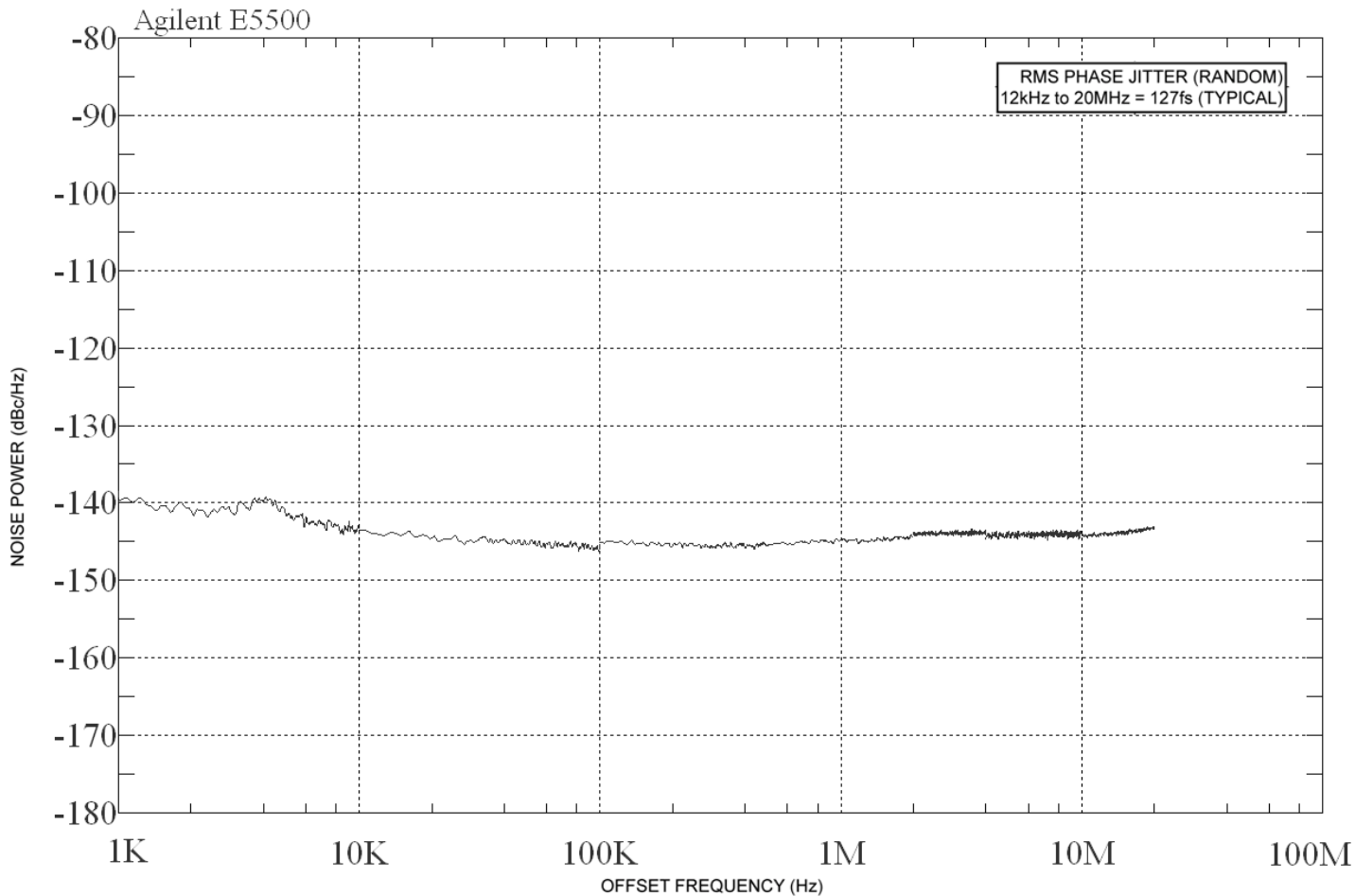
$V_{CC} = 3.135V$ to $3.465V$, $V_{CCO} = 2.375V$ to $3.465V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--------------|--|-----------------------|------|------|------|-------------------|
| f_{MAX} | Maximum Frequency | | 500 | | | MHz |
| t_{PD} | Propagation Delay | Note 7 | 1 | | 2 | ns |
| t_{Skew} | Output-to-Output skew | Note 8, 10 | | 26 | 50 | ps |
| | Part-to-Part Skew | Notes 9, 10 | | | 250 | ps |
| t_{JITTER} | Integration Range = 12kHz – 20MHz | Output = 500MHz | | 127 | | fs _{RMS} |
| t_R, t_F | Output Rise/Fall Times (20% to 80%) | At full output swing. | 300 | | 700 | ps |
| | Duty Cycle | | 47 | 50 | 53 | % |

Notes:

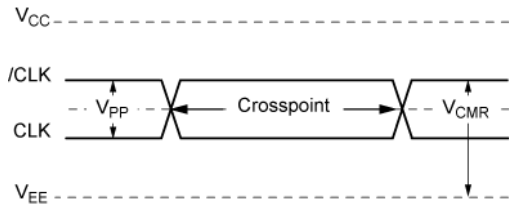
7. Measured from the differential input crossing point to the differential output crossing point.
8. Output-to-Output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage and transition.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. This parameter is defined in accordance with JEDEC Standard 65.

Phase Noise Graph

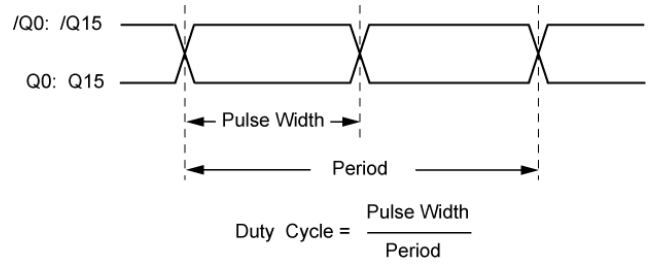


Phase Noise Plot: 500MHz @ 3.3V

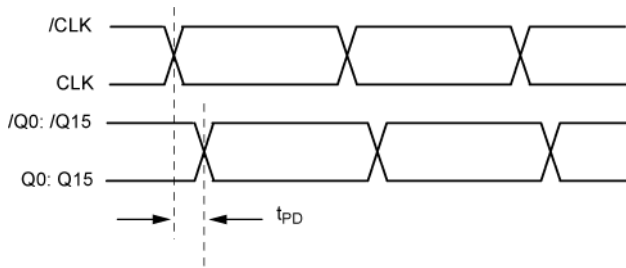
Test Circuit



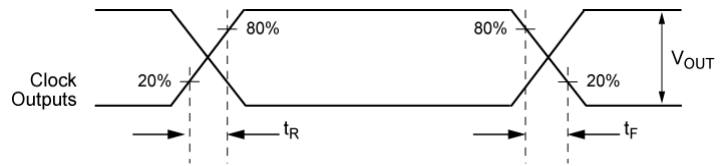
Differential Input Level



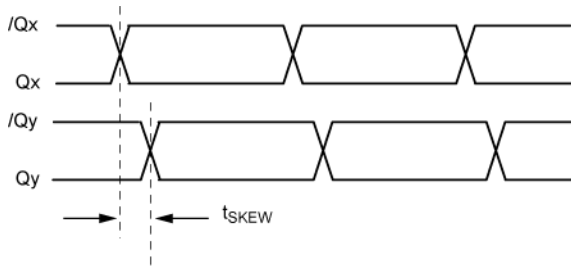
Output Duty Cycle



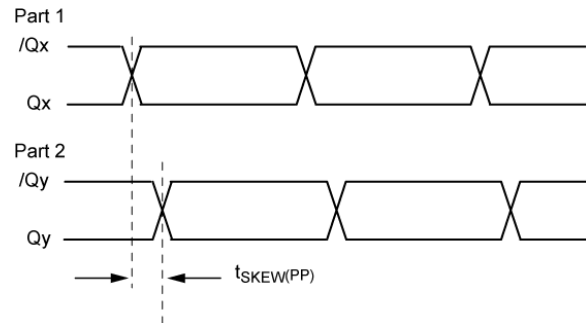
Propagation Delay



Output Rise/Fall Times



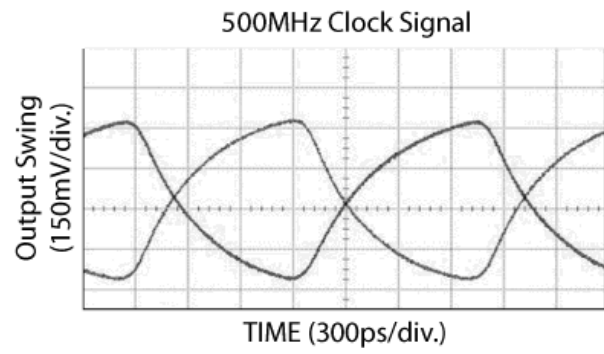
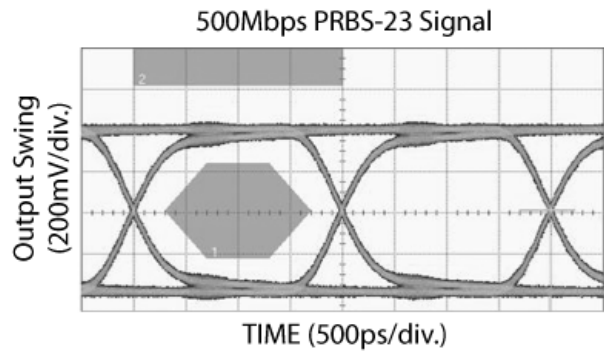
Output-to-Output Skew



Part-to-Part Skew

Typical Characteristics

$V_{CC} = 3.3V$, $V_{CCO} = 2.5V$ or $3.3V$, $T_A = 25^\circ C$, Input Signal = $800mV$



Junction Temperature

The maximum recommended junction temperature is $T_J = 125^\circ\text{C}$. The outputs are terminated with 50 ohms to $V_{CC0} - 2V$. Below is a calculation of the worst case scenario with zero airflow:

T_J = Junction Temperature

T_A = Ambient Temperature

Θ_{JA} = Junction-to-Ambient Thermal Resistance

P_d = Power Dissipation

$$P_d = P_{d_core} + P_{d_outputs}$$

$$P_{d_core} = V_{CC_max} * I_{EE_max}$$

$$P_{d_core} = 3.465V * 125mA = 433mW$$

$$P_{d_output} = P_{d_h} + P_{d_l}$$

$$P_{d_h} = [(V_{oh} - (V_{CC0} - 2V))/R_L] * (V_{CC0} - V_{oh_max})$$

$$P_{d_h} = [(2V - 0.7V)/50\Omega] * 0.7V$$

$$P_{d_h} = 18.2mW$$

$$P_{d_l} = [(V_{ol} - (V_{CC0} - 2V))/R_L] * (V_{CC0} - V_{ol_max})$$

$$P_{d_l} = [(2V - 1.4V)/50\Omega] * 1.4V$$

$$P_{d_l} = 16.8mW$$

$$P_{d_output} = 35mW$$

$$P_{d_outputs} = 16 * 35mW$$

$$P_{d_outputs} = 560mW$$

$$P_d = 433mW + 560mW$$

$$P_d = 0.993 W$$

$$T_J = T_A + \Theta_{JA} * P_d$$

$$T_{J_worst_case} = 70^\circ\text{C} + 0.993W * 48^\circ\text{C/W}$$

$$T_{J_worst_case} = 118^\circ\text{C in still air.}$$

The worst case junction temperature is below 125 C.

Output Interface Applications

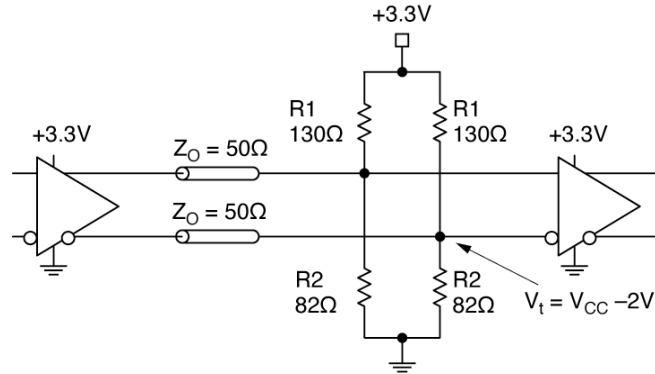


Figure 1. Parallel Termination-Thevenin Equivalent

Notes:

1. For +2.5V systems: R1 = 250Ω, R2 = 82.5Ω.

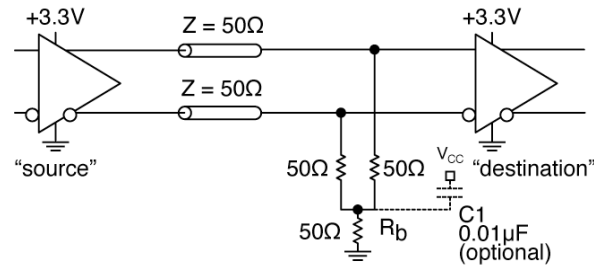


Figure 2. Three-Resistor "Y-Termination"

Notes:

1. Power-saving alternatives to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. For +2.5V systems, R_b = 19Ω. R_b resistor sets the DC bias voltage, equal to V_t.

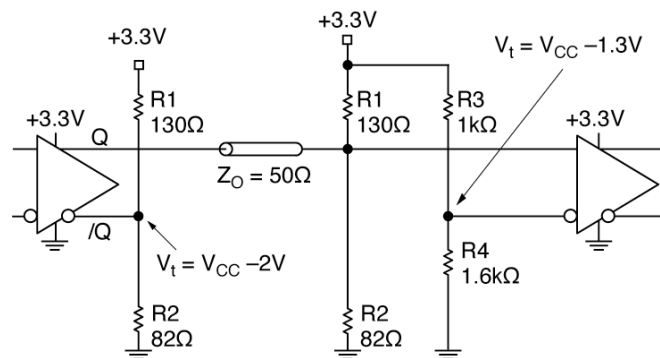


Figure 3. Terminating Unused I/O

Notes:

1. Unused output (/Q) must be terminated to balance the output.
2. For 2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.

Input Interface Applications

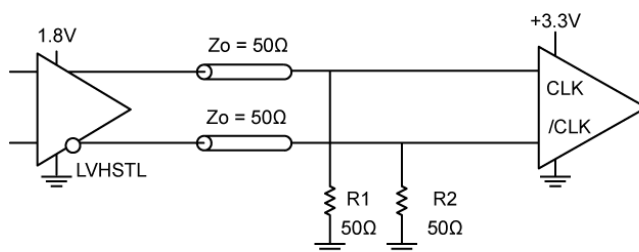


Figure 4. CLK and /CLK Input Driven By 1.8V LVHSTL

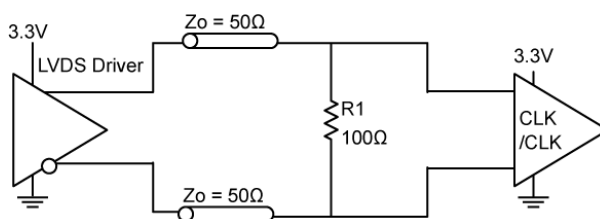


Figure 5. CLK and /CLK Input Driven By 3.3V LVDS Driver

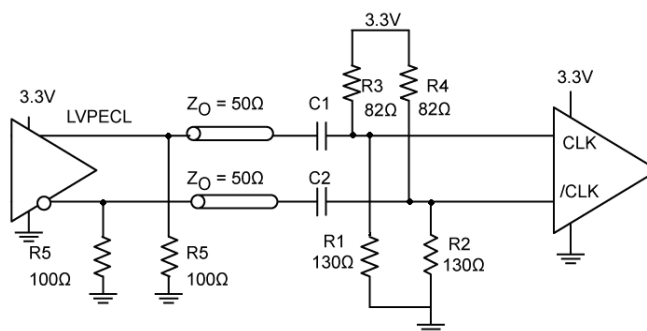
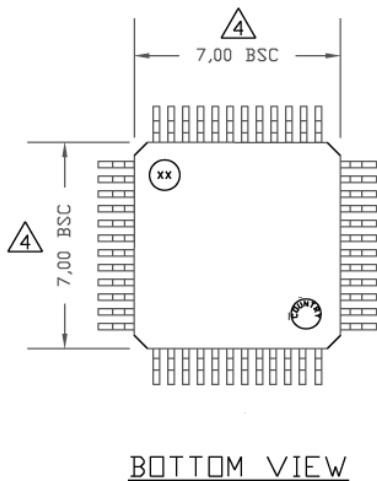
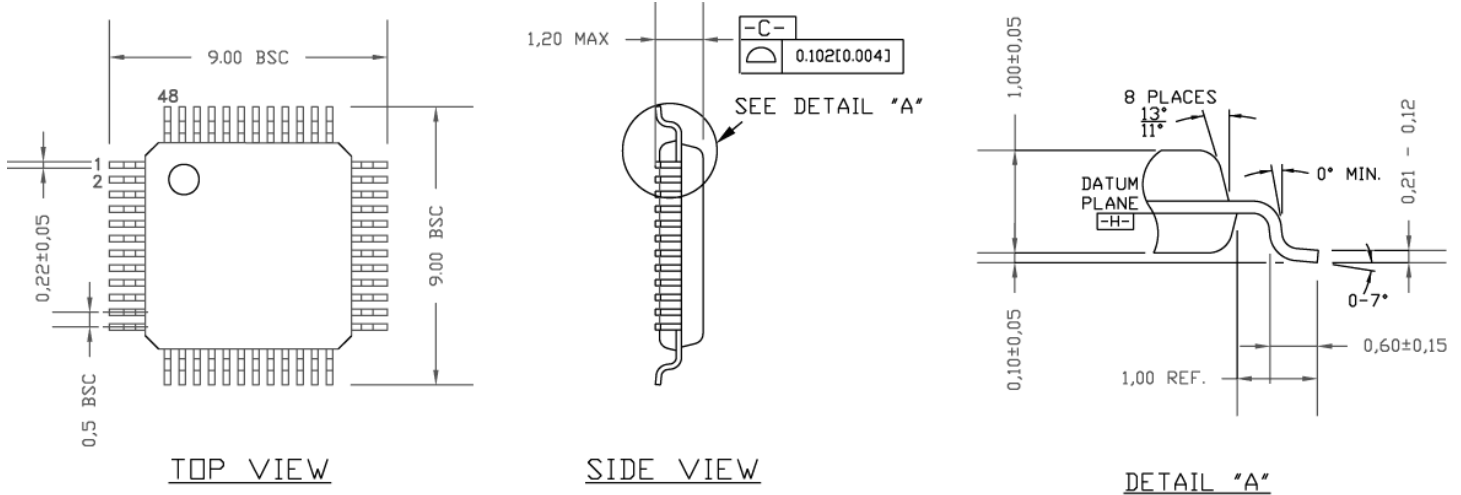


Figure 6. CLK and /CLK Input Driven By 3.3V LVPECL Driver with AC Couple

Notes:

1. For +2.5V systems: R5 = 50 Ω. R1 & R2 = 220Ω, R3 & R4 = 68Ω.

Package Information



NOTES:

1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254MM.
2. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
3. PACKAGE TOP MOLD DIMENSIONS ARE SMALLER THAN BOTTOM
4. MOLD DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

48-Pin TQFP (TQFP-48)

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