NCV8508B

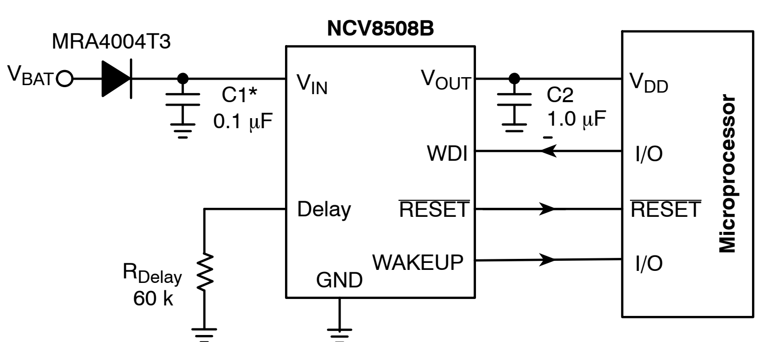
LDO Regulator - Watchdog, RESET

5.0 V, 3.3 V, 250 mA

The NCV8508B is a precision micropower Low Dropout (LDO) voltage regulator. The part contains many of the required features for powering microprocessors. Its robustness makes it suitable for severe automotive environments. In addition, the NCV8508B is ideal for use in battery operated, microprocessor controlled equipment because of its extremely low quiescent current.

Features

- Output Voltage: 5.0 V and 3.3 V
- ±3.0% Output Voltage
- I_{OUT} Up to 250 mA
- Quiescent Current Independent of Load
- Micropower Compatible Control Functions:
  - Wakeup
  - Watchdog
  - RESET
- Low Quiescent Current (100 μA typ)
- Protection Features:
  - Thermal Shutdown
  - Short Circuit
  - 45 V Operation
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- AEC Qualified
- PPAP Capable
- These are Pb−Free Devices



*C1 required if regulator is located far from power supply filter.

Figure 1. Application Circuit

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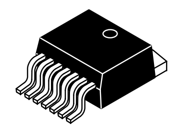
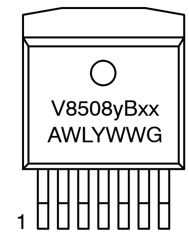
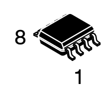
MARKING DIAGRAMS

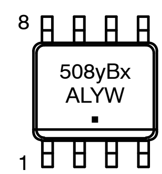


D²PAK−7
DS SUFFIX
CASE 936AB





SO−8 EP
PD SUFFIX
CASE 751AC



xx, x	=	Voltage Option 5.0 V (xx = 50, x = 5) 3.3 V (xx = 33, x = 3)
y	=	Timing Option (see Page 4 for more details) 1 (Delay Time = 3 ms @ R_{Delay} = 60k) 2 (Delay Time = 9 ms @ R_{Delay} = 60k)
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

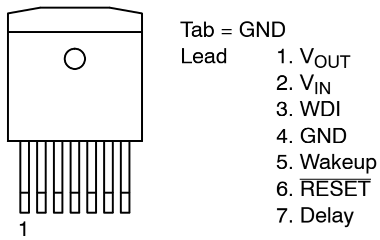
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

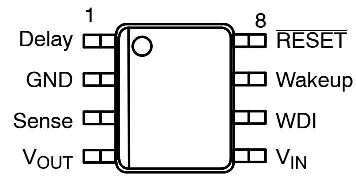
September, 2019 − Rev. 3

Publication Order Number:
NCV8508B/D

PIN CONNECTIONS



D^2PAK−7



SO−8 EP

PACKAGE PIN DESCRIPTION

PACKAGE PIN #		PIN SYMBOL	FUNCTION
D^2PAK−7	SO−8 EP		
1	4	V_{OUT}	Regulated output voltage ± 3.0%.
2	5	V_{IN}	Supply Voltage to the IC.
3	6	WDI	CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming signal.
4	2	GND	Ground connection.
5	7	Wakeup	CMOS compatible output consisting of a continuously generated signal used to “wake up” the microprocessor from sleep mode.
6	8	$\overline{RESET}$	CMOS compatible output lead $\overline{RESET}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct Watchdog signal.
7	1	Delay	Buffered bandgap voltage used to create timing current for $\overline{RESET}$ and Wakeup from $R_{Delay.}$
–	–	NC	No Connection.
–	3	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to V_{OUT} if remote sensing is not required.
–	EPAD	EPAD	Connect to Ground potential or leave unconnected.

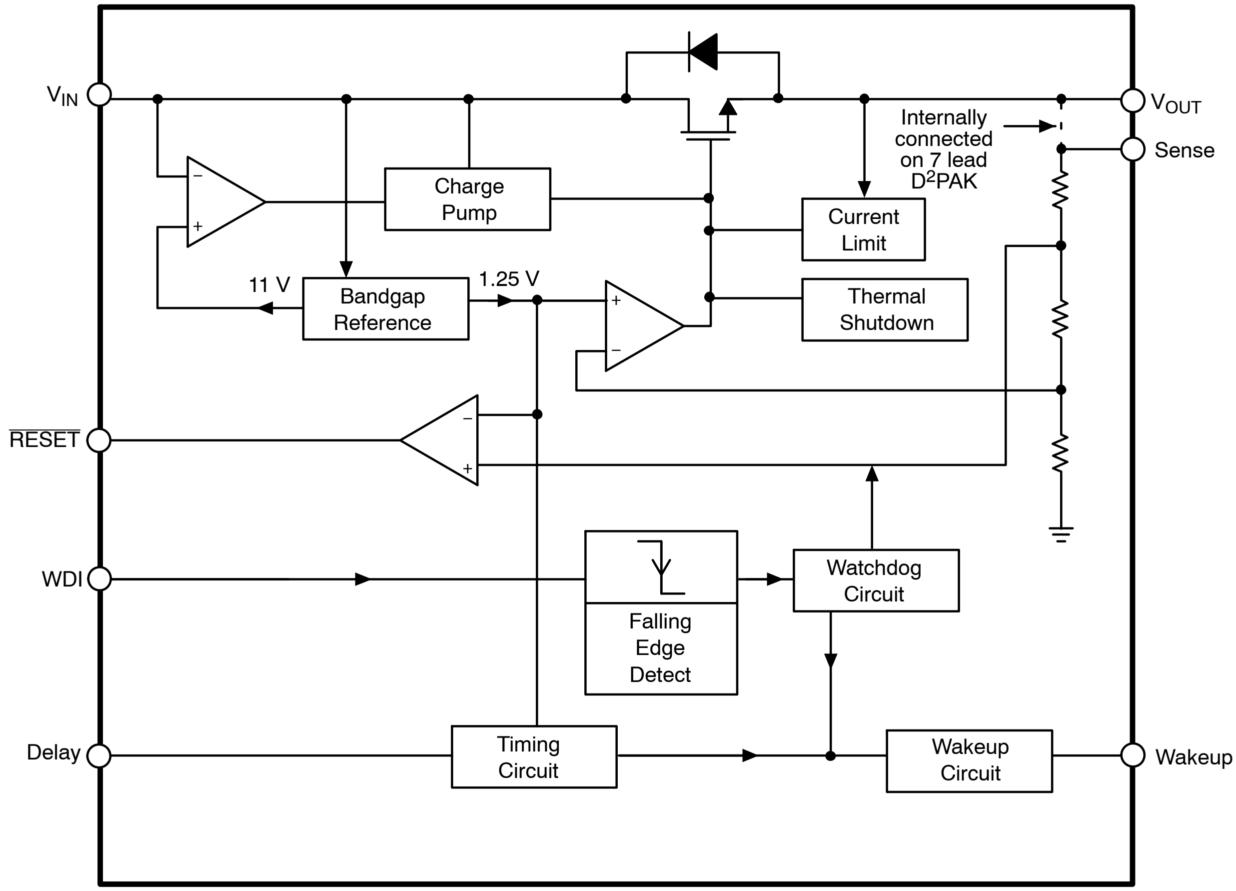


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Input Voltage, V_{IN} (DC)		−0.3 to 45	V
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)		60	V
Output Voltage, V_{OUT}		−0.3 to 18	V
ESD Susceptibility:	Human Body Model Machine Model Charged Device Model	2.0 200 1.0	kV V kV
Logic Inputs/Outputs ($\overline{RESET}$, WDI, Wakeup)		−0.3 to +7.0	V
Operating Junction Temperature, T_J		−40 to150	°C
Storage Temperature Range, T_S		−55 to +150	°C
Peak Reflow Soldering Temperature:	Reflow: (Note 1)	260 Peak (Note 2)	°C
Moisture Sensitivity Level:	D2PAK−7 SO−8EP	3 2	–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. 60 second maximum above 183°C.
2. −5°C/+0°C allowable conditions.

THERMAL CHARACTERISTICS

See Package Thermal Data Section (Page 11)

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic		Test Conditions	Min	Typ	Max	Unit
OUTPUT						
Output Voltage	5.0 V	–	4.85	5.00	5.15	V
Output Voltage	3.3 V	–	3.201	3.3	3.399	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	5.0 V	I_{OUT} = 150 mA. Note 3	–	450	900	mV
Load Regulation		V_{IN} = 14 V, 100 μA ≤ I_{OUT} ≤ 150 mA	–	5.0	30	mV
Line Regulation		6.0 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 5.0 mA	–	5.0	50	mV
Current Limit		–	250	400	–	mA
Thermal Shutdown		Guaranteed by Design	150	180	210	°C
Quiescent Current		V_{IN} = 12 V, I_{OUT} = 150 mA, (see Figure 6)	–	100	150	μA
$\overline{\text{RESET}}$						
Threshold	5.0 V	–	4.50	4.65	4.80	V
Threshold	3.3 V	–	2.970	3.069	3.168	V
Output Low		R_{LOAD} = 10 k to V_{OUT}, V_{OUT} ≥ 1.0 V R_{LOAD} = 5.1 k to V_{OUT}, V_{OUT} ≥ 1.0 V	–	0.2 0.4	0.4 0.8	V
Output High		R_{LOAD} = 10 k to GND R_{LOAD} = 5.1 k to GND	V_{OUT} – 0.5 V_{OUT} – 1.0	V_{OUT} – 0.25 V_{OUT} – 0.5	–	V
Delay Time	NCV85081B	V_{IN} = 14 V, R_{Delay} = 60 k, I_{OUT} = 5.0 mA V_{IN} = 14 V, R_{Delay} = 120 k, I_{OUT} = 5.0 mA	2.0 –	3.0 6.0	4.0 –	ms ms
Delay Time	NCV85082B	V_{IN} = 14 V, R_{Delay} = 60 k, I_{OUT} = 5.0 mA V_{IN} = 14 V, R_{Delay} = 120 k, I_{OUT} = 5.0 mA	6.0 –	9.0 18	12.0 –	ms ms
WATCHDOG INPUT						
Threshold High		–	70	–	–	%V_{OUT}
Threshold Low		–	–	–	30	%V_{OUT}
Hysteresis		–	–	100	–	mV
Input Current		WDI = 6.0 V	–	0.1	+10	μA
Pulse Width		50% WDI falling edge to 50% WDI rising edge and 50% WDI rising edge to 50% WDI falling edge, (see Figure 5)	5.0	–	–	μs
WAKEUP OUTPUT (V_{IN} = 14 V, I_{OUT} = 5.0 mA)						
Wakeup Period	NCV85081B	See Figures 4 and 5, R_{DELAY} = 60 k See Figures 4 and 5, R_{DELAY} = 120 k	18 –	25 50	32 –	ms ms
Wakeup Period	NCV85082B	R_{DELAY} = 60 k R_{DELAY} = 120 k	54 –	75 150	96 –	ms ms
Wakeup Duty Cycle Nominal		See Figure 3	45	50	55	%
$\overline{\text{RESET}}$ HIGH to Wakeup Rising Delay Time	NCV85081B	R_{DELAY} = 60 k, 50% $\overline{\text{RESET}}$ rising edge to 50% Wakeup edge R_{DELAY} = 120 k (see Figures 3 and 4)	9.0 –	12.5 25	16 –	ms ms

3. Measured when the output voltage has dropped 100 mV from the nominal value. (see Figure 12)
4. Current drain on the Delay pin directly affects the Delay Time, Wakeup Period, and the $\overline{\text{RESET}}$ to Wakeup Delay Time.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
WAKEUP OUTPUT (V_{IN} = 14 V, I_{OUT} = 5.0 mA)					
$\overline{\text{RESET}}$ HIGH to Wakeup Rising Delay Time NCV85082B	R_{DELAY} = 60 k, 50% $\overline{\text{RESET}}$ rising edge to 50% Wakeup edge R_{DELAY} = 120 k	27 –	37.5 75	48 –	ms ms
Wakeup Response to Watchdog Input	50% WDI falling edge to 50% Wakeup falling edge	–	0.1	5.0	μs
Wakeup Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ falling edge to 50% Wakeup falling edge $V_{OUT} = V_{OUT\_NOM}$ –> 90% of V_{OUT_NOM}	–	0.1	5.0	μs
Output Low	R_{LOAD} = 10 k to V_{OUT}, $V_{OUT} \ge 1.0$ V R_{LOAD} = 5.1 k to V_{OUT}, $V_{OUT} \ge 1.0$ V	–	0.2 0.4	0.4 0.8	V
Output High	R_{LOAD} = 10 k to GND R_{LOAD} = 5.1 k to GND	V_{OUT} – 0.5 V_{OUT} – 1.0	V_{OUT} – 0.25 V_{OUT} – 0.5	–	V
DELAY					
Output Voltage	I_{DELAY} = 50 μA. Note 4	–	1.25	–	V

3. Measured when the output voltage has dropped 100 mV from the nominal value. (see Figure 12)
4. Current drain on the Delay pin directly affects the Delay Time, Wakeup Period, and the $\overline{\text{RESET}}$ to Wakeup Delay Time.

TIMING DIAGRAMS

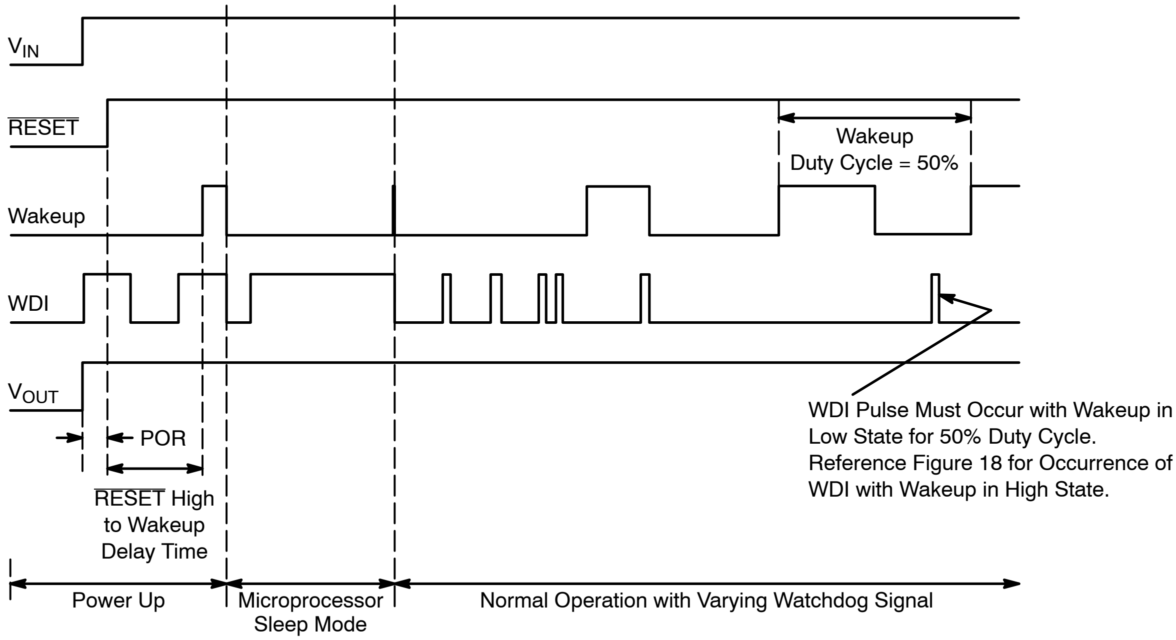


Figure 3. Power Up, Sleep Mode and Normal Operation

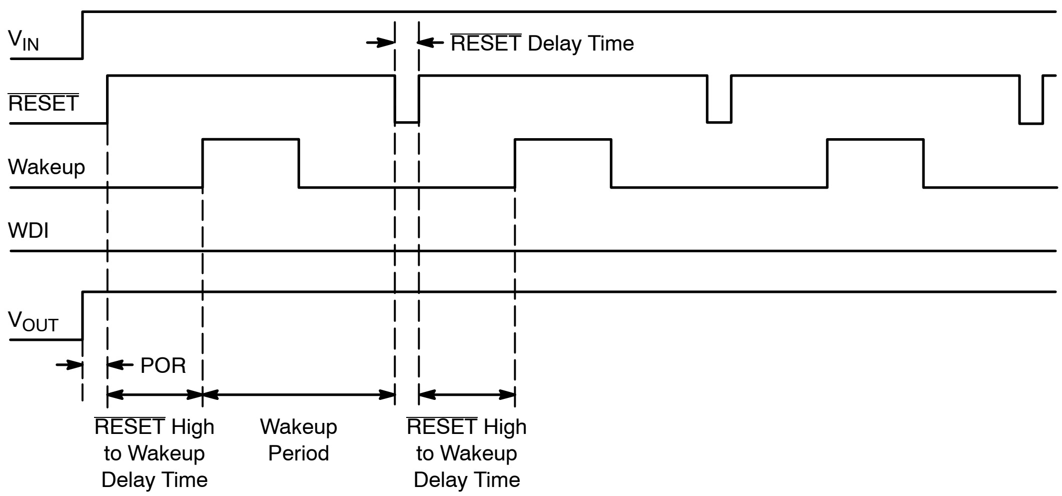


Figure 4. Error Condition: Watchdog Remains Low and a RESET Is Issued

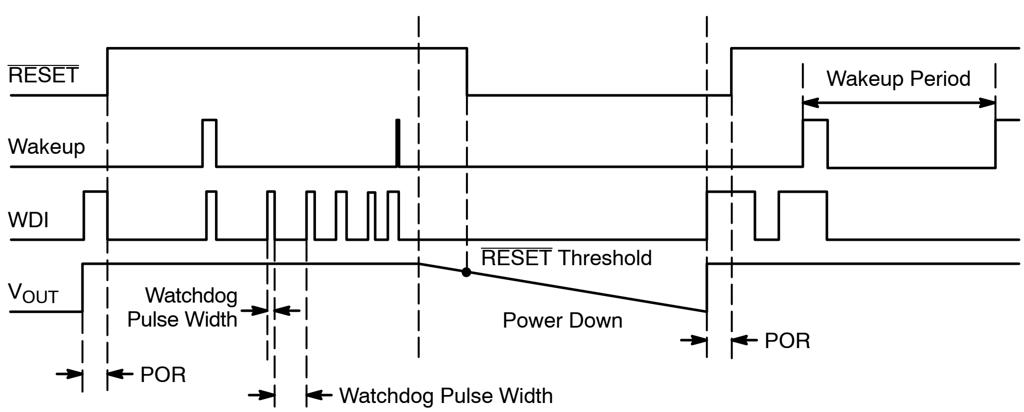


Figure 5. Power Down and Restart Sequence

TYPICAL PERFORMANCE CHARACTERISTICS

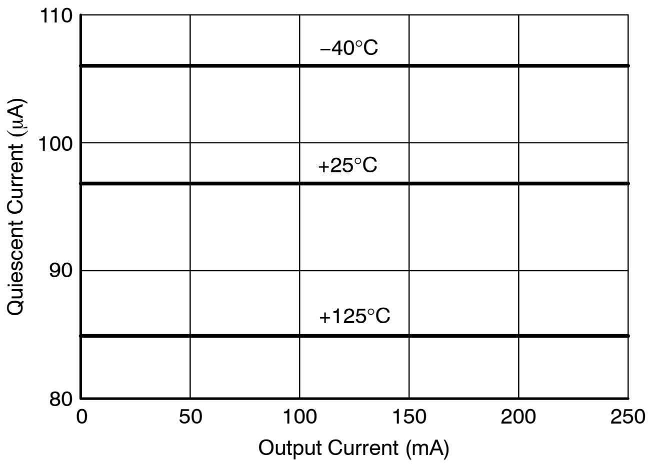


Figure 6. Quiescent Current vs Output Current

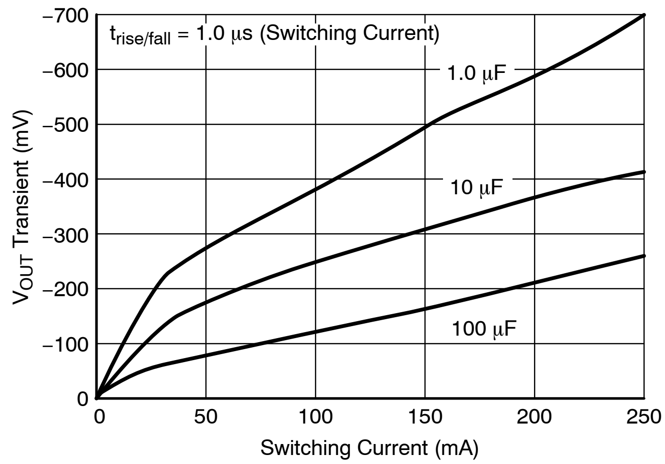


Figure 7. Load Transient Response

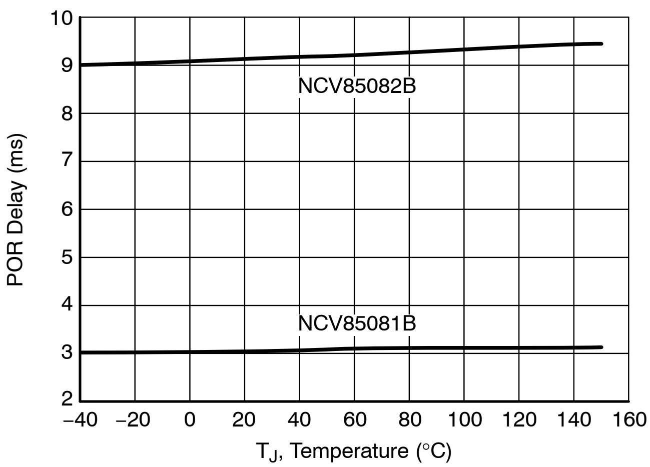


Figure 8. Reset Delay Time vs Junction Temperature

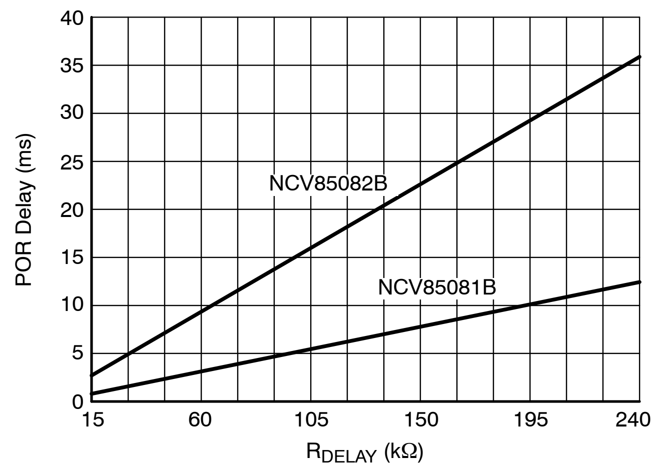


Figure 9. Reset Delay Time vs Reset Delay Resistor

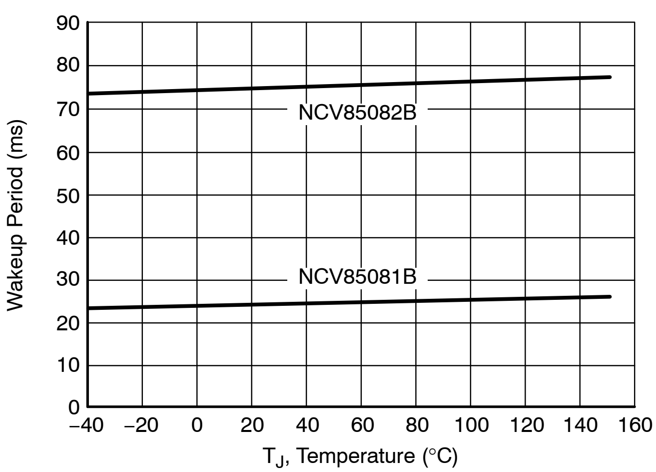


Figure 10. Wakeup Period vs Junction Temperature

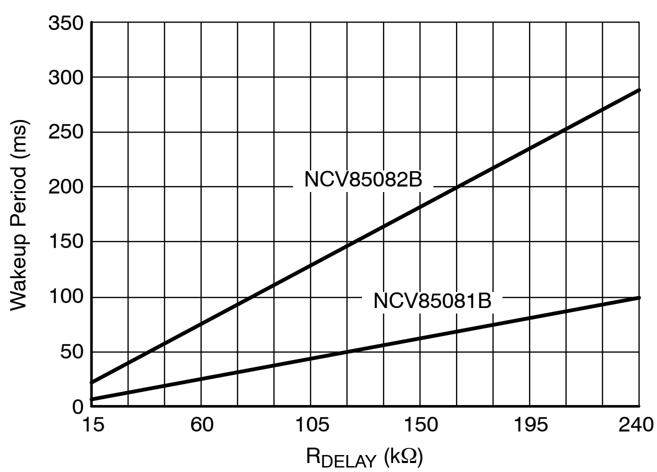


Figure 11. Wakeup Period vs Reset Delay Resistor

TYPICAL PERFORMANCE CHARACTERISTICS

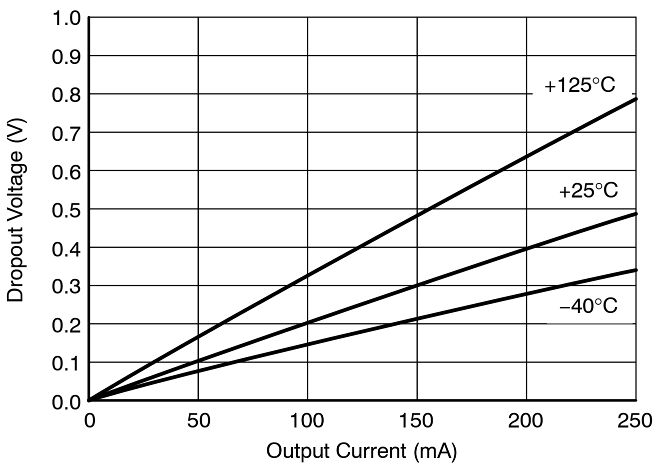


Figure 12. Dropout Voltage vs Output Current

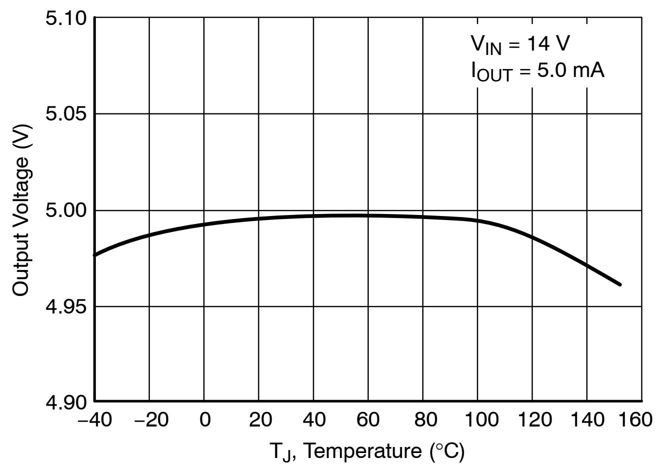


Figure 13. Output Voltage vs Junction Temperature, 5 V

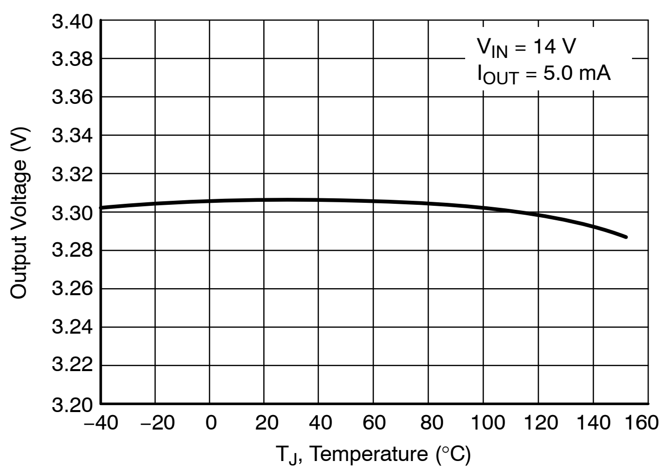


Figure 14. Output Voltage vs Junction Temperature, 3.3 V

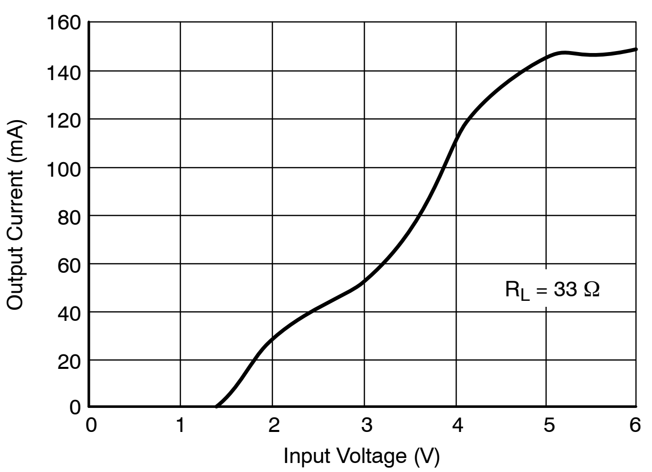


Figure 15. Output Current vs Input Voltage

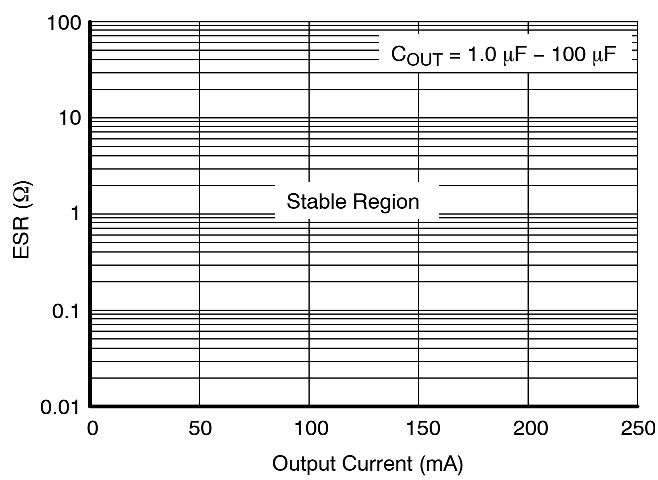


Figure 16. Output Capacitor ESR

DEFINITION OF TERMS

Dropout Voltage: The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

DETAILED OPERATING DESCRIPTION

The NCV8508B is a precision micropower voltage regulator with very low quiescent current (100 μA typical at 250 mA load). A typical dropout voltage is 450 mV at 150 mA for 5 V option. Microprocessor control logic includes Watchdog, Wakeup and $\overline{\text{RESET}}$. This unique combination of extremely low quiescent current and full microprocessor control makes the NCV8508B ideal for use in battery operated, microprocessor controlled equipment in addition to being a good fit in the automotive environment.

The NCV8508B Wakeup function brings the microprocessor out of Sleep mode. The microprocessor in turn signals its Wakeup status back to the NCV8508B by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The NCV8508B responds to the falling edge of the Watchdog signal which it expects at least once during each Wakeup period. When the correct Watchdog signal is received, a falling edge is issued on the Wakeup signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1.0 V. A signal is issued in any of three situations. During power up, the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. Finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a Watchdog signal within the Wakeup period.

The $\overline{\text{RESET}}$ pulse width, Wakeup signal frequency, and Wakeup delay time are all set by one external resistor, R_{Delay}.

The Delay pin is a buffered bandgap voltage (1.25 V). It can be used as a reference for an external tracking regulator as shown in Figure 17.

The regulator is protected against short circuit and thermal runaway conditions. The device runs through 45 volt transients, making it suitable for use in automotive environments.

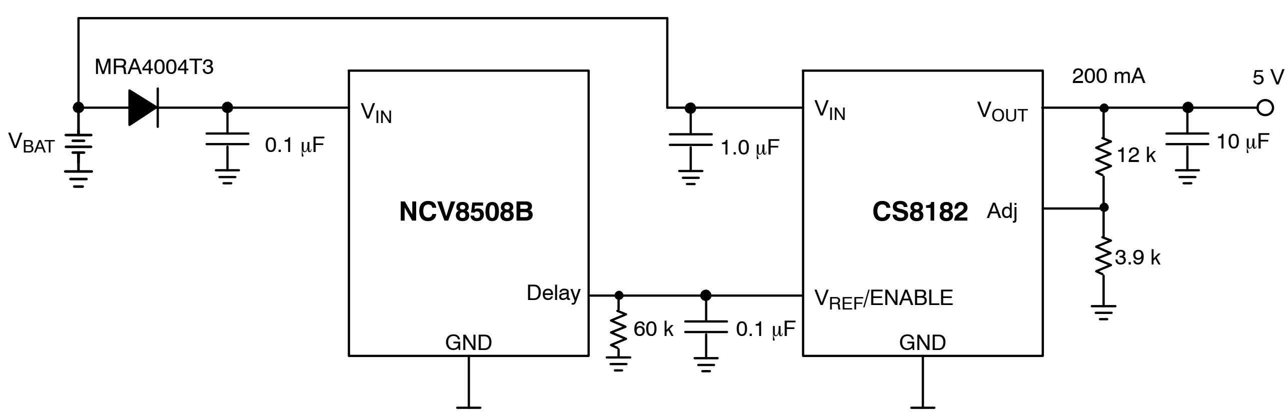


Figure 17. Application Circuit

CIRCUIT DESCRIPTION

Functional Description

To reduce the drain on the battery, a system can go into a low current consumption mode whenever it is not performing a main routine. The Wakeup signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 (or 3.3 V) volt square wave (voltage generated from V_{OUT}) with a duty cycle of 50% at a frequency that is determined by a timing resistor, R_{Delay}.

When the microprocessor receives a rising edge from the Wakeup output, it must issue a Watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the Watchdog signal causes the Wakeup to go low within 2.0 μs (typ) and remain low until the next Wakeup cycle (see Figure 18). Other Watchdog pulses received within the same cycle are ignored (Figure 3).

During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text{RESET}}$ delay, $\overline{\text{RESET}}$ returns high.

The Watchdog circuitry continuously monitors the input Watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wakeup cycle will cause a $\overline{\text{RESET}}$ pulse to occur at the end of the Wakeup cycle. (see Figure 4).

The Wakeup output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wakeup cycle begins again (see Figure 4).

The $\overline{\text{RESET}}$ Delay Time, Wakeup signal frequency and $\overline{\text{RESET}}$ high to Wakeup delay time are all set by one external resistor R_{Delay}.

Wakeup Period = $(4.17 \times 10^{-7})R_{Delay}$

$\overline{\text{RESET}}$ Delay Time = $(5.21 \times 10^{-8})R_{Delay}$

$\overline{\text{RESET}}$ HIGH to Wakeup Delay Time = $(2.08 \times 10^{-7})R_{Delay}$

Resistor temperature coefficient and tolerance as well as the tolerance of the NCV8508B must be taken into account in order to get the correct system tolerance for each parameter.

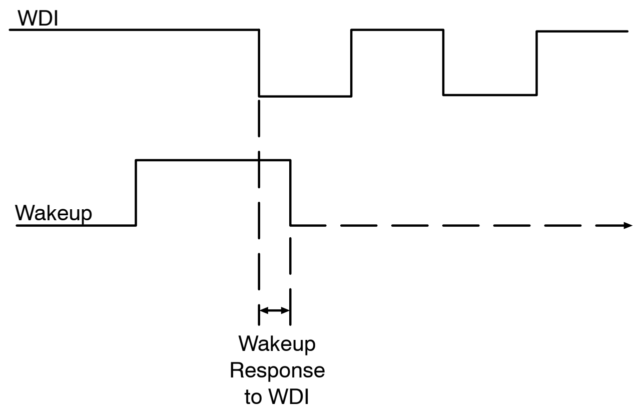


Figure 18. Wakeup Response to WDI

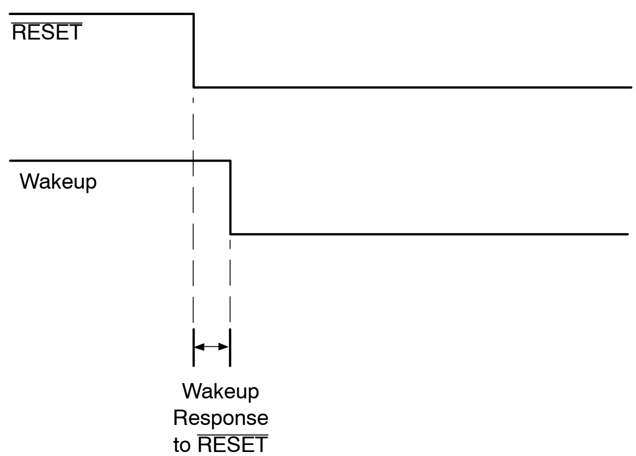


Figure 19. Wakeup Response to $\overline{\text{RESET}}$ (Low Voltage)

Recommend Thermal Data for D^2PAK−7 Package

Parameter	Test Conditions Typical Value		Units
	min−pad board (Note 5)	**1"−pad board** (Note 6)	
Junction−to−Lead (psi−JL, Ψ_{JL})	12	12	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	84	48	°C/W

5. 1 oz. copper, 118 mm^2 copper area, 0.062" thick FR4.
6. 1 oz. copper, 626 mm^2 copper area, 0.062" thick FR4.

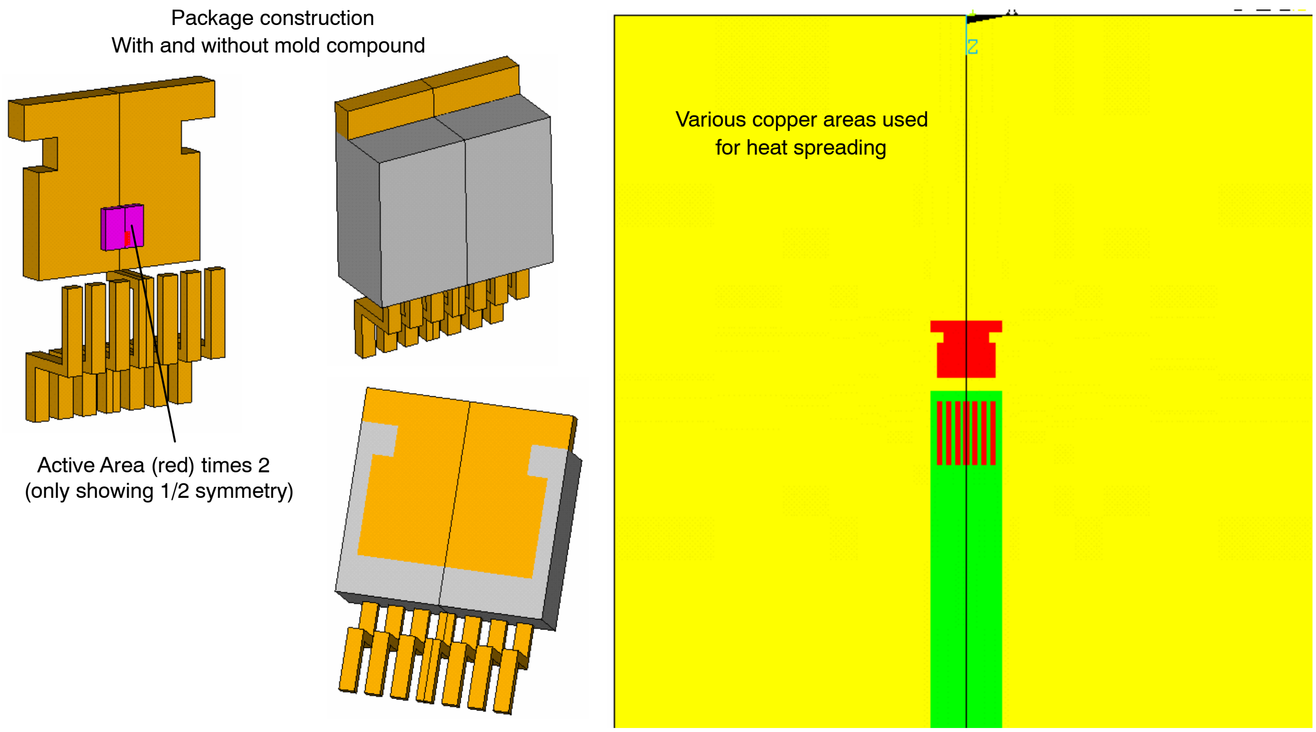


Figure 20. PCB Layout and Package Construction for Simulation

Table 1. D^2PAK 7−Lead Thermal RC Network Models

	118 mm^2	626 mm^2		118 mm^2	626 mm^2	Cu Area
	Cauer Network			Foster Network		
	C’s	C’s	Units	Tau	Tau	units
1	8.6E−07	8.6E−07	W−s/C	1.00E−07	1.00E−07	sec
2	3.6E−06	3.6E−06	W−s/C	1.00E−06	1.00E−06	sec
3	1.4E−05	1.4E−05	W−s/C	1.00E−05	1.00E−05	sec
4	1.4E−04	1.4E−04	W−s/C	3.07E−04	3.07E−04	sec
5	6.4E−04	6.4E−04	W−s/C	1.00E−03	1.00E−03	sec
6	1.1E−02	1.1E−02	W−s/C	6.00E−03	6.00E−03	sec
7	3.0E−02	3.0E−02	W−s/C	2.00E−02	2.00E−02	sec
8	4.9E−01	5.2E−01	W−s/C	1.43E+00	1.43E+00	sec
9	4.8E−01	1.5E+00	W−s/C	6.15E+00	3.82E+00	sec
10	6.9E−01	9.5E−01	W−s/C	1.04E+02	9.68E+01	sec
	R’s	R’s		R’s	R’s	
1	0.147	0.147	C/W	0.090	0.090	C/W
2	0.301	0.301	C/W	0.194	0.194	C/W
3	0.603	0.603	C/W	0.614	0.614	C/W
4	2.733	2.733	C/W	1.200	1.200	C/W
5	1.178	1.178	C/W	2.600	2.600	C/W
6	1.369	1.366	C/W	0.100	0.100	C/W
7	0.272	0.270	C/W	1.700	1.700	C/W
8	14.820	7.855	C/W	0.100	0.100	C/W
9	6.055	2.741	C/W	6.944	5.181	C/W
10	56.834	30.488	C/W	70.770	35.902	C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 166 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

θJA vs Copper Spreader Area

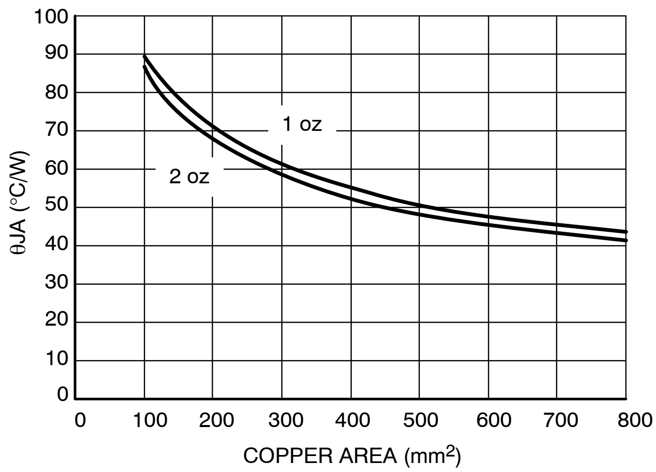


Figure 21. D²PAK 7−lead θJA as a Function of the Pad Copper Area Including Traces, Board Material

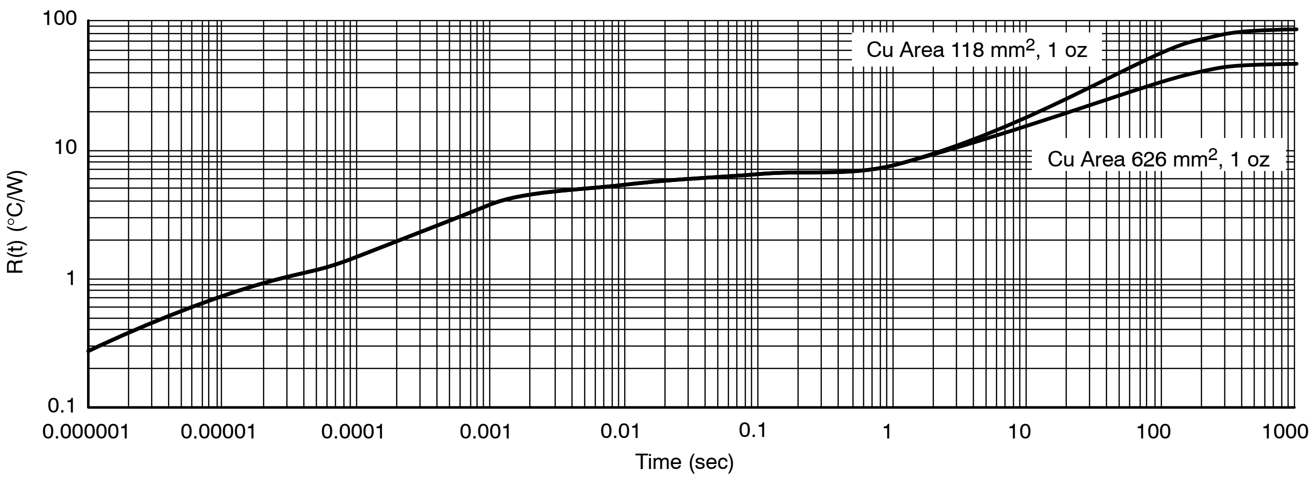


Figure 22. D²PAK 7−Lead Single Pulse Heating Curve

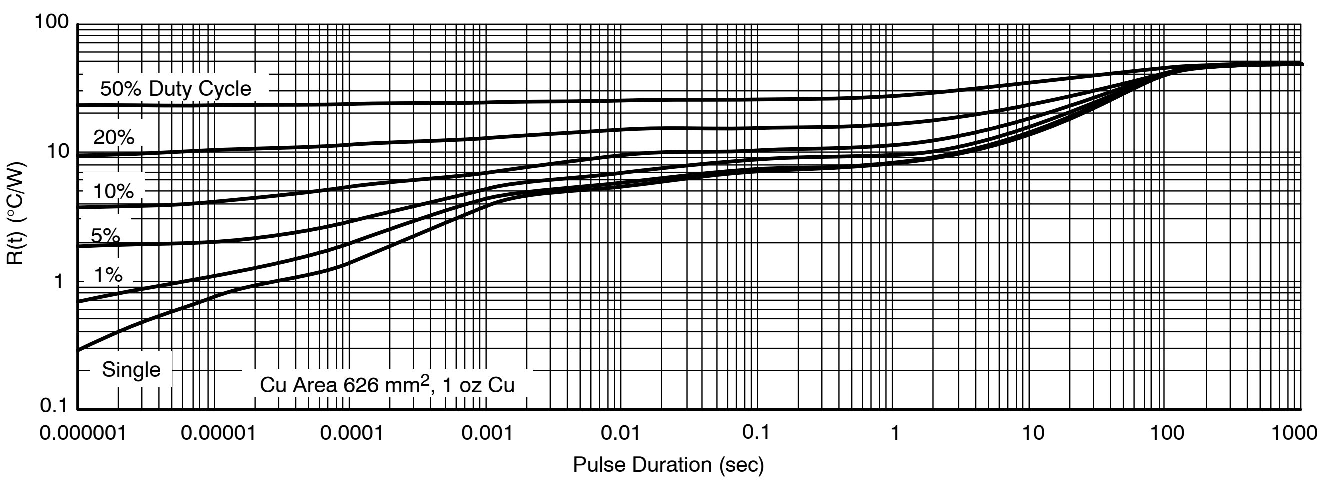


Figure 23. D²PAK 7−Lead Thermal Duty Cycle Curves on 1” Spreader Test Board

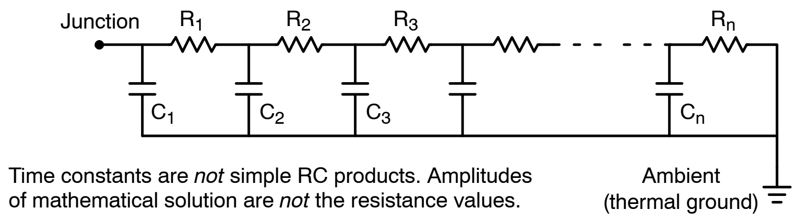


Figure 24. Grounded Capacitor Thermal Network (“Cauer” Ladder)

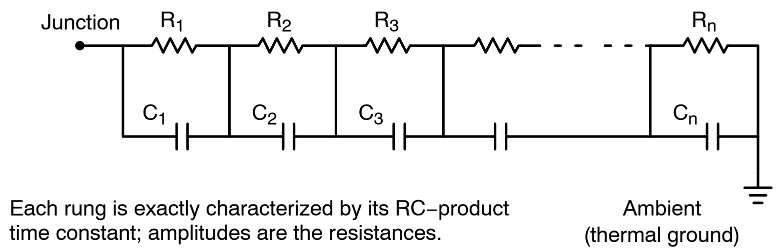


Figure 25. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

Recommend Thermal Data for SOIC−8 EP Package

Parameter	Test Conditions Typical Value		Units
Pad is soldered to PCB copper	**min−pad board** (Note 7)	**1”−pad board** (Note 8)	
Junction−to−Lead (psi−JL, Ψ_{JL})	38	24	°C/W
Junction−to−Lead (psi−JPad, Ψ_{Jp})	8.0	9.0	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	126	64	°C/W

7. 1 oz. copper, 54 mm^2 copper area, 0.062” thick FR4.
8. 1 oz. copper, 717 mm^2 copper area, 0.062” thick FR4.

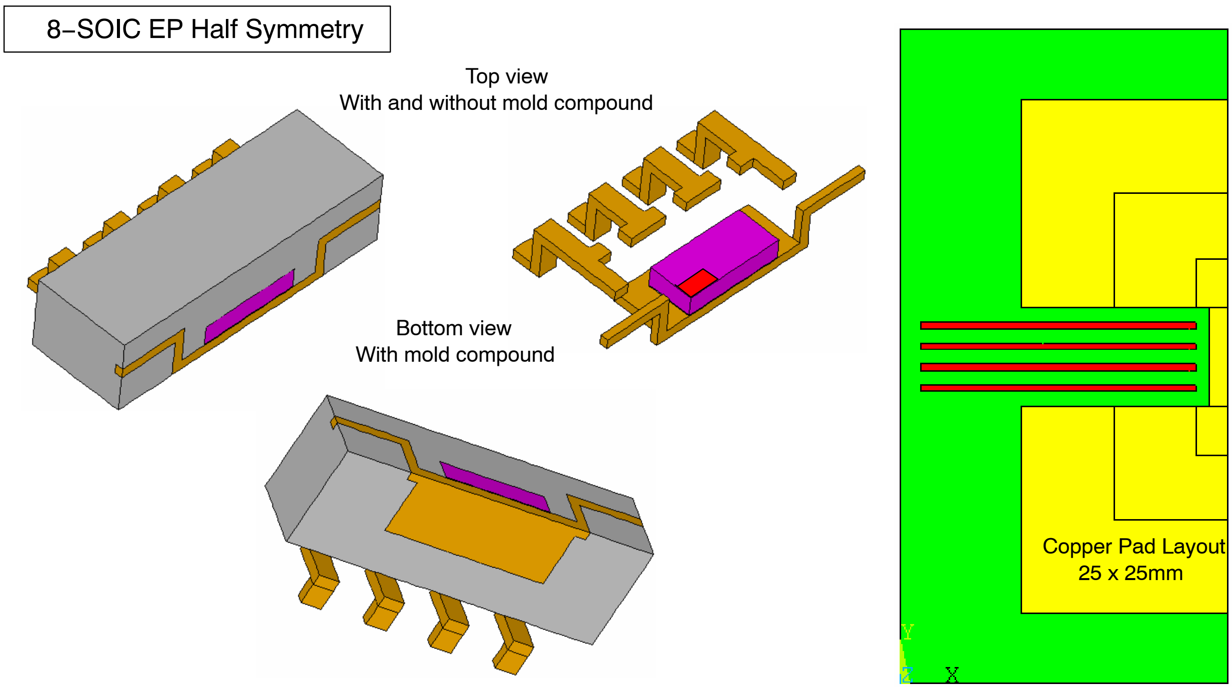


Figure 26. Internal Construction of the Package and PCB Layout for Multiple Pad Area

Table 2. SOIC 8−Lead EP Thermal RC Network Models

	54 mm^2	717 mm^2		54 mm^2	717 mm^2	Cu Area
	Cauer Network			Foster Network		
	C's	C's	Units	Tau	Tau	units
1	2.7E−06	2.7E−06	W−s/C	1.00E−06	1.00E−06	sec
2	1.1E−05	1.1E−05	W−s/C	1.00E−05	1.00E−05	sec
3	3.2E−05	3.2E−05	W−s/C	1.00E−04	1.00E−04	sec
4	1.3E−04	1.3E−04	W−s/C	9.39E−04	9.39E−04	sec
5	1.8E−03	1.8E−03	W−s/C	3.13E−03	3.13E−03	sec
6	7.9E−03	8.3E−03	W−s/C	3.30E−02	3.30E−02	sec
7	2.5E−02	3.1E−02	W−s/C	6.00E−01	6.00E−01	sec
8	1.4E−01	5.1E−01	W−s/C	4.00E+00	4.00E+00	sec
9	4.1E−01	2.1E+00	W−s/C	1.16E+01	4.83E+01	sec
10	1.6E+00	6.3E+01	W−s/C	5.58E+01	2.37E+02	sec
	R's	R's		R's	R's	
1	0.474	0.474	C/W	0.282	0.282	C/W
2	1.086	1.086	C/W	0.610	0.610	C/W
3	3.011	3.010	C/W	1.929	1.929	C/W
4	5.883	5.874	C/W	5.825	5.825	C/W
5	1.944	1.911	C/W	2.700	2.700	C/W
6	4.655	4.264	C/W	3.000	3.000	C/W
7	21.431	15.678	C/W	15.000	15.000	C/W
8	40.130	9.238	C/W	11.494	7.797	C/W
9	23.392	18.454	C/W	34.982	20.473	C/W
10	24.381	3.581	C/W	50.566	5.953	C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 225 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

θJA vs Copper Spreader Area

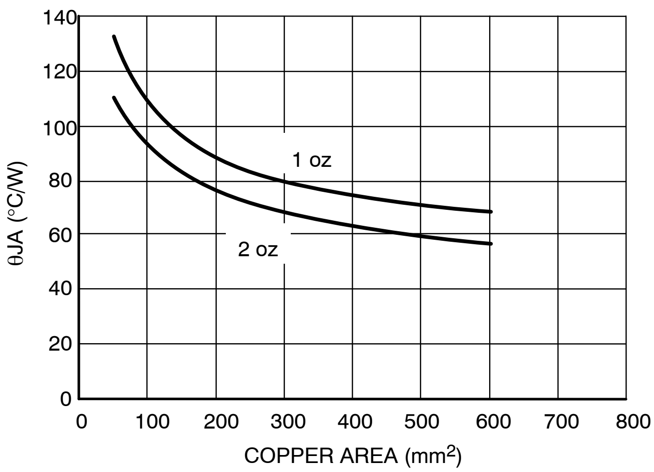


Figure 27. SOIC 8−Lead EP θJA as a Function of the Pad Copper Area Including Traces, Board Material

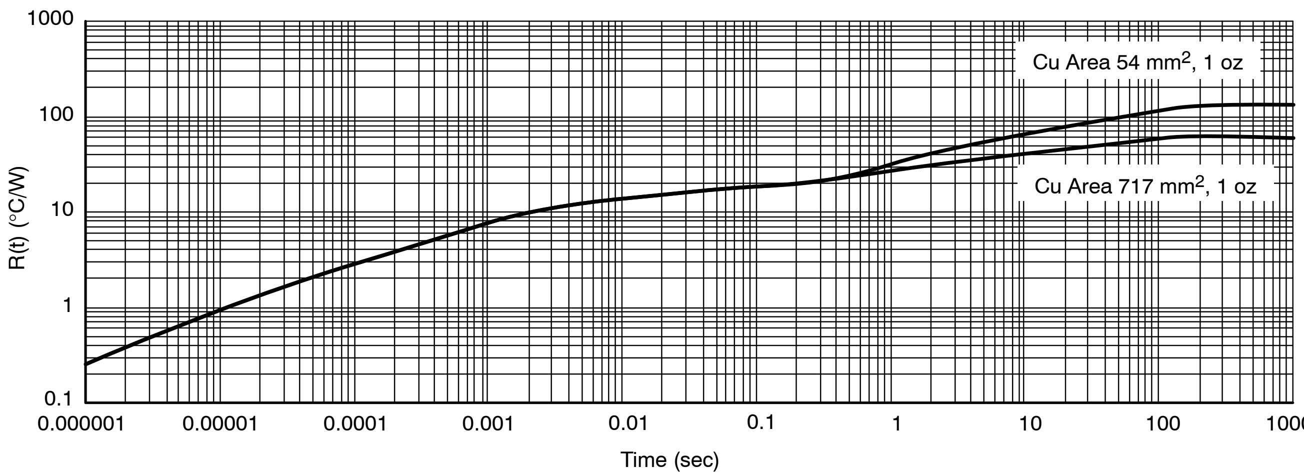


Figure 28. SOIC 8−Lead EP Single Pulse Heating Curve

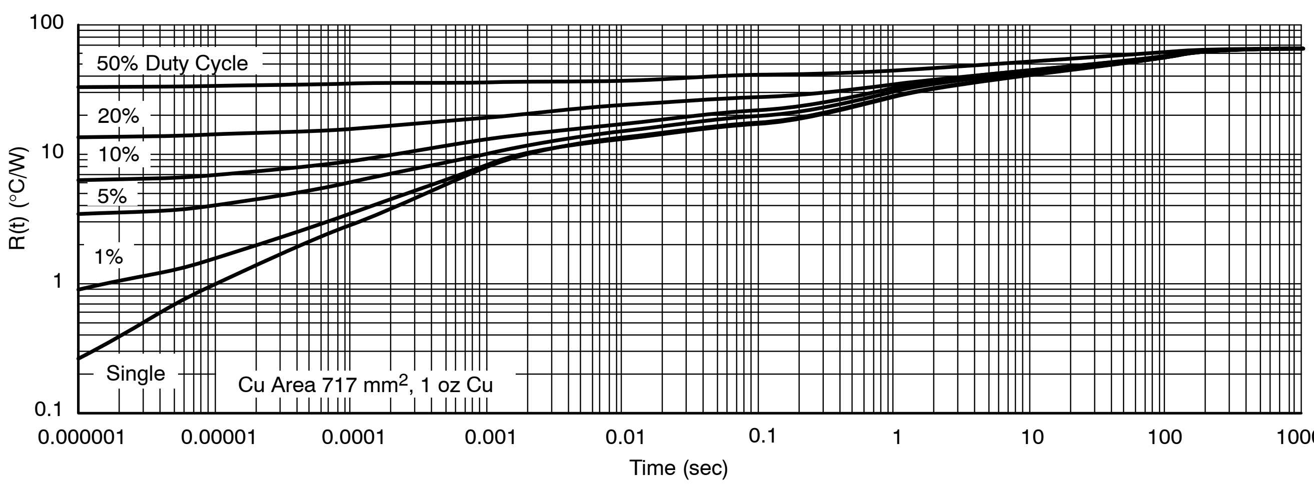


Figure 29. SOIC 8−Lead Thermal Duty Cycle Curves on 1” Spreader Test Board

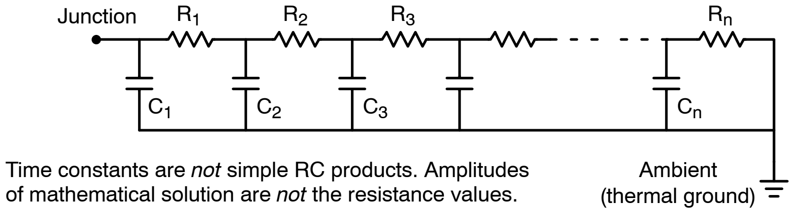


Figure 30. Grounded Capacitor Thermal Network (“Cauer” Ladder)

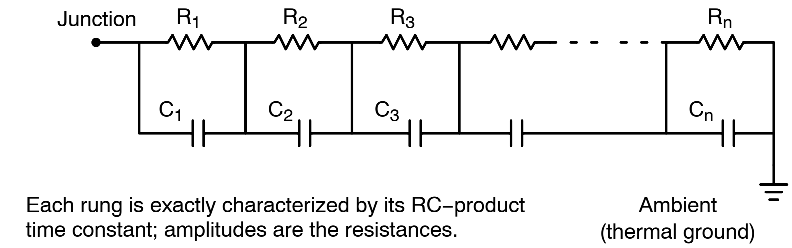


Figure 31. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

APPLICATION NOTES

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 32) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] I_{OUT(max)} + V_{IN(max)} I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application, and
I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

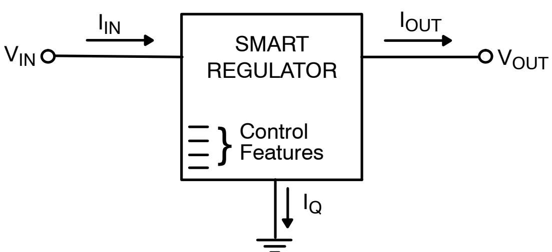


Figure 32. Single Output Regulator with Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

ORDERING INFORMATION

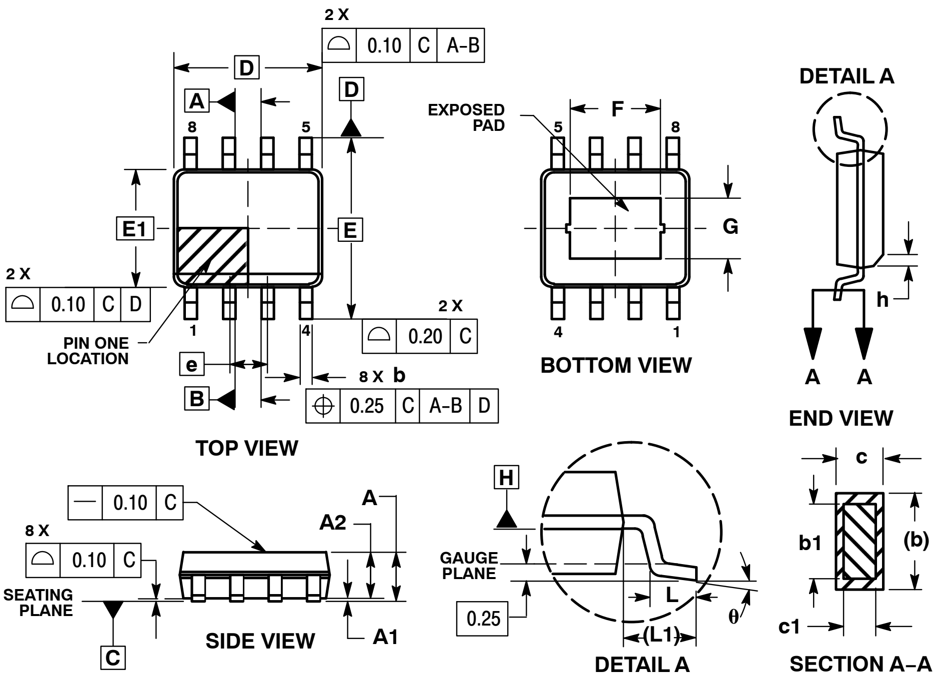
Device	Output Voltage	Timing Option (R_{Delay} = 60 kΩ)	Package	Shipping†
NCV85081BDS50G	5.0 V	Delay Time = 3 ms Wakeup Period = 25 ms RESET HIGH to Wakeup Rising Delay Time = 12.5 ms	D2PAK – 7 (Pb – Free)	50 Units / Rail
NCV85081BDS50R4G	5.0 V	Delay Time = 3 ms Wakeup Period = 25 ms RESET HIGH to Wakeup Rising Delay Time = 12.5 ms	D2PAK – 7 (Pb – Free)	750 / Tape & Reel
NCV85081BPD50R2G	5.0 V	Delay Time = 3 ms Wakeup Period = 25 ms RESET HIGH to Wakeup Rising Delay Time = 12.5 ms	SO – 8 EP (Pb – Free)	2500 / Tape & Reel
NCV85082BPD33R2G	3.3 V	Delay Time = 9 ms Wakeup Period = 75 ms RESET HIGH to Wakeup Rising Delay Time = 37.5 ms	SO – 8 EP (Pb – Free)	2500 / Tape & Reel

NOTE: Contact factory for other options.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

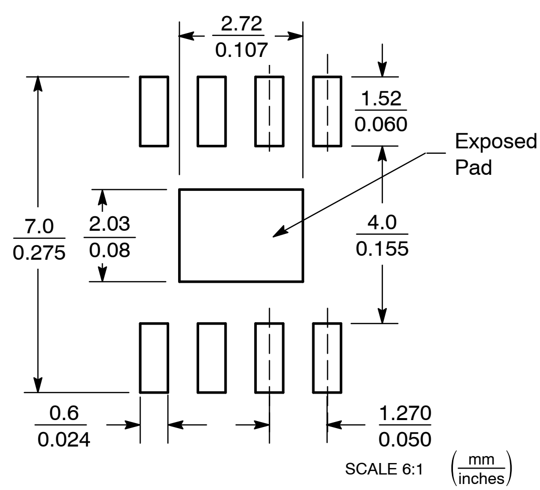
SOIC−8 EP
CASE 751AC−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

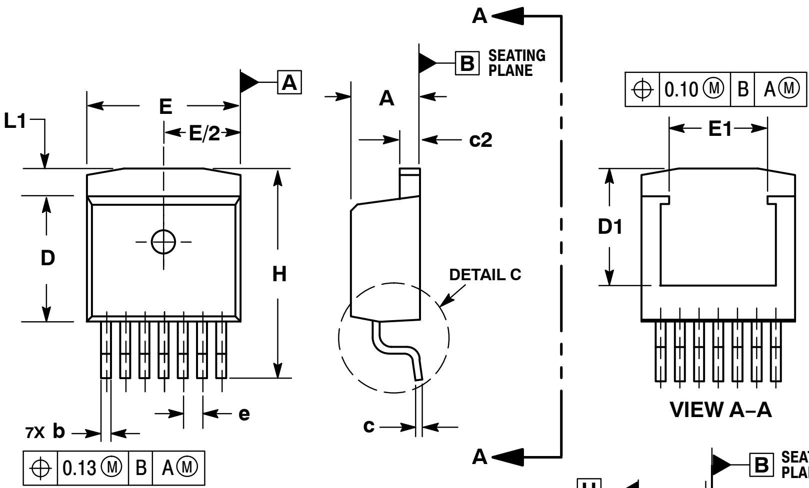
SOLDERING FOOTPRINT*

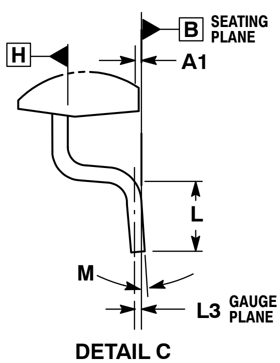


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

D^2PAK−7 (SHORT LEAD)
CASE 936AB−01
ISSUE B

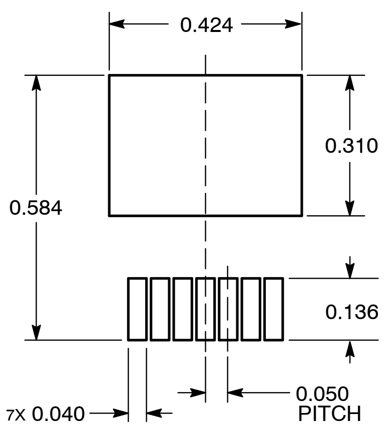




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.270	−−−	6.86	−−−
E	0.380	0.420	9.65	10.67
E1	0.245	−−−	6.22	−−−
e	0.050 BSC		1.27 BSC	
H	0.539	0.579	13.69	14.71
L	0.058	0.078	1.47	1.98
L1	−−−	0.066	−−−	1.68
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Email: orderlit@onsemi.com

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