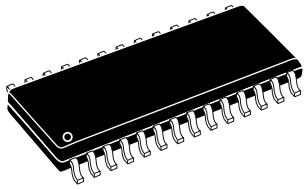
VNQ600P-E

Quad channel high side driver

Datasheet - production data



SO-28 (double island)

GAPG1102151005PS

Features

Type	$R_{DS(on)}$ (1)	I_{lim}	V_{CC}
VNQ600AP-E	35 mΩ	25 A	36 V

1. Per each channel

- DC short circuit current: 22 A
- CMOS compatible inputs
- Proportional load current sense.
- Undervoltage & overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against:
  - Loss of ground & loss of V_{CC}
- Reverse battery protection
- In compliance with the 2002/95/EC european directive

Description

The VNQ600P-E is a quad HSD formed by assembling two VNQ600P-E chips in the same SO-28 package. The VNQ600P-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. The VNQ600P-E is intended for driving any type of multiple loads with one side connected to ground.

This device has four independent channels and four analog sense outputs which deliver currents proportional to the outputs currents.

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28 (double island)	VNQ600P-E	VNQ600PTR-E

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

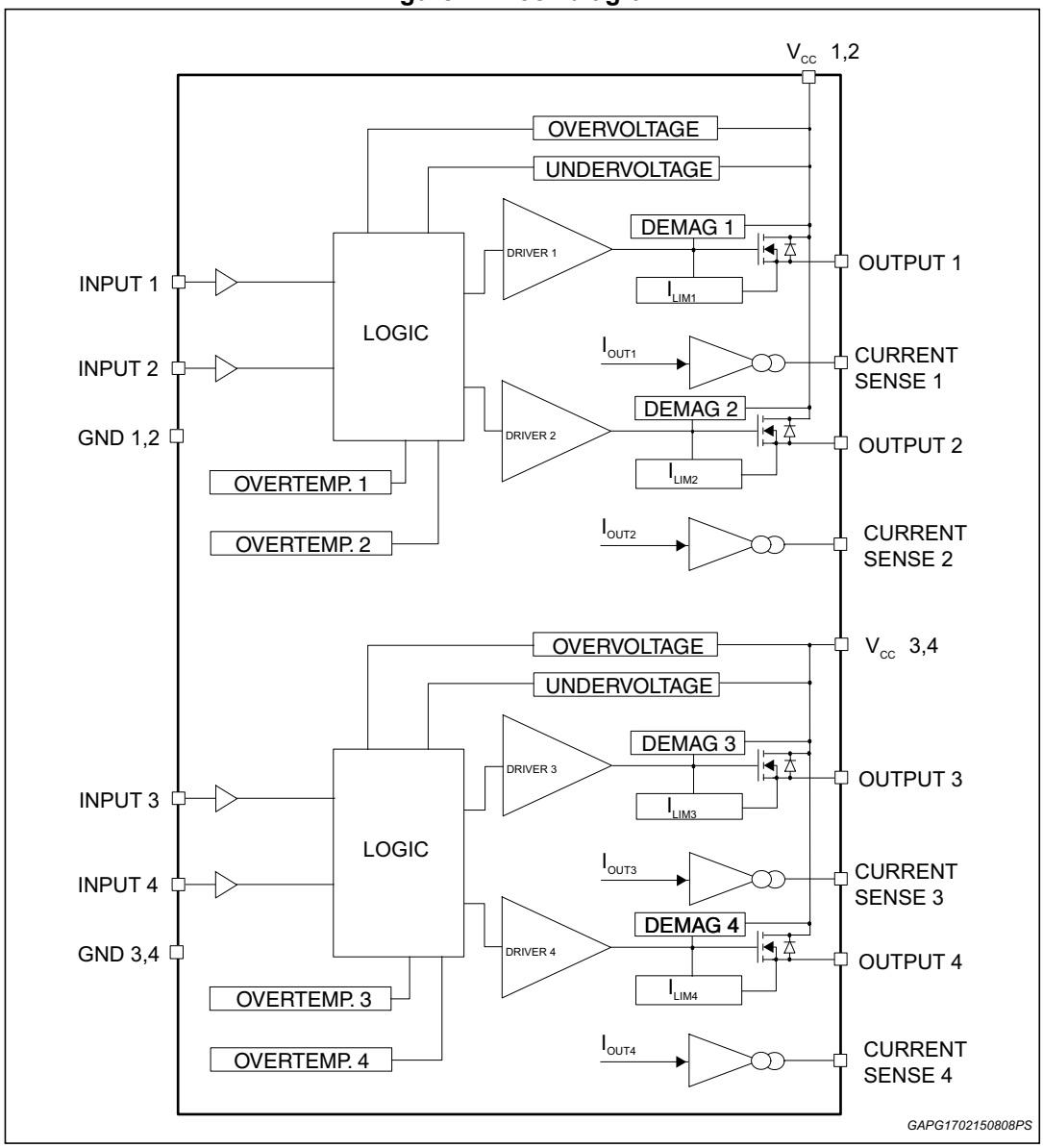


Figure 2. Configuration diagram (top view)

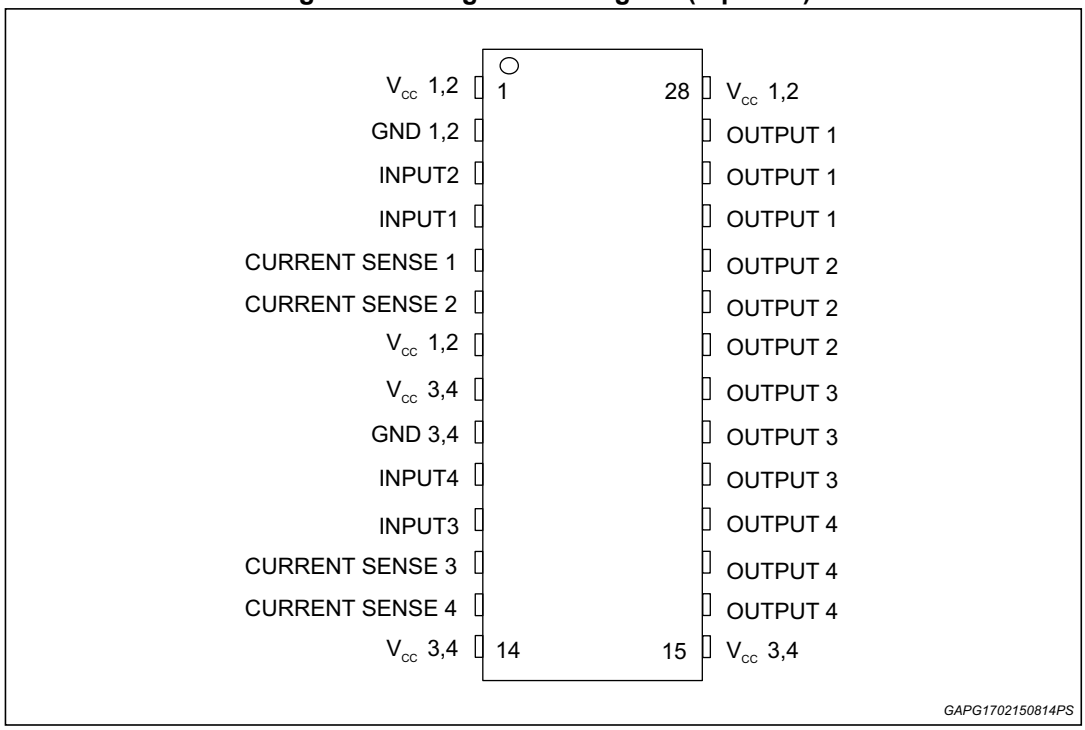


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1 KΩ resistor	X		Through 10 KΩ resistor

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (continuous)	41	V
$-V_{CC}$	Reverse supply voltage (continuous)	-0.3	V
I_{OUT}	Output current (continuous), for each channel	15	A
I_R	Reverse output current (continuous), for each channel	-15	A
I_{IN}	Input current	±10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
I_{GND}	Ground current at $T_{pins} \leq 25$ °C (continuous)	-200	mA
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C=100pF) – INPUT – CURRENT SENSE – OUTPUT – V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum switching energy (L=0.11 mH; R_L= 0 Ω; V_{bat}=13.5 V; T_{jstart}=150ºC; I_L=40 A)	126	mJ
P_{tot}	Power dissipation (per island) at T_{lead} = 25 °C	6.25	W
T_j	Junction operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

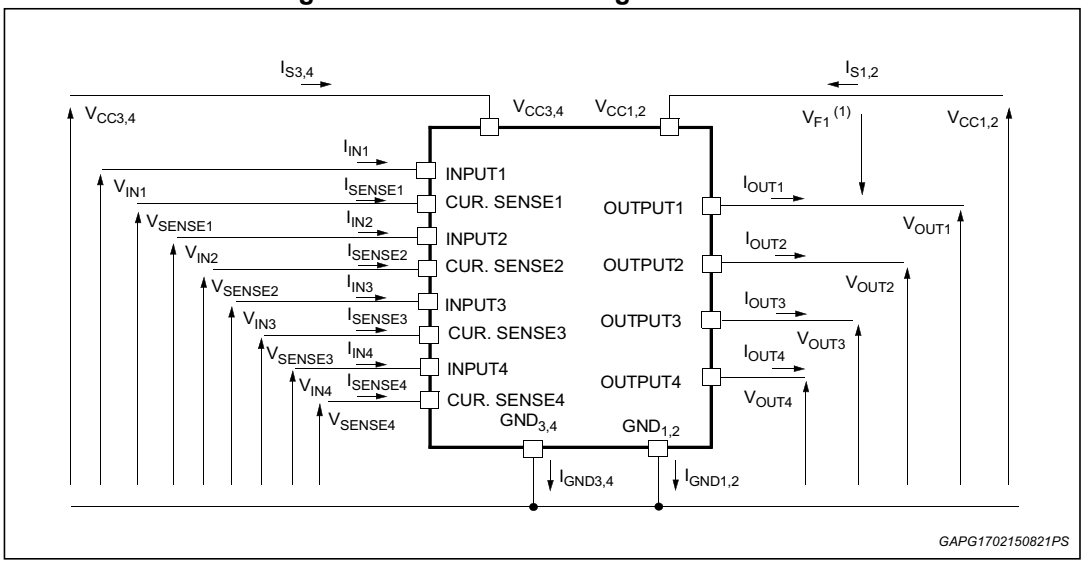
Symbol	Parameter	Value		Unit
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	15		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (one chip ON)	60(1)	44(2)	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance junction-ambient (two chips ON)	46(1)	31(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm^2 of Cu (at least 35 µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C< T_j < 150 °C, unless otherwise stated.

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On state resistance	I_{OUT}1,2,3,4 = 5 A; T_j = 25°C I_{OUT}1,2,3,4 = 5 A; T_j = 50°C I_{OUT}1,2,3,4 = 3 A; V_{CC} = 6 V			35 70 120	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_{CC} = 20 mA	41	48	55	V
I_S	Supply current	Off State; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V Off State; V_{CC} = 13 V; V_{IN}=V_{OUT}=0V; T_j = 25 °C On State; V_{CC} = 13 V; V_{IN} = 5V; I_{OUT} = 0 A; R_{SENSE} = 3.9 KΩ		12 12 	40 25 6	µA µA mA
$I_{L(off1)}$	Off state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off state output current	V_{IN} = 0 V; V_{OUT} = 3.5 V	-75		0	µA
$I_{L(off3)}$	Off state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C			5	µA
$I_{L(off4)}$	Off state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C			3	µA

Note: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	DC Short circuit current	V_{CC} = 13 V 5.5 V < V_{CC} < 36 V	25	40	70 70	A A
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
V_{demag}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.5 A; T_j = -40°C to +150°C		50		mV

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.6 Ω channels 1,2,3,4 (see *Figure 5*)		40		µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.6 Ω channels 1,2,3,4 (see *Figure 5*)		40		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 2.6 Ω channels 1,2,3,4 (see *Figure 5*)		See *Figure 10*		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 2.6 Ω channels 1,2,3,4 (see *Figure 5*)		See *Figure 12*		V/µs

Table 8. Current sense (9 V < V_{CC}< 16 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2} = 0.5 A; V_{SENSE} = 0.5 V; other channels open; T_j= -40 °C...150 °C	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	I_{OUT1} or I_{OUT2} = 0.35 A; V_{SENSE} = 0.5 V; other channels open; T_j = -40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2} = 5 A; V_{SENSE} = 4 V; other channels open; T_j = -40 °C T_j = 25 °C...150 °C	 4200 4400	 4900 4900	 6000 5750	
dK_2/K_2	Current sense ratio drift	I_{OUT1} or I_{OUT2} = 2 A; V_{SENSE} = 2.5 V; other channels open; T_j = -40 °C...150 °C	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2} = 15 A; V_{SENSE} = 4 V; other channels open; T_j = -40 °C; T_j = 25 °C...150 °C	 4200 4400	 4900 4900	 5500 5250	
dK_3/K_3	Current sense ratio drift	I_{OUT1} or I_{OUT2} = 15 A; V_{SENSE} = 4 V; other channels open; T_j = -40 °C...150 °C	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	V_{CC} = 5.5 V; $I_{OUT1,2}$ = 2.5 A; R_{SENSE} = 10 kΩ V_{CC} > 8 V, $I_{OUT1,2}$ = 5 A; R_{SENSE} = 10 kΩ	2 4			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC} = 13 V; R_{SENSE} = 3.9 kΩ		5.5		V

Table 8. Current sense (9 V < V_{CC}< 16 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{VSENSEH}$	Analog sense output Impedance in overtemperature condition	V_{CC}=13V; T_j>T_{TSD}; All channels open		400		W
t_{DSENSE}	Current sense delay response	To 90% I_{SENSE}(1)			500	µs

1. Current sense signal delay after positive input slope.

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage				1.25	V
V_{IH}	High level input voltage		3.25			V
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
I_{IL}	Input current	V_{IN} = 1.5 V	1			µA
I_{IN}	Input current	V_{IN} = 3.5 V			10	µA
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA I_{IN} = -1 mA	6	6.8 -0.7	8	V V

Table 10. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	-I_{OUT} = 2.3 A; T_j = 150 °C			0.6	V

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

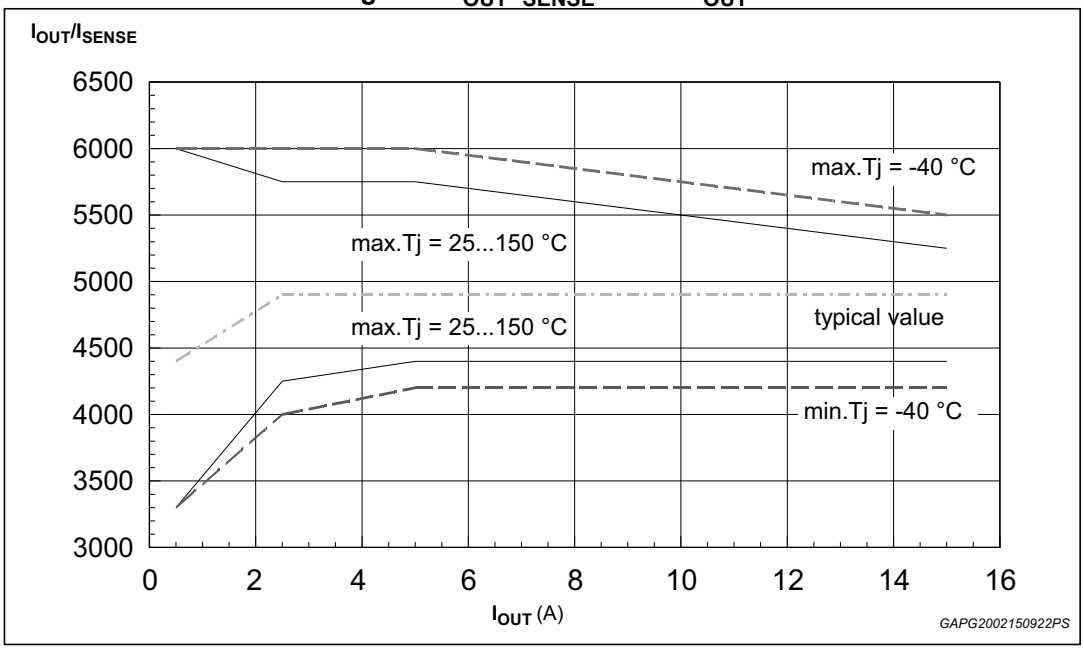


Figure 5. Switching characteristics

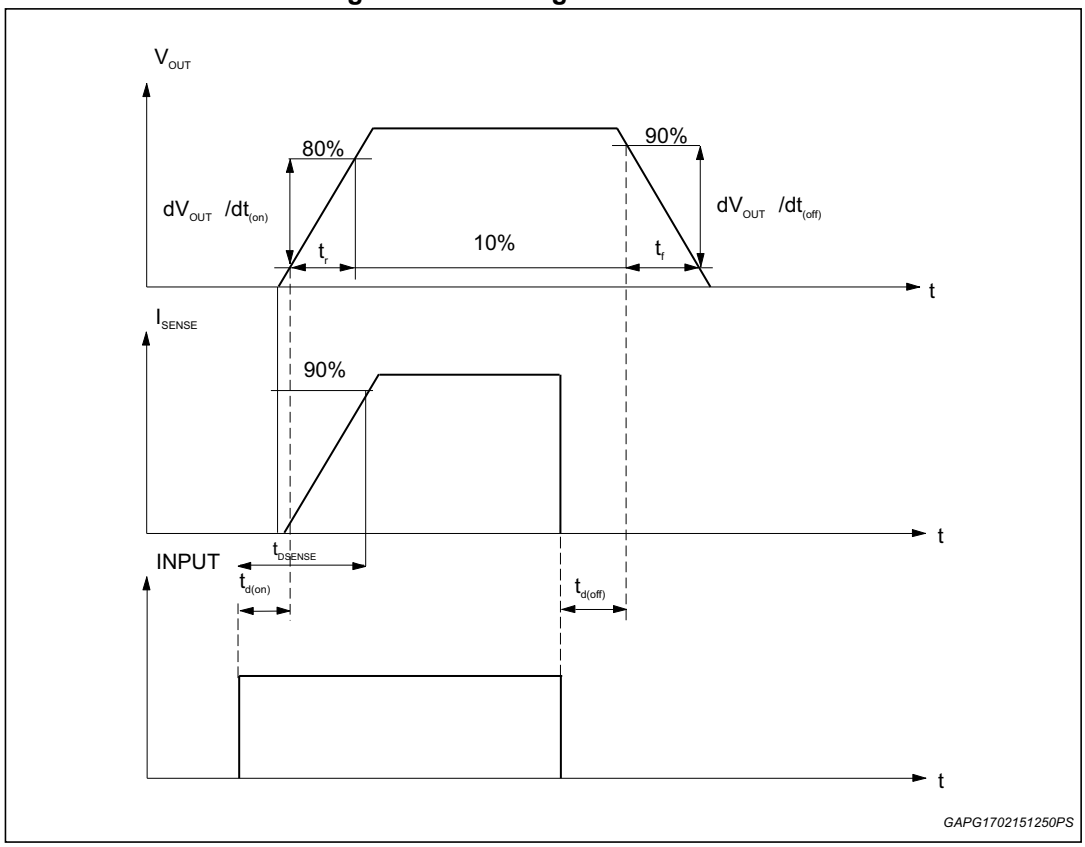


Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements (part 1/3)

ISO T/R 7637/1 Test pulse	Test levels I	Test levels II	Test levels III	Test levels IV	Test levels delays and impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1µs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400ms, 2 Ω

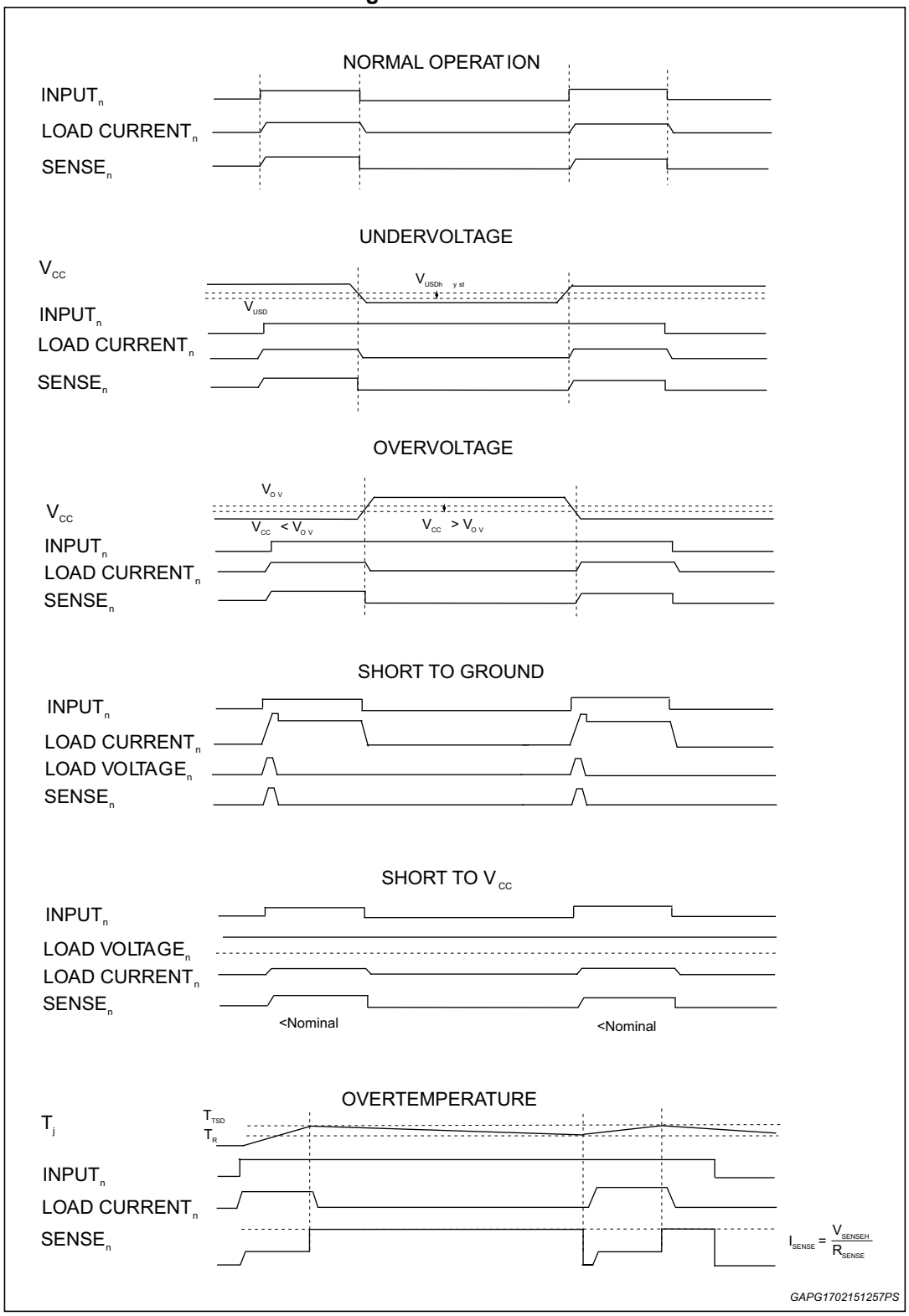
Table 13. Electrical transient requirements (part 2/3)

ISO T/R 7637/1 Test pulse	Test levels result I	Test levels result II	Test levels result III	Test levels result IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



3 Electrical characteristics curves

Figure 7. Off state output current

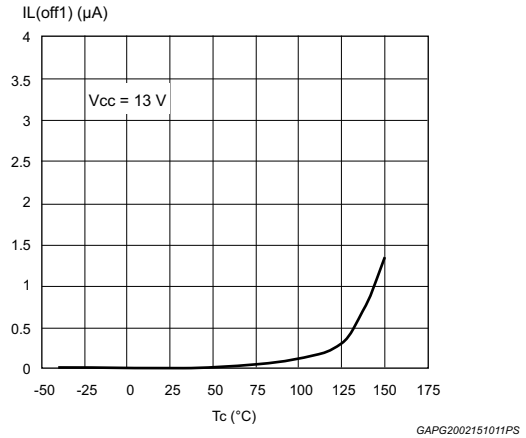


Figure 8. Low level input current

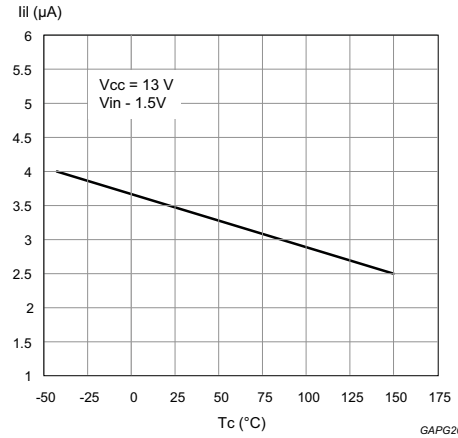


Figure 9. Input clamp voltage

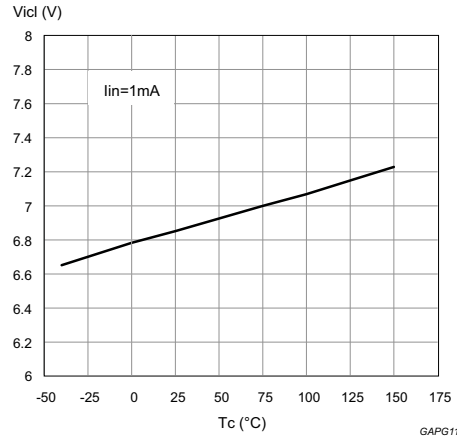


Figure 10. Turn-on voltage slope

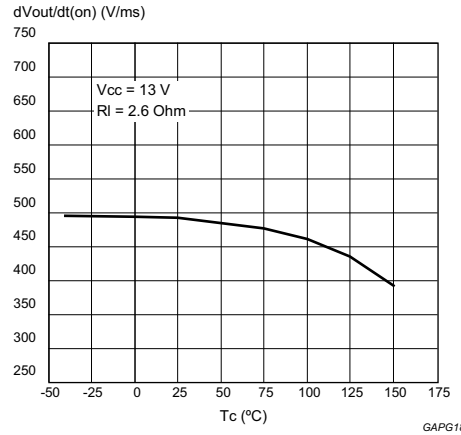


Figure 11. Overvoltage shutdown

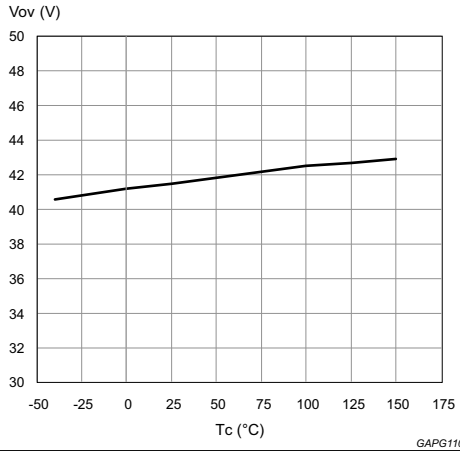


Figure 12. Turn-off voltage slope

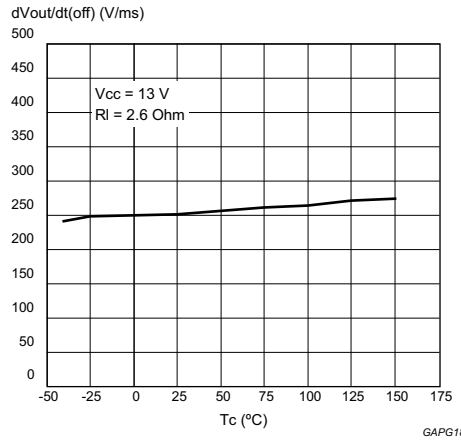


Figure 13. I_{LIM} vs T_{case}

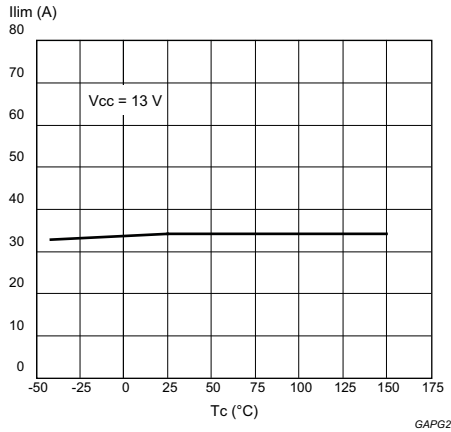


Figure 14. Input low level

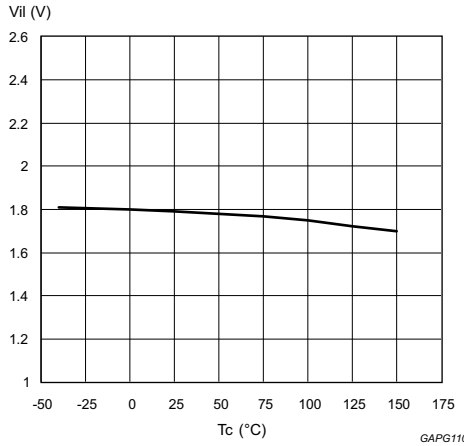


Figure 15. Input high level

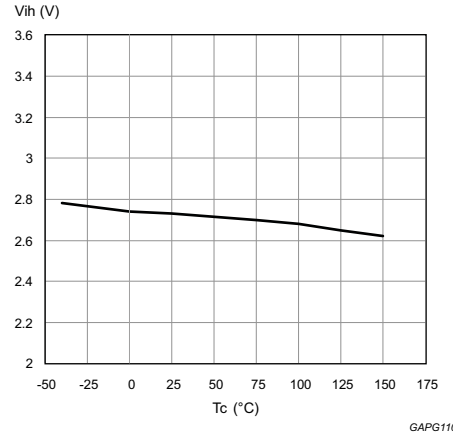


Figure 16. Input hysteresis voltage

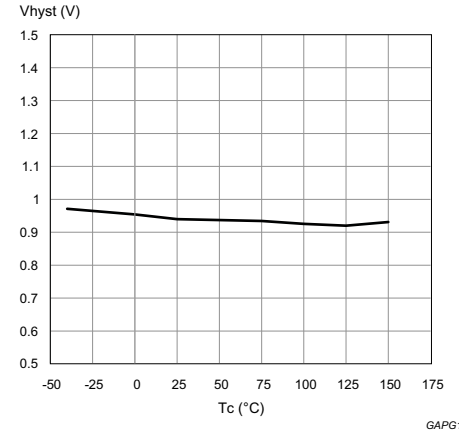
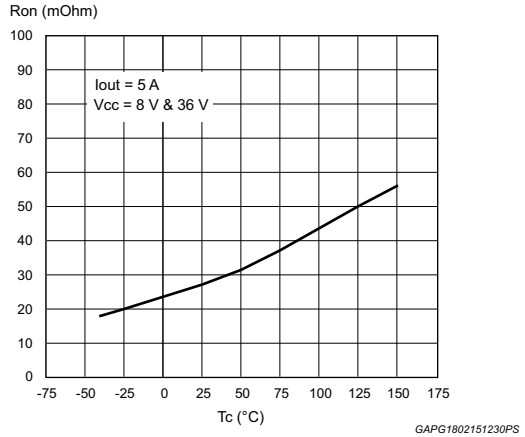
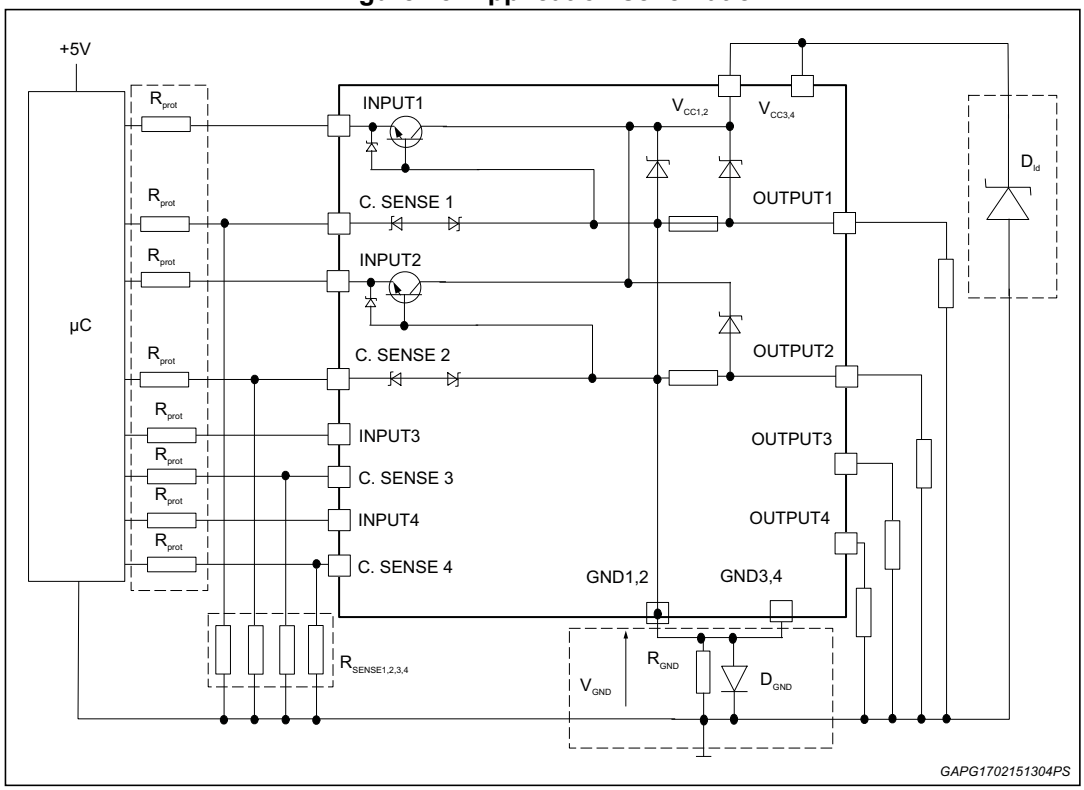


Figure 17. On state resistance vs T_{case}



4 Application information

Figure 18. Application schematic



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

4.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

4.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600mV / 2(I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC}<0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2/R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

4.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (RGND=1kΩ) should be inserted in parallel to DGND if the device will be driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

4.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

4.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

V_{CCpeak}= - 100 V

$I_{latchup}$ ≥ 20 mA

$V_{OH\mu C}$ ≥ 4.5V

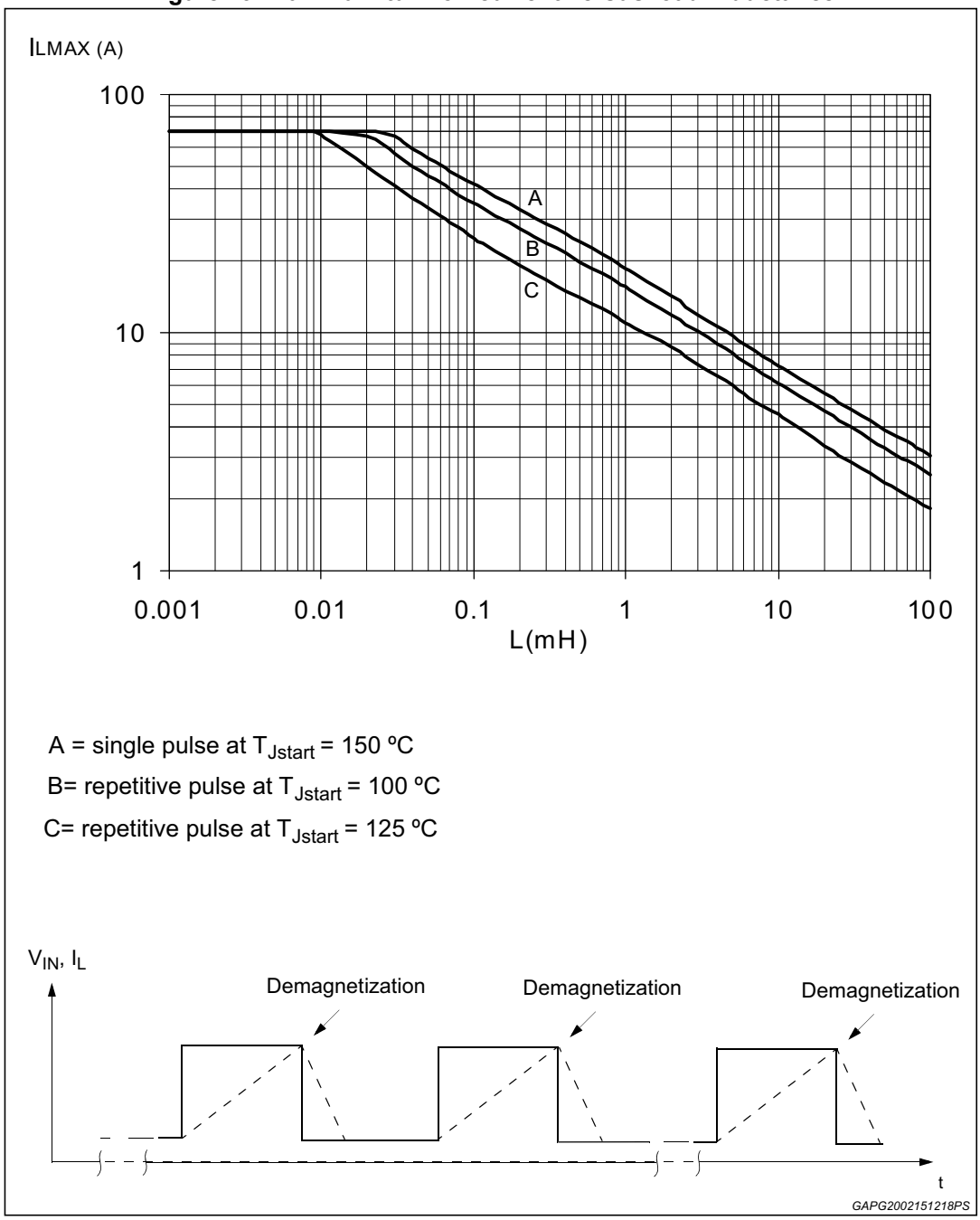
5 kΩ ≤ R_{prot} ≤ 65 kΩ.

Recommended values are:

R_{prot} =10 kΩ

4.4 Maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 19. Maximum turn-off current versus load inductance



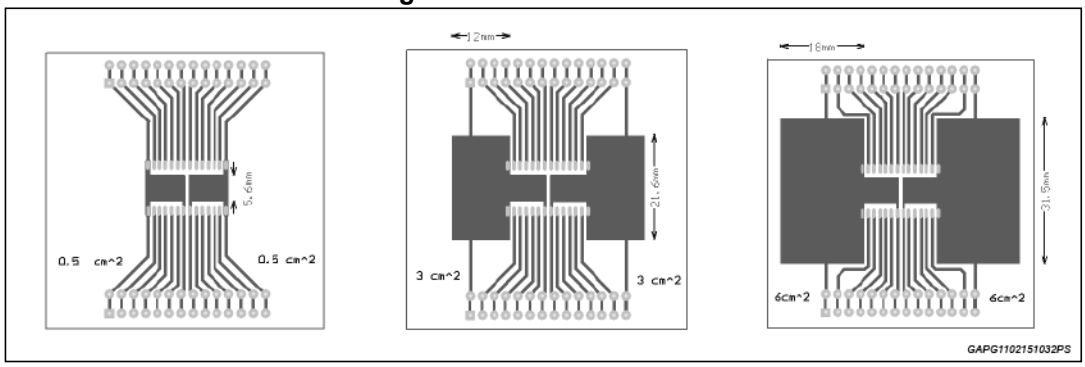
Note: Values are generated with R_L=0Ω.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

5 Package and PCB thermal data

5.1 SO-28 thermal data

Figure 20. SO-28 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: 0.5 cm^2, 3 cm^2, 6 cm^2).

Table 15. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1}=P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = Thermal resistance Junction to Ambient with one chip ON

R_{thB} = Thermal resistance Junction to Ambient with both chips ON and $P_{dchip1}=P_{dchip2}$

R_{thC} = Mutual thermal resistance

Figure 21. $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition

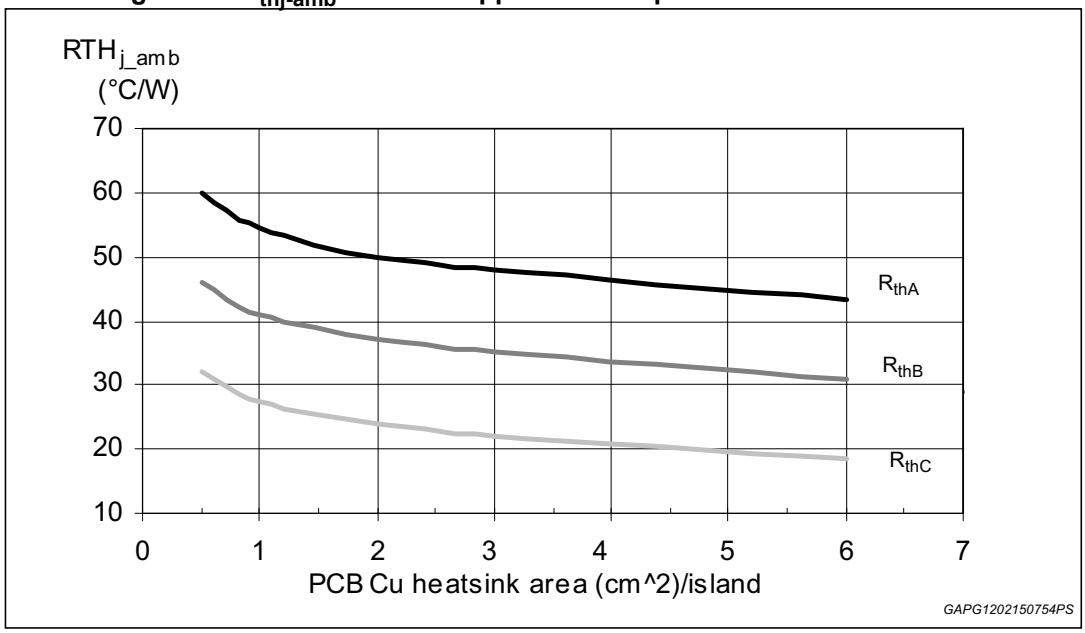
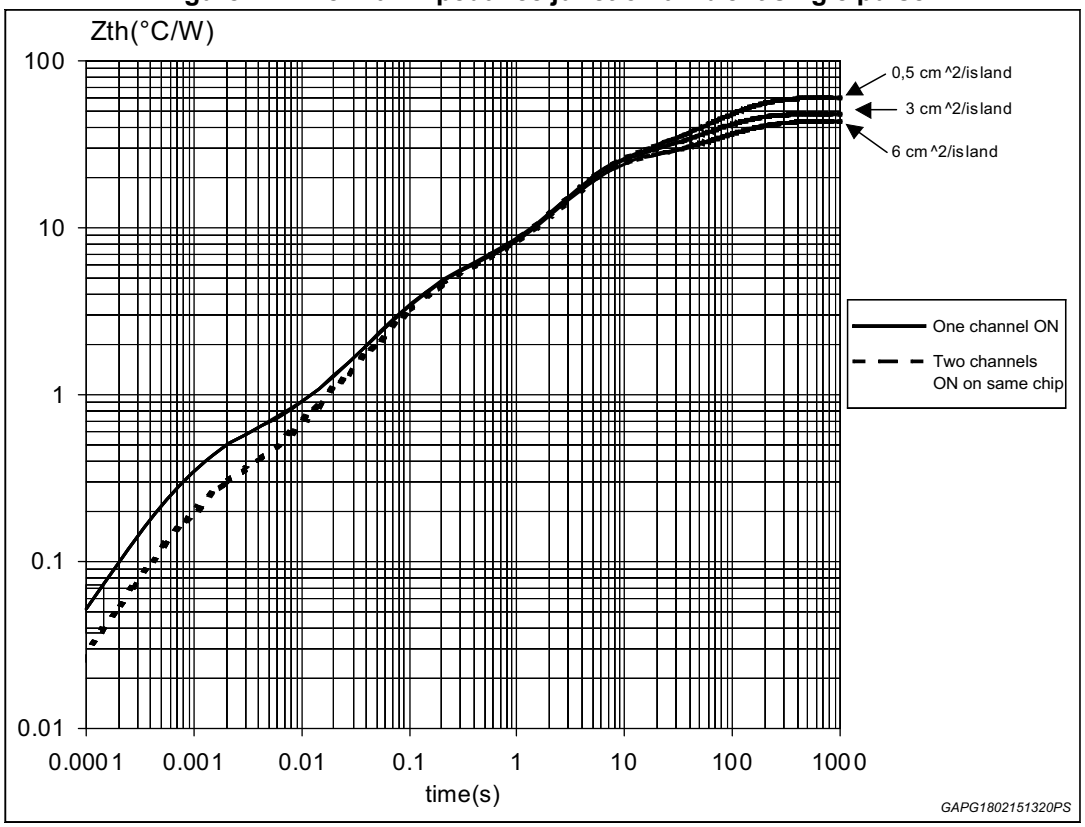


Figure 22. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 23. Thermal fitting model of a quad channel HSD in SO-28

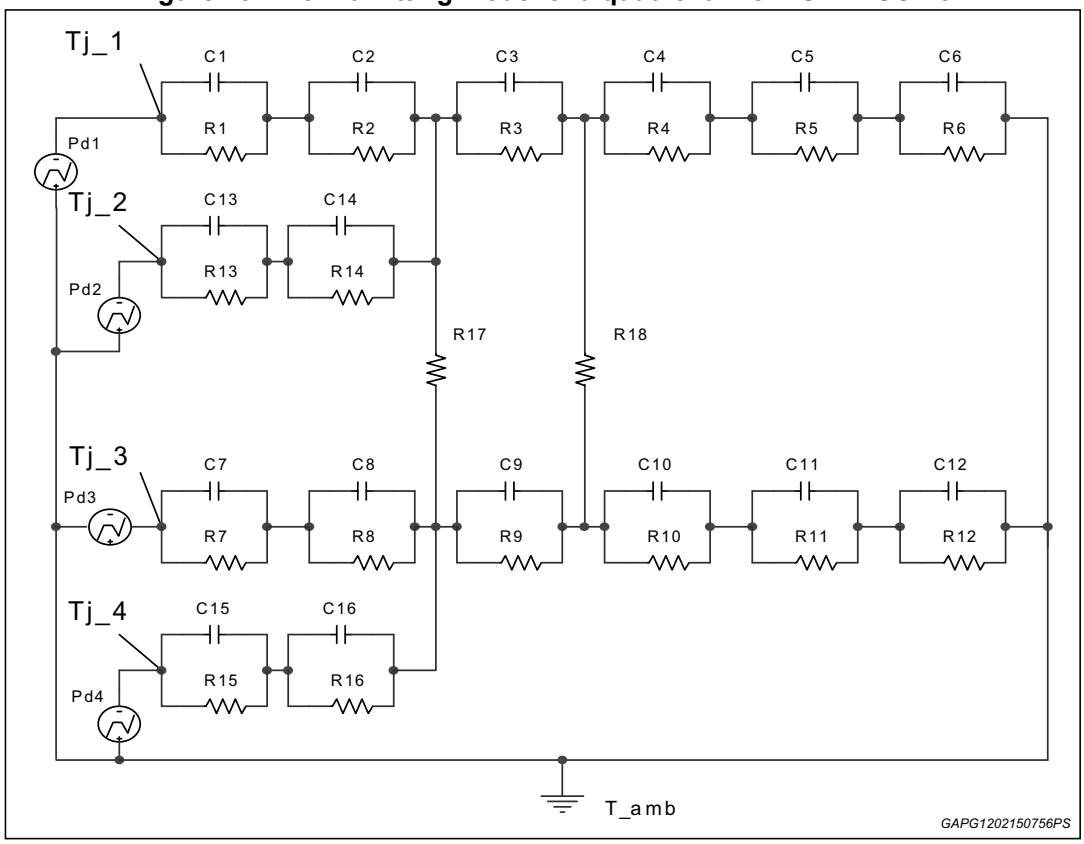


Table 16. Thermal parameters

Area/island (cm^2)	0.5	6
R1=R7=R13=R15 (°C/W)	0.05	
R2=R8=R14=R16 (°C/W)	0.3	
R3=R9 (°C/W)	3.4	
R4=R10 (°C/W)	11	
R5=R11 (°C/W)	15	
R6=R12 (°C/W)	30	13
C1=C7=C13=C15 (W.s/°C)	0.001	
C2=C8=C14=C16 (W.s/°C)	5.00E-03	
C3=C9 (W.s/°C)	1.00E-02	
C4=C10 (W.s/°C)	0.2	
C5=C11 (W.s/°C)	1.5	
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 SO-28 package information

Figure 24. SO-28 package outline

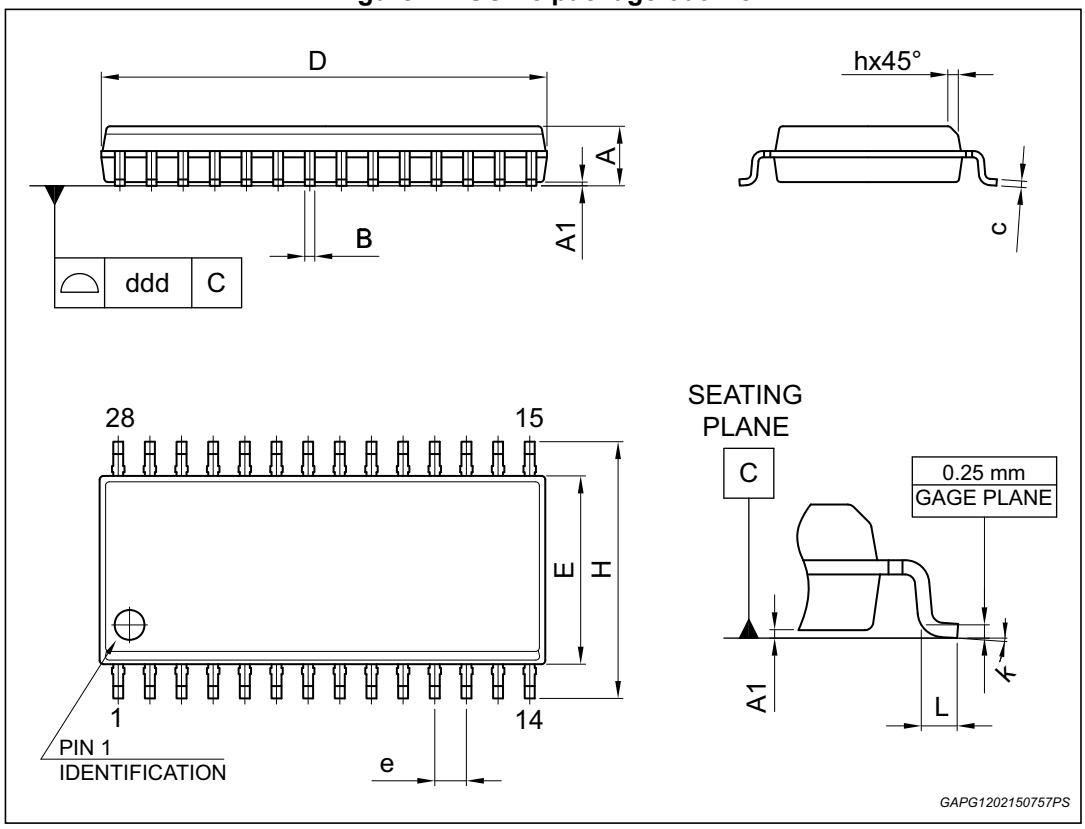


Table 17. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D(1)	17.70		18.10

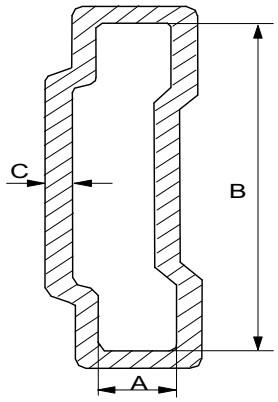
Table 17. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

6.2 SO-28 packing information

Figure 25. SO-28 tube shipment (no suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

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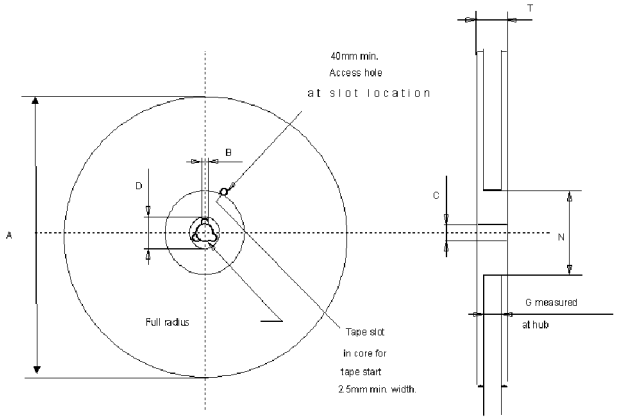
Figure 26. SO-28 tape and reel shipment (suffix "TR")



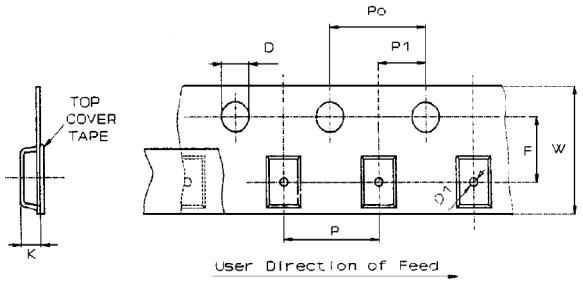
Reel dimensions

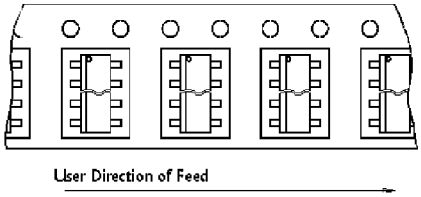
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

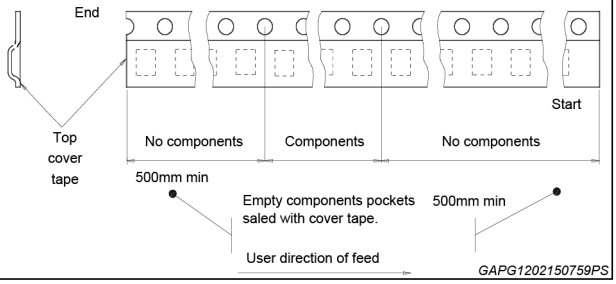
Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Description	Dimensions	mm
Tape width	W (± 0.3)	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	3.1
Hole Spacing	P1 (± 0.1)	2







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7 Revision history

Table 18. Document revision history

Date	Revision	Changes
Oct-2004	1	Initial release.
02-Jul-2006	2	Added *Table 18: Document revision history*.
11-Nov-2008	3	Document converted to corporate template.
25-Sep-2013	4	Updated disclaimer.
20-Feb-2015	5	Updated: – *Section 6.1: SO-28 package information*; – Tape dimensions in *Figure 26: SO-28 tape and reel shipment (suffix "TR") on page 25*.

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