PCA9624

8-bit Fm+ I²C-bus 100 mA 40 V LED driver

Rev. 4.1 — 18 January 2016 Product data sheet

1. General description

The PCA9624 is an I²C-bus controlled 8-bit LED driver optimized for voltage switch dimming and blinking 100 mA Red/Green/Blue/Amber (RGBA) LEDs. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0 % to 99.6 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9624 operates with a supply voltage range of 2.3 V to 5.5 V and the 100 mA open-drain outputs allow voltages up to 40 V.

The PCA9624 is one of the first LED controller devices in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and more densely populated bus operation (up to 4000 pF).

The active LOW Output Enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices must be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCA9624 devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. Seven hardware address pins allow up to 126 devices on the same bus.

The Software Reset (SWRST) Call allows the master to perform a reset of the PCA9624 through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the outputs to be set HIGH (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

The PCA9624 and PCA9634 software is identical and if the PCA9624 on-chip 100 mA NAND FETs do not provide enough current or voltage to drive the LEDs, then the PCA9634 with larger current or higher voltage external drivers can be used.

2. Features and benefits

- 8 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
- 1 MHz Fast-mode Plus compatible I²C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness using a 97 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 190 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 24 Hz to 10.73 s and duty cycle from 0 % to 99.6 %
- Eight open-drain outputs can sink between 0 mA to 100 mA and are tolerant to a maximum off state voltage of 40 V. No input function.
- Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time (default to 'Change on STOP').
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs
- 7 hardware address pins allow 126 PCA9624 devices to be connected to the same I²C-bus and to be individually programmed
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCA9624s on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that $\frac{1}{3}$ of all devices on the bus can be addressed at the same time in a group). Software enable and disable for I²C-bus address.
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 25 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage (V_{DD}) range of 2.3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP24, HVQFN24

3. Applications

- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices

4. Ordering information

Table 1. Ordering information

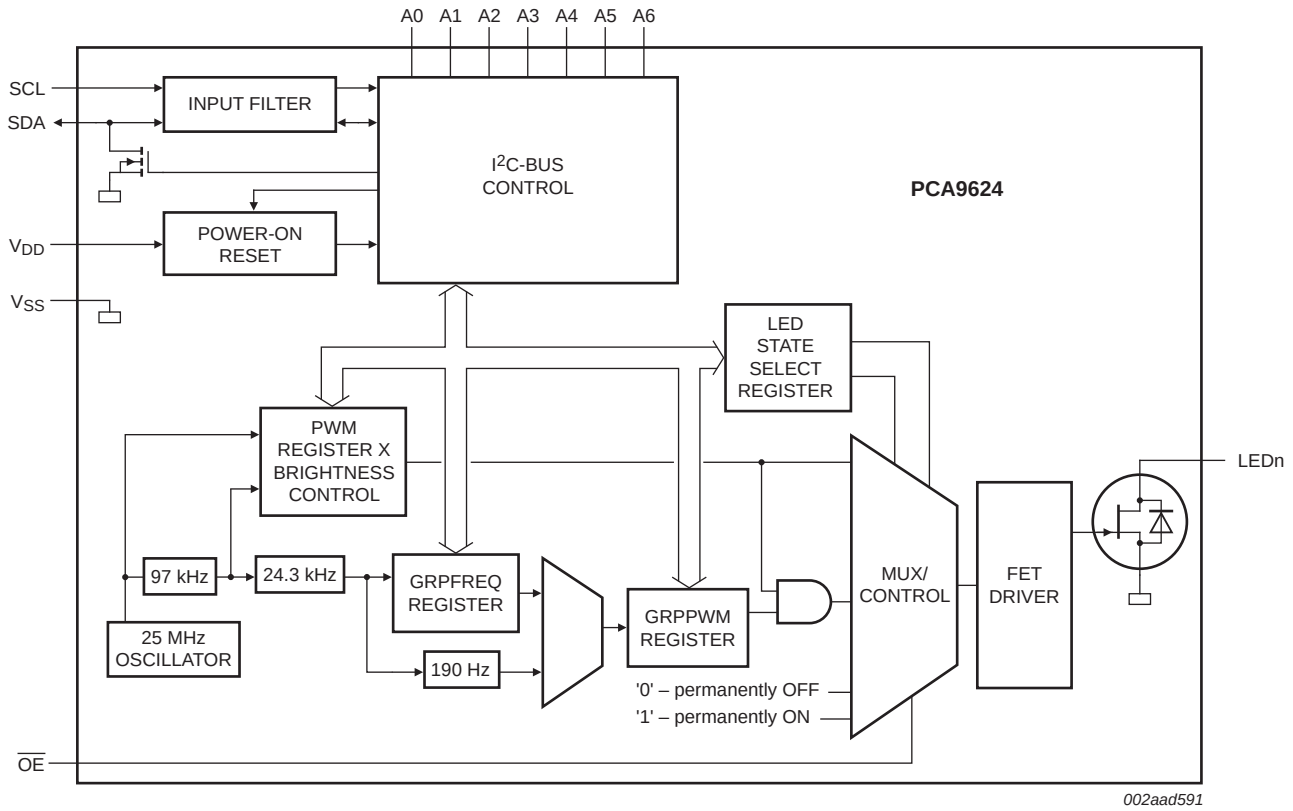
Type number	Topside mark	Package		
		Name	Description	Version
PCA9624BS	9624	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3
PCA9624PW	PCA9624PW	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9624BS	PCA9624BS,118	HVQFN24	Reel 13” Q1/T1 *Standard mark SMD	6000	T_{amb} = –40 °C to +85 °C
PCA9624PW	PCA9624PW,112	TSSOP24	Standard marking * IC’s tube - DSC bulk pack	1575	T_{amb} = –40 °C to +85 °C
	PCA9624PW,118	TSSOP24	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +85 °C

5. Block diagram



Remark: Only one LED output shown for clarity.

Fig 1. Block diagram of PCA9624

6. Pinning information

6.1 Pinning

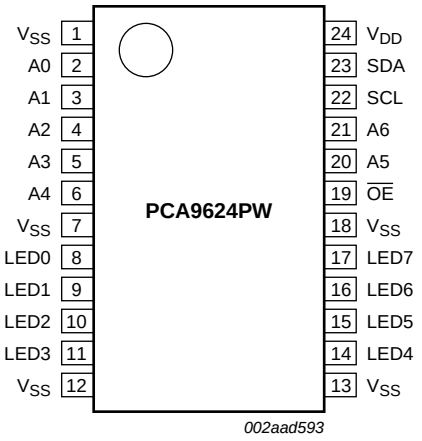


Fig 2. Pin configuration for TSSOP

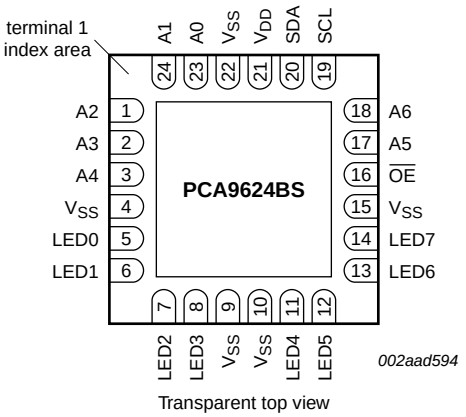


Fig 3. Pin configuration for HVQFN24

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	TSSOP24	HVQFN24		
V_{SS}	1, 7, 12, 13, 18	4, 9, 22, 10, 15[1]	power supply	supply ground
A0	2	23	I	address input 0
A1	3	24	I	address input 1
A2	4	1	I	address input 2
A3	5	2	I	address input 3
A4	6	3	I	address input 4
LED0	8	5	O	LED driver 0
LED1	9	6	O	LED driver 1
LED2	10	7	O	LED driver 2
LED3	11	8	O	LED driver 3
LED4	14	11	O	LED driver 4
LED5	15	12	O	LED driver 5
LED6	16	13	O	LED driver 6
LED7	17	14	O	LED driver 7
$\overline{OE}$	19	16	I	active LOW output enable
A5	20	17	I	address input 5
A6	21	18	I	address input 6
SCL	22	19	I	serial clock line
SDA	23	20	I/O	serial data line
V_{DD}	24	21	power supply	supply voltage

[1] HVQFN24 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCA9624”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

There are a maximum of 128 possible programmable addresses using the 7 hardware address pins. Two of these addresses, Software Reset and LED All Call, cannot be used because their default power-up state is ON, leaving a maximum of 126 addresses. Using other reserved addresses, as well as any other Sub Call address, reduces the total number of possible addresses even further.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCA9624 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

Remark: Using reserved I²C-bus addresses interferes with other devices, but only if the devices are on the bus and/or the bus is open to other I²C-bus systems at some later date. In a closed system where the designer controls the address assignment these addresses can be used since the PCA9624 treats them like any other address. The LED All Call, Software Rest and PCA9564 or PCA9665 slave address (if on the bus) can never be used for individual device addresses.

- PCA9624 LED All Call address (1110 000) and Software Reset (0000 0110) which are active on start-up
- PCA9564 (0000 000) or PCA9665 (1110 000) slave address which is active on start-up
- ‘reserved for future use’ I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)

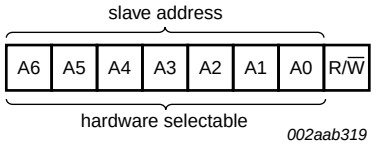


Fig 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled. PCA9624 sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.8 “ALLCALLADR, LED All Call I²C-bus address” for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All the PCA9624s on the I²C-bus acknowledge the address if sent by the I²C-bus master.

7.1.3 LED Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: E2h or 1110 001
  - SUBADR2 register: E4h or 1110 010
  - SUBADR3 register: E8h or 1110 100
- Programmable through I²C-bus (volatile programming)
- At power-up, Sub Call I²C-bus addresses are disabled. PCA9624 does not send an ACK when E2h (R/$\overline{W}$ = 0) or E3h (R/$\overline{W}$ = 1), E4h (R/$\overline{W}$ = 0) or E5h (R/$\overline{W}$ = 1), or E8h (R/$\overline{W}$ = 0) or E9h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.7 “SUBADR1 to SUBADR3, I²C-bus subaddress 1 to 3” for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.1.4 Software Reset I²C-bus address

The address shown in Figure 5 is used when a reset of the PCA9624 must be performed by the master. The Software Reset address (SWRST Call) must be used with R/$\overline{W}$ = logic 0. If R/$\overline{W}$ = logic 1, the PCA9624 does not acknowledge the SWRST. See Section 7.6 “Software reset” for more detail.

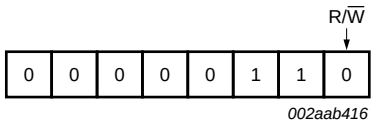


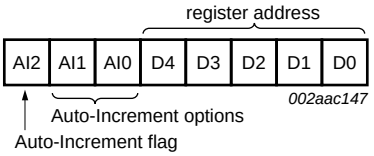
Fig 5. Software Reset address

Remark: The Software Reset I²C-bus address is a reserved address and cannot be used as a regular I²C-bus slave address or as an LED All Call or LED Sub Call address.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master sends a byte to the PCA9624, which is stored in the Control register.

The lowest 5 bits are used as a pointer to determine which register is accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).



reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address.

Fig 6. Control register

When the Auto-Increment flag is set (AI2 = logic 1), the five low-order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 4. Auto-Increment options

AI2	AI1	AI0	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for all registers. D[4:0] roll over to 00h after the last register (11h) is accessed.
1	0	1	Auto-Increment for individual brightness registers only. D[4:0] roll over to 02h after the last register (11h) is accessed.
1	1	0	Auto-Increment for global control registers only. D[4:0] roll over to 0Ah' after the last register (0Bh) is accessed.
1	1	1	Auto-Increment for individual and global control registers only. D[4:0] roll over to 02h after the last register (0Bh) is accessed.

Remark: Other combinations not shown in Table 4 (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the 16 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I²C-bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individual and global changes must be performed during the same I²C-bus communication, for example, changing a color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When the Control register is written, the register entry point determined by D[4:0] is the first register that is addressed (read or write operation), and can be anywhere between 0 0000 and 1 0001 (as defined in Table 5). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AI[2:0]. See Table 4 for rollover values. For example, if the Control register = 1110 0100 (E4h), then the register addressing sequence is (in hexadecimal):
04 → … → 0B → 02 → … → 0B → 02 → … → 0B → 02 → … → 0B → 02 → … as long as the master keeps sending or reading data.

7.3 Register definitions

Table 5. Register summary[1]

Register number	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	0	1	0	PWM0	read/write	brightness control LED0
03h	0	0	0	1	1	PWM1	read/write	brightness control LED1
04h	0	0	1	0	0	PWM2	read/write	brightness control LED2
05h	0	0	1	0	1	PWM3	read/write	brightness control LED3
06h	0	0	1	1	0	PWM4	read/write	brightness control LED4
07h	0	0	1	1	1	PWM5	read/write	brightness control LED5
08h	0	1	0	0	0	PWM6	read/write	brightness control LED6
09h	0	1	0	0	1	PWM7	read/write	brightness control LED7
0Ah	0	1	0	1	0	GRPPWM	read/write	group duty cycle control
0Bh	0	1	0	1	1	GRPFREQ	read/write	group frequency
0Ch	0	1	1	0	0	LEDOUT0	read/write	LED output state 0
0Dh	0	1	1	0	1	LEDOUT1	read/write	LED output state 1
0Eh	0	1	1	1	0	SUBADR1	read/write	I²C-bus subaddress 1
0Fh	0	1	1	1	1	SUBADR2	read/write	I²C-bus subaddress 2
10h	1	0	0	0	0	SUBADR3	read/write	I²C-bus subaddress 3
11h	1	0	0	0	1	ALLCALLADR	read/write	LED All Call I²C-bus address

[1] Only D[4:0] = 0 0000 to 1 0001 are allowed and are acknowledged. D[4:0] = 1 0010 to 1 1111 are reserved and are not acknowledged.

7.3.1 Mode register 1, MODE1

Table 6. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AI2	read only	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled.
6	AI1	read only	0*	Auto-Increment bit 1 = 0.
			1	Auto-Increment bit 1 = 1.
5	AI0	read only	0*	Auto-Increment bit 0 = 0.
			1	Auto-Increment bit 0 = 1.
4	SLEEP[1]	R/W	0	Normal mode[2].
			1*	Low-power mode. Oscillator off[3].
3	SUB1	R/W	0*	PCA9624 does not respond to I²C-bus subaddress 1.
			1	PCA9624 responds to I²C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9624 does not respond to I²C-bus subaddress 2.
			1	PCA9624 responds to I²C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9624 does not respond to I²C-bus subaddress 3.
			1	PCA9624 responds to I²C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9624 does not respond to LED All Call I²C-bus address.
			1*	PCA9624 responds to LED All Call I²C-bus address.

[1] Bit 4 must be programmed with logic 0 for proper device operation.

[2] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[3] No blinking or dimming is possible when the oscillator is off.

7.3.2 Mode register 2, MODE2

Table 7. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	-	read only	0*	reserved
6	-	read only	0*	reserved
5	DMBLNK	R/W	0*	group control = dimming.
			1	group control = blinking.
4	INVRT	R/W	0*	reserved; write must always be a logic 0
3	OCH	R/W	0*	outputs change on STOP command[1]
			1	outputs change on ACK
2	-	R/W	1*	reserved; write must always be a logic 1[2]
1	-	R/W	0*	reserved; write must always be a logic 0[2]
0	-	R/W	1*	reserved; write must always be a logic 1[2]

[1] Change of the outputs at the STOP command allows synchronizing outputs of more than one PCA9624. Applicable to registers from 02h (PWM0) to 08h (LEDOUT) only.

[2] **Remark:** If you change these bits from their default values, the device does not perform as expected.

7.3.3 PWM0 to PWM7, individual brightness control

Table 8. PWM0 to PWM7 - PWM registers 0 to 7 (address 02h to 09h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle

A 97 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (1)$$

7.3.4 GRPPWM, group duty cycle control

Table 9. GRPPWM - Group brightness control register (address 0Ah) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190 Hz fixed frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (2)$$

7.3.5 GRPFREQ, group frequency

Table 10. GRPFREQ - Group Frequency register (address 0Bh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Bh	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{24}(s) \quad (3)$$

7.3.6 LEDOUT0 and LEDOUT1, LED driver output state

Table 11. LEDOUT0 to LEDOUT1 - LED driver output state register (address 0Ch to 0Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	LEDOUT0	7:6	LDR3	R/W	00*	LED3 output state control
		5:4	LDR2	R/W	00*	LED2 output state control
		3:2	LDR1	R/W	00*	LED1 output state control
		1:0	LDR0	R/W	00*	LED0 output state control
0Dh	LEDOUT1	7:6	LDR7	R/W	00*	LED7 output state control
		5:4	LDR6	R/W	00*	LED6 output state control
		3:2	LDR5	R/W	00*	LED5 output state control
		1:0	LDR4	R/W	00*	LED4 output state control

LDRx = 00 — LED driver x is off (default power-up state).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

7.3.7 SUBADR1 to SUBADR3, I²C-bus subaddress 1 to 3

Table 12. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 0 to 3 (address 0Eh to 10h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Eh	SUBADR1	7:1	A1[7:1]	R/W	1110 001*	I²C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
0Fh	SUBADR2	7:1	A2[7:1]	R/W	1110 010*	I²C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
10h	SUBADR3	7:1	A3[7:1]	R/W	1110 100*	I²C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Subaddresses are programmable through the I²C-bus. Default power-up values are E2h, E4h, E8h, and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once subaddresses have been programmed to their right values, SUBx bits must be set to logic 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I²C-bus subaddress are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to logic 1, the corresponding I²C-bus subaddress can be used during either an I²C-bus read or write sequence.

7.3.8 ALLCALLADR, LED All Call I²C-bus address

Table 13. ALLCALLADR - LED All Call I²C-bus address register (address 11h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
11h	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I²C-bus address allows all the PCA9624s on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I²C-bus and can be used during either an I²C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

7.4 Active LOW output enable input

The active LOW output enable ($\overline{OE}$) pin, allows enabling or disabling all the LED outputs at the same time.

- When a LOW level is applied to $\overline{OE}$ pin, all the LED outputs are enabled.
- When a HIGH level is applied to $\overline{OE}$ pin, all the LED outputs are high-impedance.

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9624 devices at the same time. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{OE}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{OE}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it results in an undefined blinking pattern. Do not use $\overline{OE}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it results in an undefined dimming pattern.

Remark: During power-down, slow decay of voltage supplies may keep LEDs illuminated. Consider disabling LED outputs using HIGH level applied to $\overline{OE}$ pin.

7.5 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9624 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9624 registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.6 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.
2. The reserved SWRST I²C-bus address ‘0000 011’ with the R/$\overline{W}$ bit set to ‘0’ (write) is sent by the I²C-bus master.
3. The PCA9624 device(s) acknowledge(s) after seeing the SWRST Call address ‘0000 0110’ (06h) only. If the R/$\overline{W}$ bit is set to ‘1’ (read), no acknowledge is returned to the I²C-bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):
   a. Byte 1 = A5h: the PCA9624 acknowledges this value only. If byte 1 is not equal to A5h, the PCA9624 does not acknowledge it.

b. Byte 2 = 5Ah: the PCA9624 acknowledges this value only. If byte 2 is not equal to 5Ah, then the PCA9624 does not acknowledge it.

If more than 2 bytes of data are sent, the PCA9624 does not acknowledge any more.

5. Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a STOP command to end the SWRST Call: the PCA9624 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

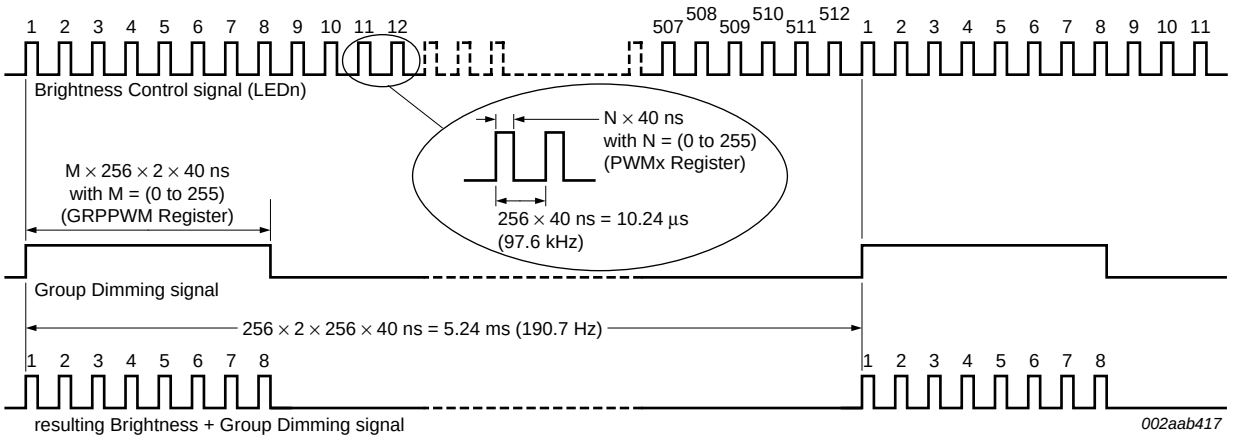
The I²C-bus master must interpret a non-acknowledge from the PCA9624 (at any time) as a 'SWRST Call Abort'. The PCA9624 does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

7.7 Individual brightness control with group dimming/blinking

A 97 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to $^{1}/_{10.73}$ Hz (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 40 ns.

Minimum pulse width for Group Dimming is 20.48 µs.

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal has 2 pulses of the LED Brightness Control signal (pulse width = N × 40 ns, with 'N' defined in PWMx register).

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 4 (8 pulses).

Fig 7. Brightness + Group Dimming signals

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 8).

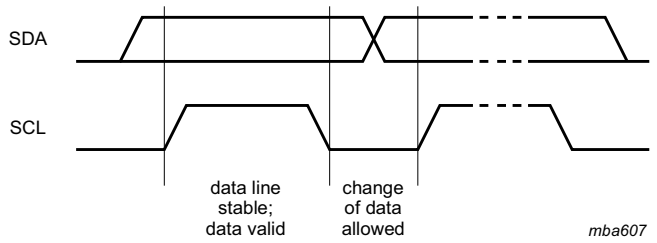


Fig 8. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

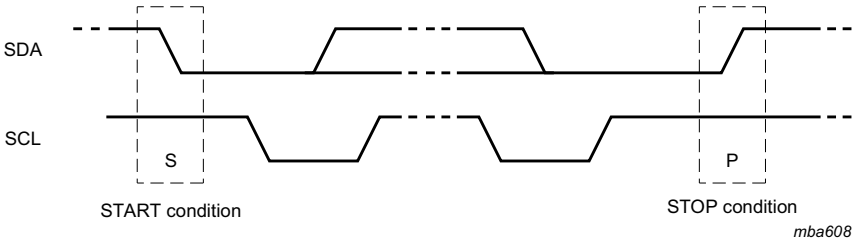


Fig 9. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

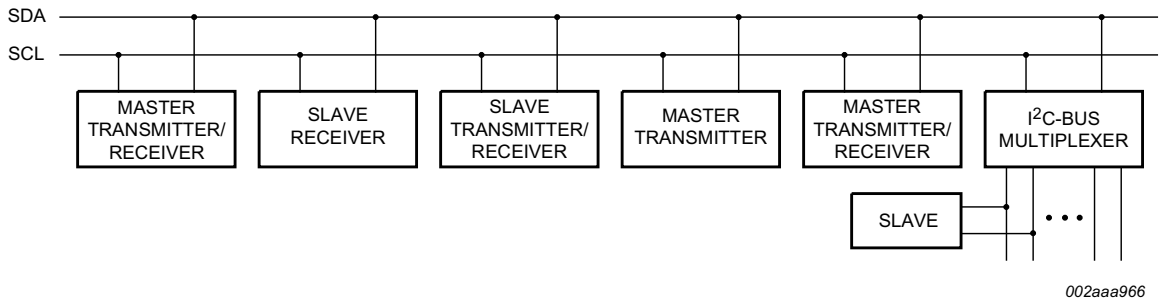


Fig 10. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

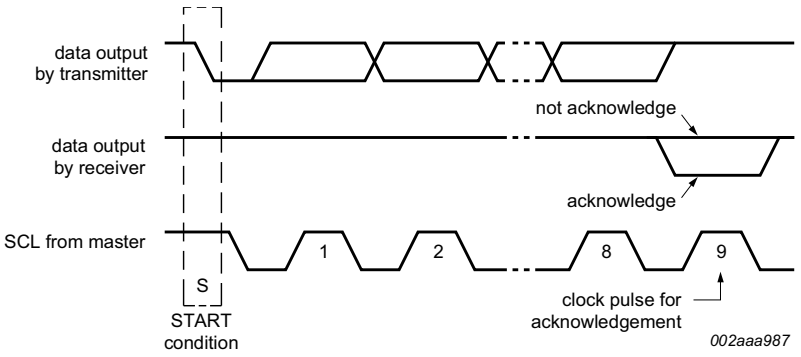
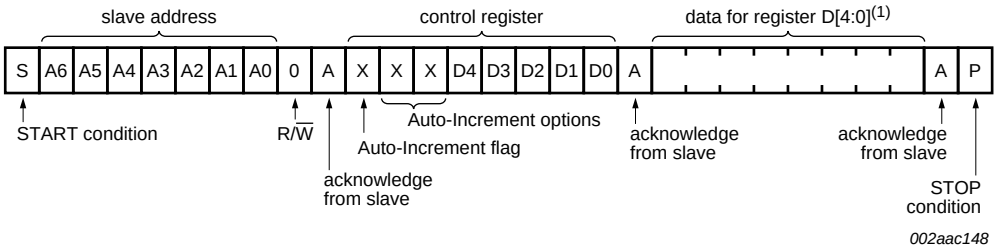


Fig 11. Acknowledgement on the I²C-bus

9. Bus transactions



(1) See Table 5 for register definition.

Fig 12. Write to a specific register

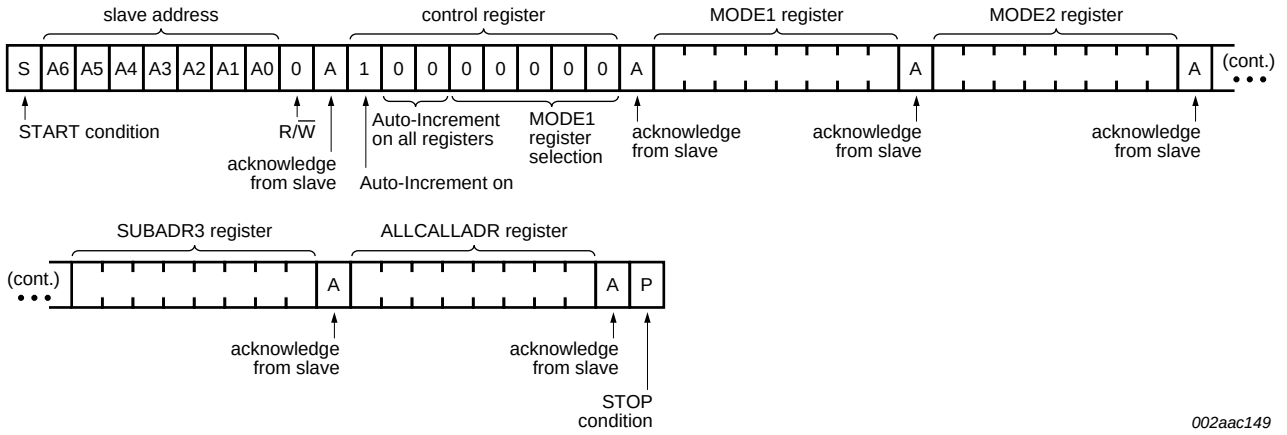


Fig 13. Write to all registers using the Auto-Increment feature

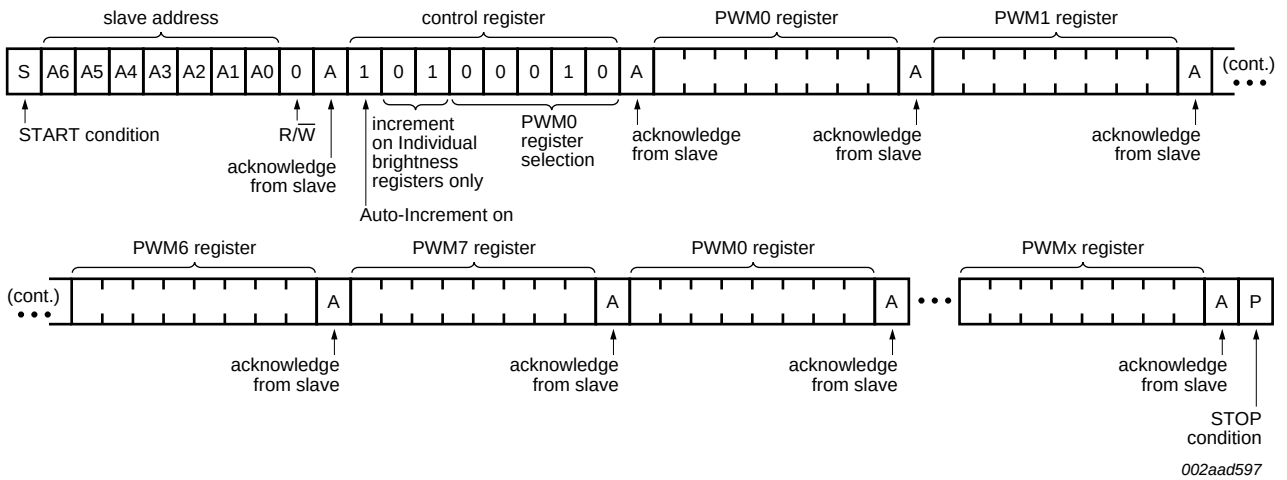


Fig 14. Multiple writes to Individual Brightness registers only using the Auto-Increment feature

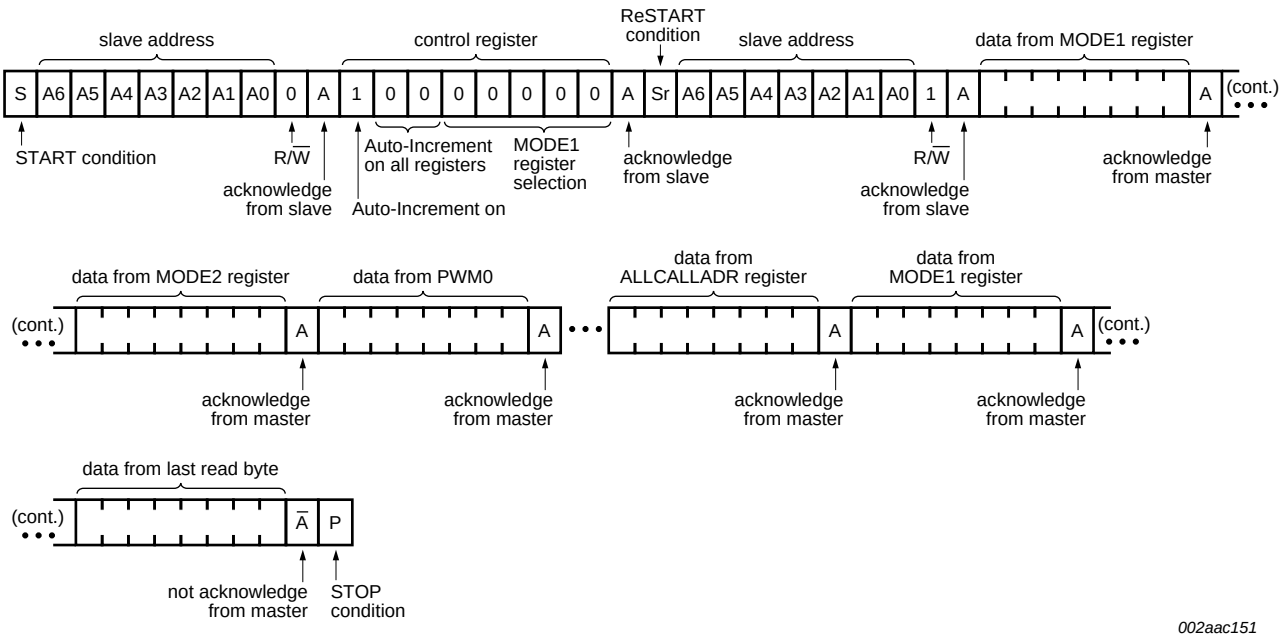
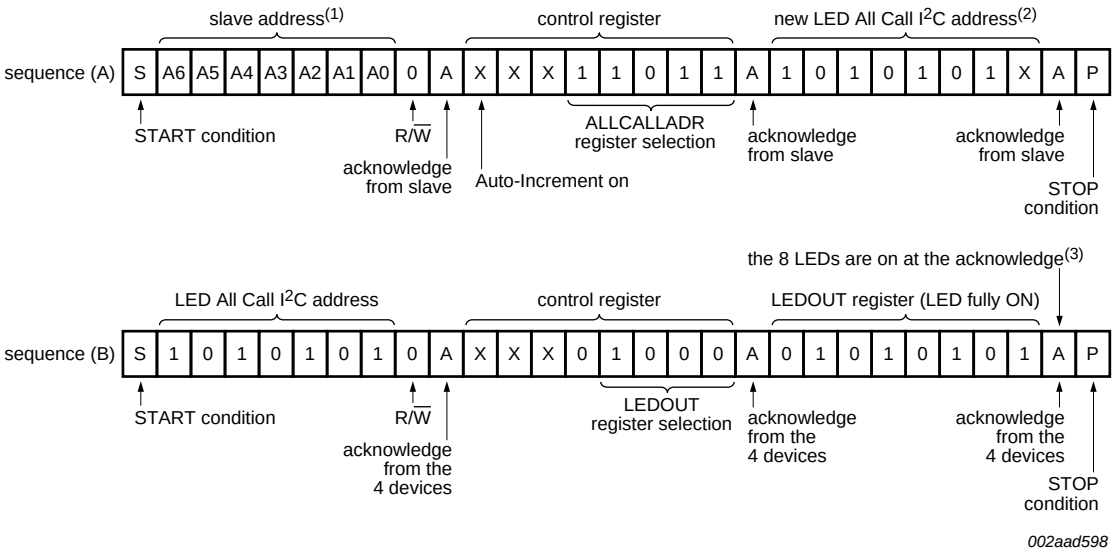


Fig 15. Read all registers using the Auto-Increment feature



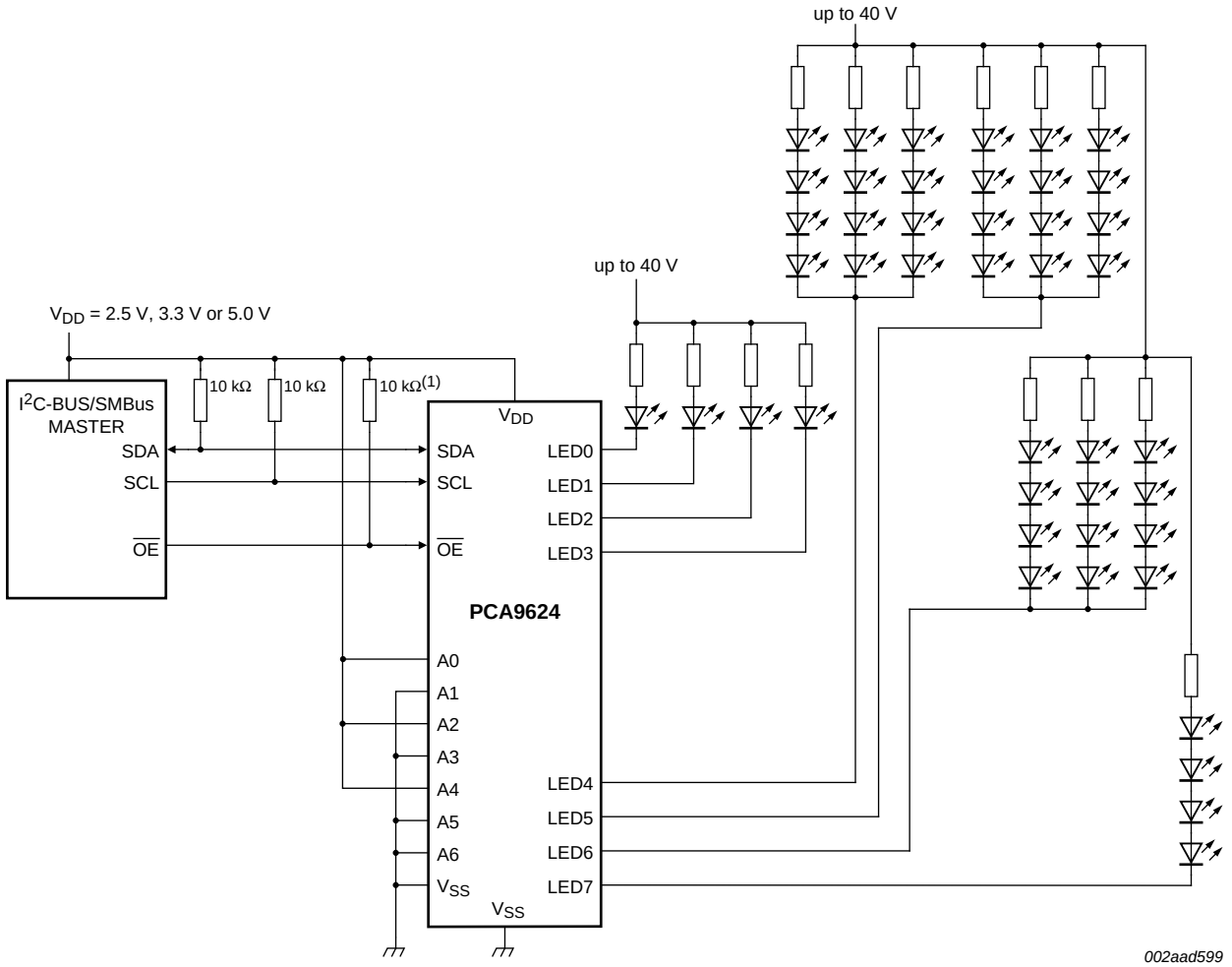
(1) In this example, several PCA9624s are used and the same sequence (A) (above) is sent to each of them.

(2) ALLCALL bit in MODE1 register is equal to 1 for this example.

(3) OCH bit in MODE2 register is equal to 1 for this example.

Fig 16. LED All Call I²C-bus address programming and LED All Call sequence example

10. Application design-in information



(1) $\overline{OE}$ requires pull-up resistor if control signal from the master is open-drain.

I²C-bus address = 0010 101x.

Remark: During power-down, slow decay of voltage supplies may keep LEDs illuminated. Consider disabling LED outputs using HIGH level applied to $\overline{OE}$ pin.

Fig 17. Typical application

10.1 Junction temperature calculation

A device junction temperature can be calculated when the ambient temperature or the case temperature is known.

When the ambient temperature is known, the junction temperature is calculated using Equation 4 and the ambient temperature, junction to ambient thermal resistance and power dissipation.

$$T_j = T_{amb} + R_{th(j\text{-}a)} \times P_{tot} \quad (4)$$

where:

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = junction to ambient thermal resistance

P_{tot} = (device) total power dissipation

When the case temperature is known, the junction temperature is calculated using Equation 5 and the case temperature, junction to case thermal resistance and power dissipation.

$$T_j = T_{case} + R_{th(j\text{-}c)} \times P_{tot} \quad (5)$$

where:

T_j = junction temperature

T_{case} = case temperature

$R_{th(j\text{-}c)}$ = junction to case thermal resistance

P_{tot} = (device) total power dissipation

Here are two examples regarding how to calculate the junction temperature using junction to case and junction to ambient thermal resistance. In the first example (Section 10.1.1), given the operating condition and the junction to ambient thermal resistance, the junction temperature of PCA9624PW, in the TSSOP24 package, is calculated for a system operating condition in 50 °C[1] ambient temperature. In the second example (Section 10.1.2), based on a specific customer application requirement where only the case temperature is known, applying the junction to case thermal resistance equation, the junction temperature of the PCA9624PW, in the TSSOP24 package, is calculated.

1. 50 °C is a typical temperature inside an enclosed system. The designers should feel free, as needed, to perform their own calculation using the examples.

10.1.1 Example 1: T_j calculation of PCA9624DR, in TSSOP24 package, when T_{amb} is known

$R_{th(j-a)}$ = 108 °C/W

T_{amb} = 50 °C

LED output low voltage (LED V_{OL}) = 0.5 V

LED output current per channel = 80 mA

Number of outputs = 8

$I_{DD(max)}$ = 10 mA

$V_{DD(max)}$ = 5.5 V

I²C-bus clock (SCL) maximum sink current = 25 mA

I²C-bus data (SDA) maximum sink current = 25 mA

1. Find P_{tot} (device total power dissipation):
   - output total power = 80 mA × 8 × 0.5 V = 320 mW
   - chip core power consumption = 10 mA × 5.5 V = 55 mW
   - SCL power dissipation = 25 mA 0.4 V = 10 mW
   - SDA power dissipation = 25 mA 0.4 V = 10 mW

   P_{tot} = (320 + 55 + 10 + 10) mW = **395 mW**
2. Find T_j (junction temperature):

   $T_j = (T_{amb} + R_{th(j-a)} \times P_{tot})$ = (50 °C + 108 °C/W × 395 mW) = **92.7 °C**

10.1.2 Example 2: T_j calculation where only T_{case} is known

This example uses a customer's specific application of the PCA9624PW, 8-channel LED controller in the TSSOP24 package, where only the case temperature (T_{case}) is known.

$T_j = T_{case} + R_{th(j-c)} \times P_{tot}$, where:

$R_{th(j-c)}$ = 30 °C/W

T_{case} (measured) = 94.6 °C

V_{OL} of LED ~ 0.5 V

$I_{DD(max)}$ = 10 mA

$V_{DD(max)}$ = 5.5 V

LED output voltage LOW = 0.5 V

LED output current:

60 mA on 1 port = (60 mA × 1)

50 mA on 6 ports = (50 mA × 6)

40 mA on 1 port = (40 mA × 1)

I²C-bus maximum sink current on clock line = 25 mA

I²C-bus maximum sink current on data line = 25 mA

1. Find P_{tot} (device total power dissipation)
   - output current (60 mA × 1 port); output power (60 mA × 1 × 0.5 V) = 30 mW
   - output current (50 mA × 6 ports); output power (50 mA × 6 × 0.5 V) = 150 mW
   - output current (40 mA × 1 port); output power (40 mA × 1 × 0.5 V) = 20 mW

   Output total power = **200 mW**
   - chip core power consumption = 10 mA × 5.5 V = 55 mW
   - SCL power dissipation = 25 mA × 0.4 V = 10 mW
   - SDA power dissipation = 25 mA × 0.4 V = 10 mW

   P_{tot} (device total power dissipation) = **275 mW**
2. Find T_j (junction temperature):

   $T_j = T_{case} + R_{th(j-a)} \times P_{tot}$ = 94.6 °C + 30 °C/W × 275 mW = **102.85 °C**

11. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} – 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage		V_{SS} – 0.5	40	V
$I_{O(LEDn)}$	output current on pin LEDn		-	100	mA
$I_{OL(tot)}$	total LOW-level output current	LED driver outputs; V_{OL} = 0.5 V [1]	800	-	mA
I_{SS}	ground supply current	per V_{SS} pin	-	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	1.8	W
		T_{amb} = 85 °C	-	0.72	W
P/ch	power dissipation per channel	T_{amb} = 25 °C	-	100	mW
		T_{amb} = 85 °C	-	45	mW
T_j	junction temperature	[2]	-	+125	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] Each bit must be limited to a maximum of 100 mA and the total package limited to 800 mA due to internal busing limits. The pull-up (current limiting) resistor must be of sufficient size (W) and value (Ω) to guarantee that the 100 mA limit is not exceeded on any output.

[2] Refer to Section 10.1 for calculation.

Table 15. TSSOP24 versus HVQFN24 power dissipation and output current capability

Measurement	TSSOP24	HVQFN24
T_{amb} = 25 °C		
maximum power dissipation (chip + output drivers)	926 mW	2220 mW
maximum power dissipation (output drivers only)	851 mW	2150 mW
maximum drive current per channel	$< \frac{851\ mW}{8\text{-}bit \times 0.5\ V} = 212.75\ mA$ [1]	$< \frac{2150\ mW}{8\text{-}bit \times 0.5\ V} = 537.5\ mA$ [1]
T_{amb} = 60 °C		
maximum power dissipation (chip + output drivers)	602 mW	1440 mW
maximum power dissipation (output drivers only)	527 mW	1365 mW
maximum drive current per channel	$< \frac{527\ mW}{8\text{-}bit \times 0.5\ V} = 131.8\ mA$ [1]	$< \frac{1365\ mW}{8\text{-}bit \times 0.5\ V} = 341.25\ mA$ [1]
T_{amb} = 80 °C		
maximum power dissipation (chip + output drivers)	417 mW	1000 mW
maximum power dissipation (output drivers only)	342 mW	925 mW
maximum drive current per channel	$< \frac{342\ mW}{8\text{-}bit \times 0.5\ V} = 85.5\ mA$	$< \frac{925\ mW}{8\text{-}bit \times 0.5\ V} = 231.3\ mA$ [1]

[1] This value signifies package's ability to handle more than 100 mA per output driver. The device's maximum current rating per output is 100 mA.

12. Thermal characteristics

Table 16. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	TSSOP24	[1]	108	°C/W
		HVQFN24	[1]	45	°C/W
$R_{th(j\text{-}c)}$	thermal resistance from junction to case	TSSOP24	[1]	30	°C/W
		HVQFN24	[1]	19.6	°C/W

[1] Calculated in accordance with JESD 51-7.

13. Static characteristics

Table 17. Static characteristics

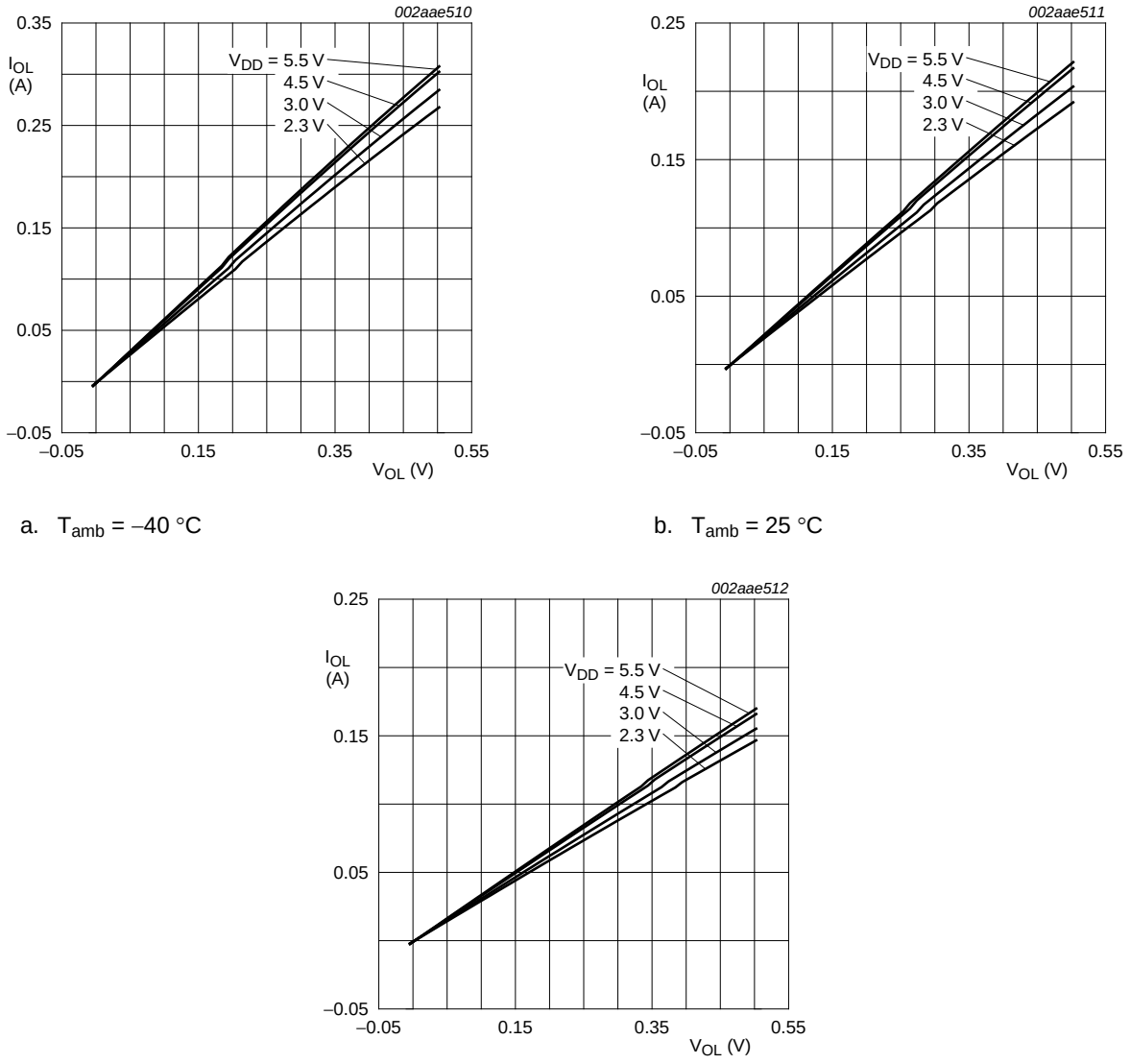
V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	5.5	V
I_{DD}	supply current	on pin V_{DD}; operating mode; no load; f_{SCL} = 1 MHz				
		V_{DD} = 2.7 V	-	0.15	4	mA
		V_{DD} = 3.6 V	-	0.4	6	mA
		V_{DD} = 5.5 V	-	2.0	10	mA
I_{stb}	standby current	on pin V_{DD}; no load; f_{SCL} = 0 Hz; I/O = inputs; $V_I = V_{DD}$				
		V_{DD} = 2.7 V	-	0.3	5	µA
		V_{DD} = 3.6 V	-	0.6	6	µA
		V_{DD} = 5.5 V	-	2.1	7	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS} [1]	-	1.70	2.0	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V	20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V	30	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	6	10	pF
LED driver outputs						
I_{OL}	LOW-level output current	V_{OL} = 0.5 V [2]	100	-	-	mA
I_{LOH}	HIGH-level output leakage current	$V_{drv(LED)}$ = 5 V	-	-	±1	µA
		$V_{drv(LED)}$ = 40 V	-	±1	15	µA
R_{on}	ON-state resistance	$V_{drv(LED)}$ = 40 V; V_{DD} = 2.3 V	-	2	5	Ω
C_o	output capacitance	[3]	-	15	40	pF
OE input						
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.7	5	pF
Address inputs						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.7	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each bit must be limited to a maximum of 100 mA and the total package limited to 800 mA due to internal busing limits.

[3] Tested with outputs off.



a. T_{amb} = −40 °C

b. T_{amb} = 25 °C

c. T_{amb} = 85 °C

Fig 18. V_{OL} versus I_{OL}

14. Dynamic characteristics

Table 18. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[2]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[3][4]	-	300	$20 + 0.1C_b$[5]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[5]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	-	50	ns
Output propagation delay									
t_{PLH}	LOW to HIGH propagation delay	$\overline{OE}$ to LEDn; MODE2[1:0] = 01	-	-	-	-	-	150	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{OE}$ to LEDn; MODE2[1:0] = 01	-	-	-	-	-	150	ns
Output port timing									
$t_{d(SCL-Q)}$	delay time from SCL to data output	SCL to LEDn; MODE2[3] = 1; outputs change on ACK	-	-	-	-	-	450	ns
$t_{d(SDA-Q)}$	delay time from SDA to data output	SDA to LEDn; MODE2[3] = 0; outputs change on STOP condition	-	-	-	-	-	450	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] C_b = total capacitance of one bus line in pF.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

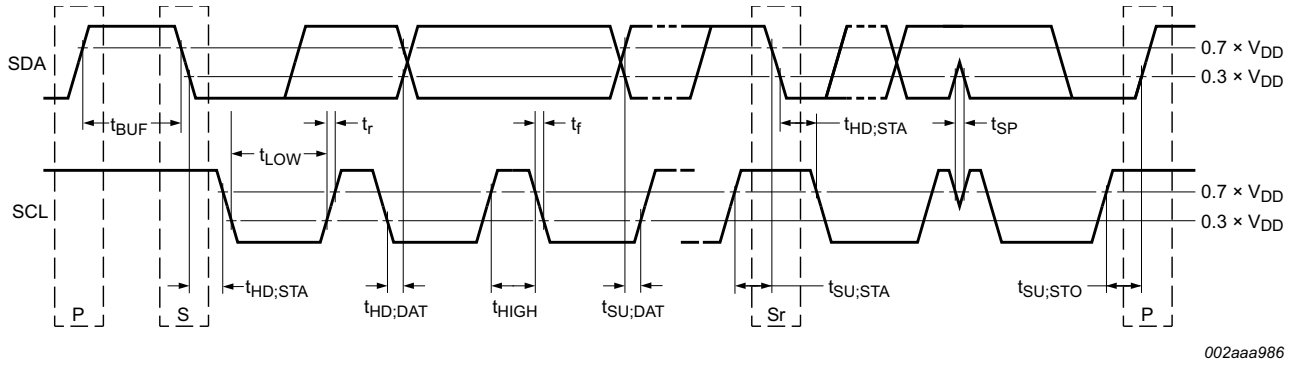
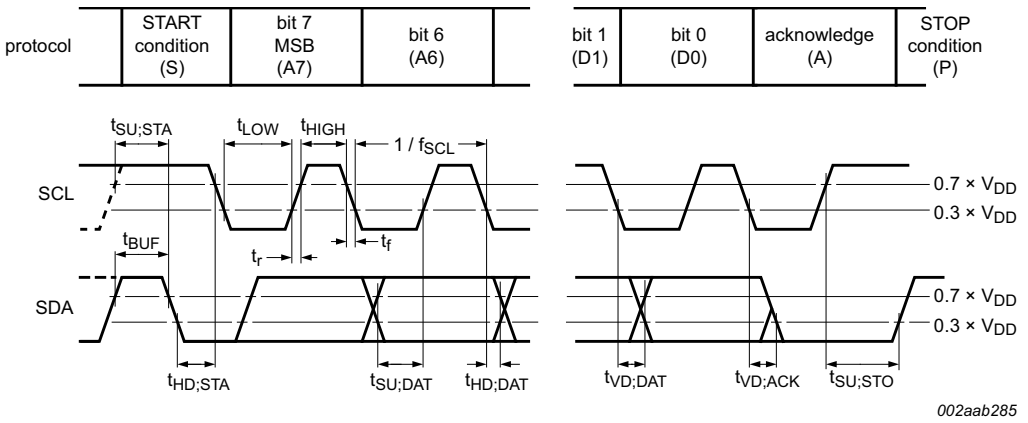


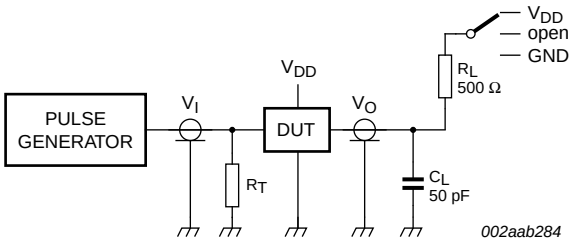
Fig 19. Definition of timing



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 20. I²C-bus timing diagram

15. Test information



R_L = Load resistor for LEDn. R_L for SDA and SCL > 1 kΩ (3 mA or less current).

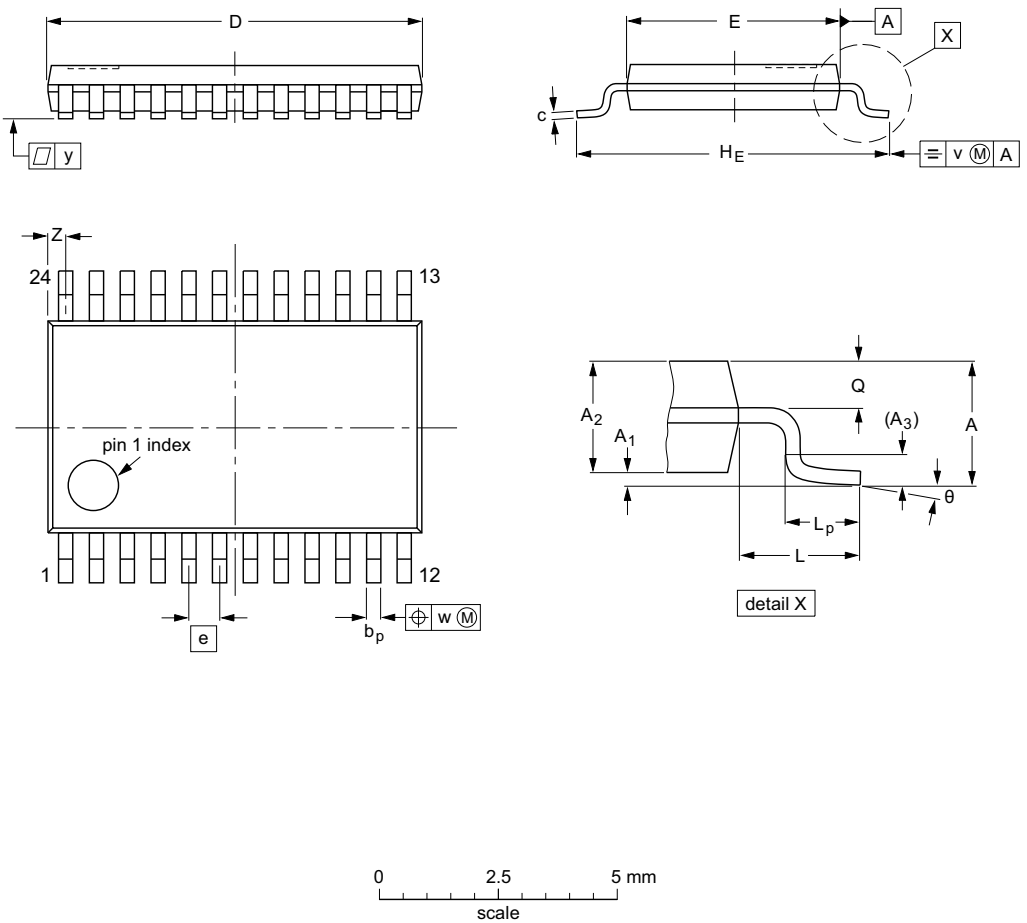
C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 21. Test circuitry for switching times

16. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

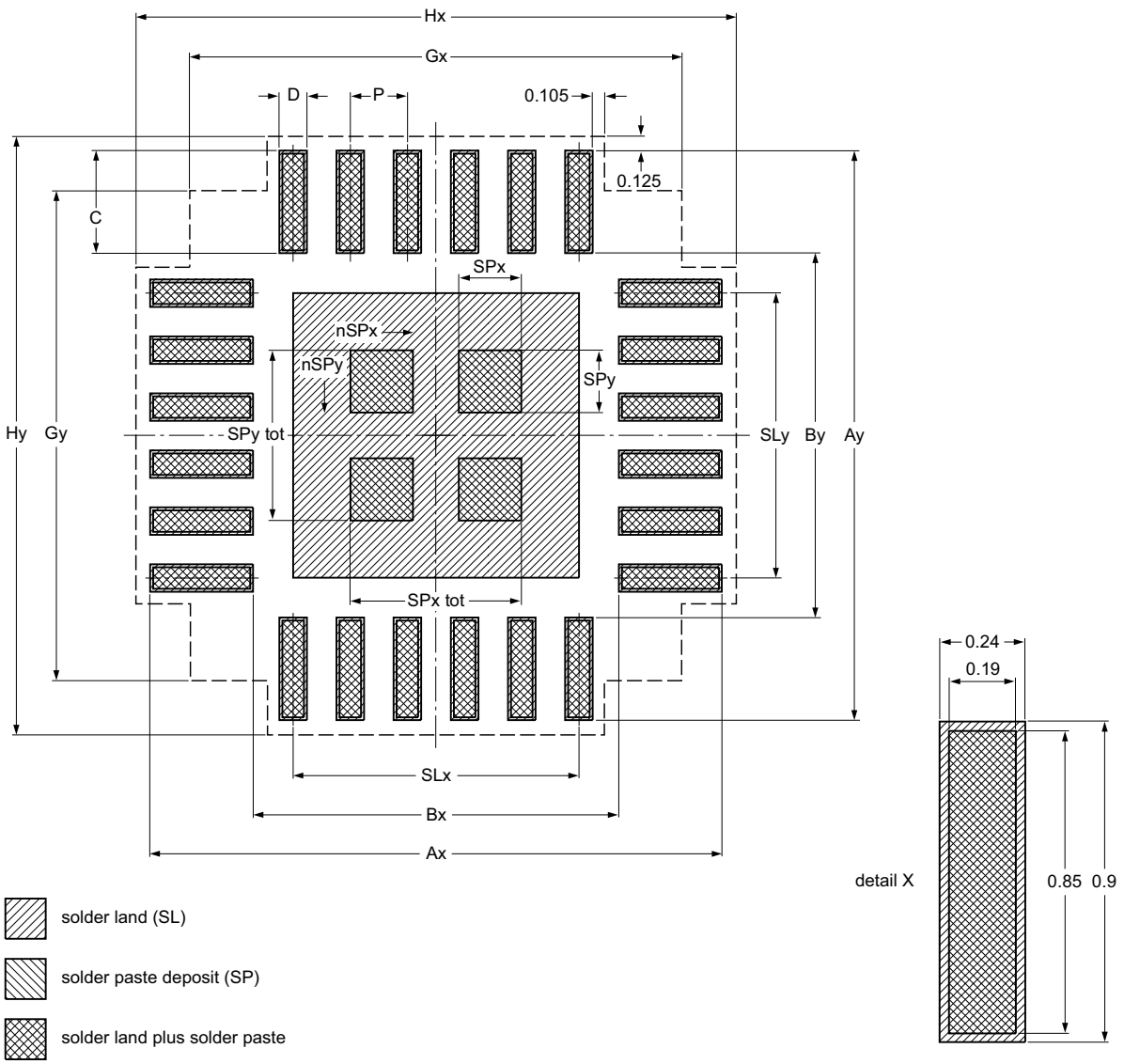
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT355-1 (TSSOP24)

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Hx	Hy
5.25	5.25

Dimensions in mm

P	Ax	Ay	Bx	By	SLx	SLy	SPx	SPy	SPx tot	SPy tot	C	D	nSPx	nSPy	Gx	Gy
0.50	5.00	5.00	3.20	3.20	2.50	2.50	0.55	0.55	1.50	1.50	0.90	0.24	2	2	4.30	4.30

Issue date ~~09-06-15~~ 14-06-12 *sot616-3_fr*

Fig 23. Package outline SOT616-3 (HVQFN24)

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19 and 20

Table 19. SnPb eutectic process (from J-STD-020D)

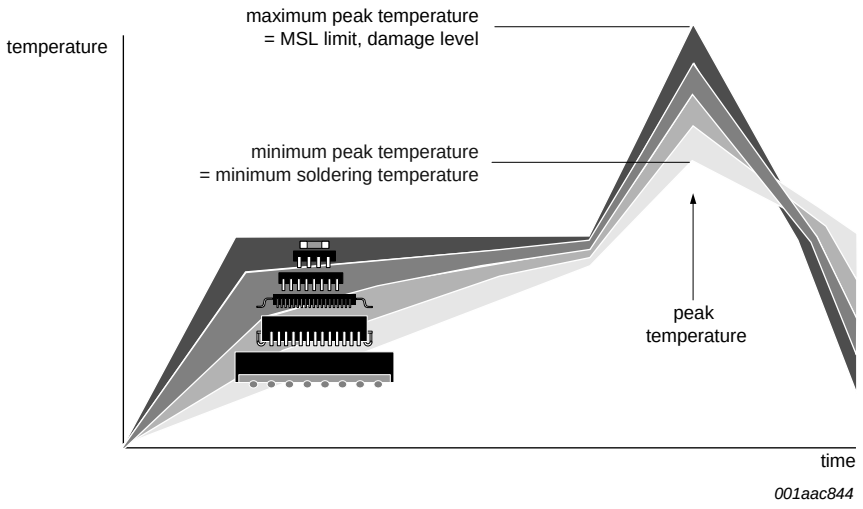
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 20. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



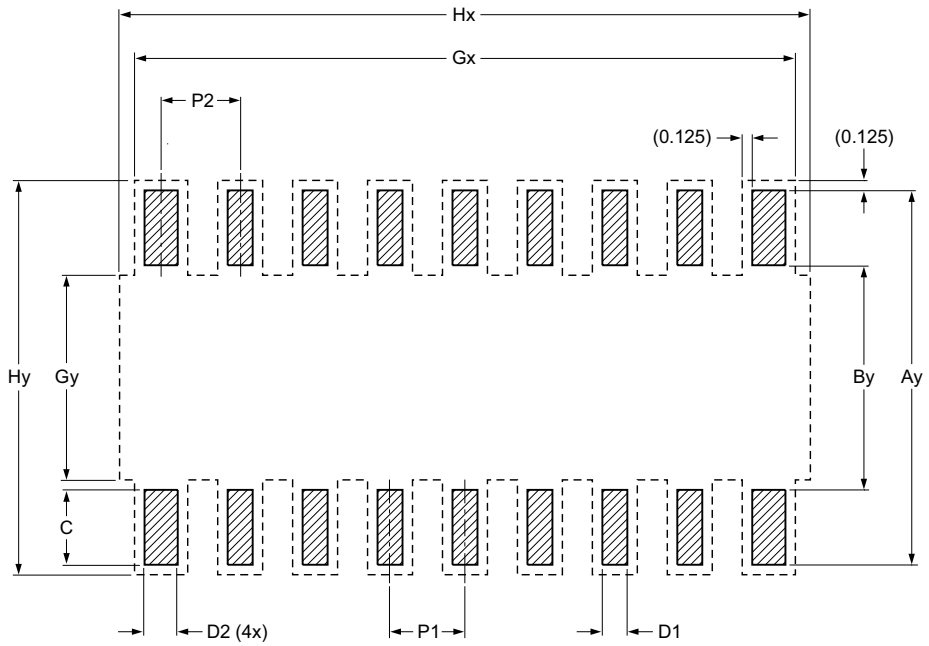
MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP24 package **SOT355-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

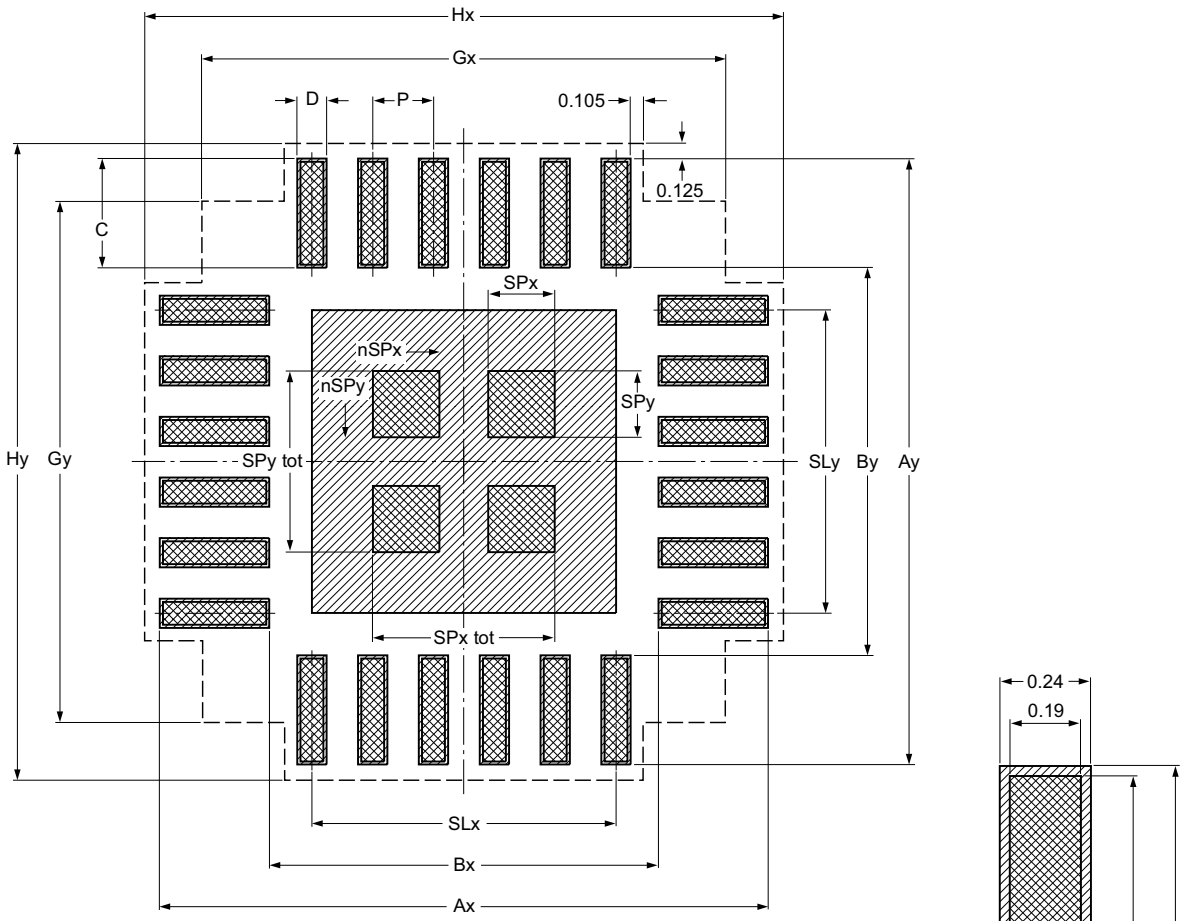
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1_fr

Fig 25. PCB footprint for SOT355-1 (TSSOP24); reflow soldering

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Hx	Hy
5.25	5.25

Dimensions in mm

P	Ax	Ay	Bx	By	SLx	SLy	SPx	SPy	SPx tot	SPy tot	C	D	nSPx	nSPy	Gx	Gy
0.50	5.00	5.00	3.20	3.20	2.50	2.50	0.55	0.55	1.50	1.50	0.90	0.24	2	2	4.30	4.30

Issue date ~~09-06-15~~ 14-06-12 *sot616-3_fr*

Fig 26. PCB footprint for SOT616-3 (HVQFN24); reflow soldering

20. Abbreviations

Table 21. Abbreviations

Acronym	Description
CDM	Charged-Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
NPN	bipolar transistor with N-type emitter and collector and a P-type base
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
PNP	bipolar transistor with P-type emitter and collector and an N-type base
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

21. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9624 v.4.1	20160118	Product data sheet	-	PCA9624 v.4
Modifications:	• Table 3 “Pin description”: corrected description for LED4 to LED7			
PCA9624 v.4	20140603	Product data sheet	-	PCA9624 v.3
Modifications:	• Added Section 4.1 “Ordering options” • Table 5 “Register summary[1]”: deleted (old) Table note [2] • Table 6 “MODE1 - Mode register 1 (address 00h) bit description”: added (new) Table note [1] and its cross-reference at SLEEP bit (bit 4) • Added Section 19 “Soldering: PCB footprints”			
PCA9624 v.3	20120906	Product data sheet	-	PCA9624 v.2
PCA9624 v.2	20090826	Product data sheet	-	PCA9624 v.1
PCA9624 v.1	20090603	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

22.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

22.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

22.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

23. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

24. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 18 January 2016
Document identifier: PCA9624

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

PCA9624PW,112 PCA9624PW,118 PCA9624BS,118