Low Skew, ÷1/÷2 Differential-to-3.3V LVPECL Clock Generator

8737-11

DATASHEET

General Description

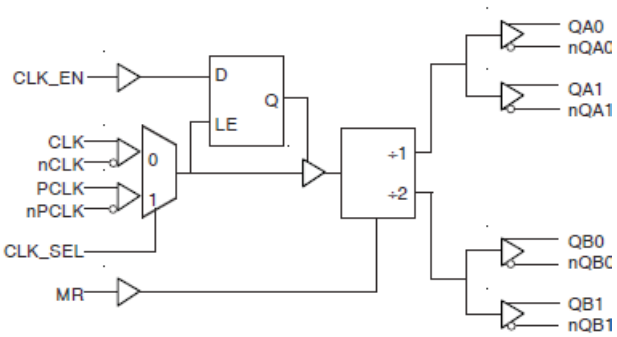
The 8737-11 is a low skew, high performance Differential-to-3.3V LVPECL Clock Generator/Divider. The 8737-11 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels.The clock enable isinternally synchronized to eliminate runt pulses on theoutputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8737-11 ideal for clock distribution applications demanding well defined performance and repeatability.

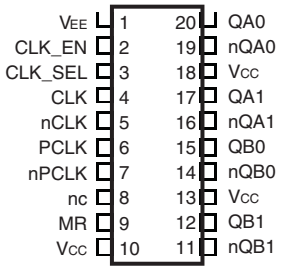
Features

- 2 divide by 1 differential 3.3V LVPECL outputs; 2 divide by 2 differential 3.3V LVPECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Output skew: 60ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Bank skew: Bank A - 20ps (maximum), Bank B - 35ps (maximum)
- Additive phase jitter, RMS: 0.04ps (typical)
- Propagation delay: 1.7ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package RoHS compliant

Block Diagram



Pin Assignment



8737-11
20-Lead TSSOP
6.50mm x 4.40mm x 0.92 package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin.
2	CLK_EN	Power	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock Select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8	nc	Unused		No connect.
9	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs QXx to go low and the inverted outputs nQXx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
10, 13, 18	V_{CC}	Power		Positive supply pins.
11, 12	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
14, 15	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
16, 17	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
19, 20	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs			
MR	CLK_EN	CLK_SEL	Selected Source	QA0, QA1	nQA0, nQA1	QB0, QB1	nQB0, nQB1
1	X	X	X	LOW	HIGH	LOW	HIGH
0	0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW	Disabled; HIGH
0	0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW	Disabled; HIGH
0	1	0	CLK, nCLK	Enabled	Enabled	Enabled	Enabled
0	1	1	PCLK, nPCLK	Enabled	Enabled	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown if Figure 1.
In the active mode, the state of the outputs are a function of the CLK , nCLK and PCLK, nPCLK inputs as described in Table 3B.

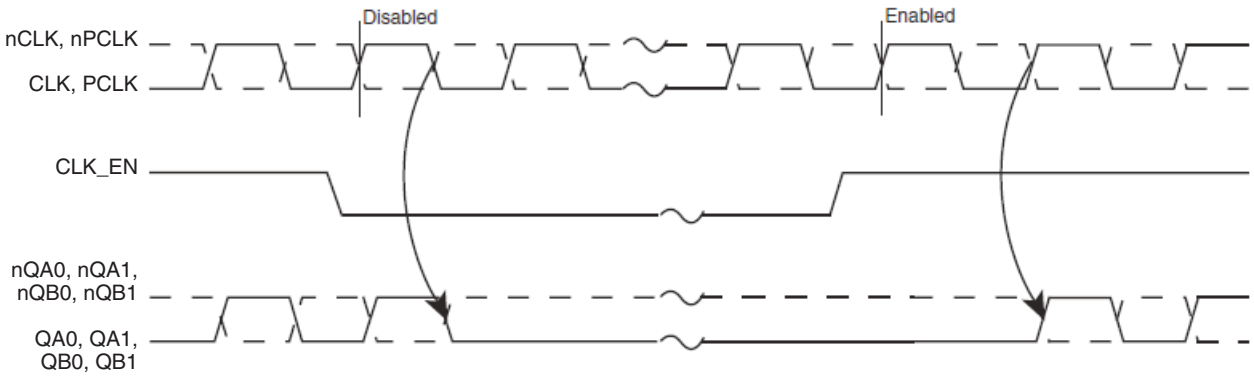


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs				Input to Output Mode	Polarity
CLK or PCLK	nCLK or nPCLK	QAx	nQAx	QBx	nQBx		
0	0	LOW	HIGH	LOW	HIGH	Differential to Differential	Non Inverting
1	1	HIGH	LOW	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	CLK_EN, CLK_SEL, MR			2		3.765	V
V_{IL}	CLK_EN, CLK_SEL, MR			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	V_{IN} = V_{CC} = 3.465V			5	µA
		CLK_SEL, MR	V_{IN} = V_{CC} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
		CLK_SEL,MR	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA

Table 4C. Differential DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{IN} = V_{CC} = 3.465V			5	µA
		CLK	V_{IN} = V_{CC} = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
		CLK	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ = 3.465V			150	µA
		$V_{IN} = V_{CC}$ = 3.465V			5	µA
I_{IL}	Input Low Current	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage		0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		V_{EE} + 1.5		V_{CC}	V
V_{OH}	Output High Voltage; NOTE 3		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 3		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.65		1.0	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V.

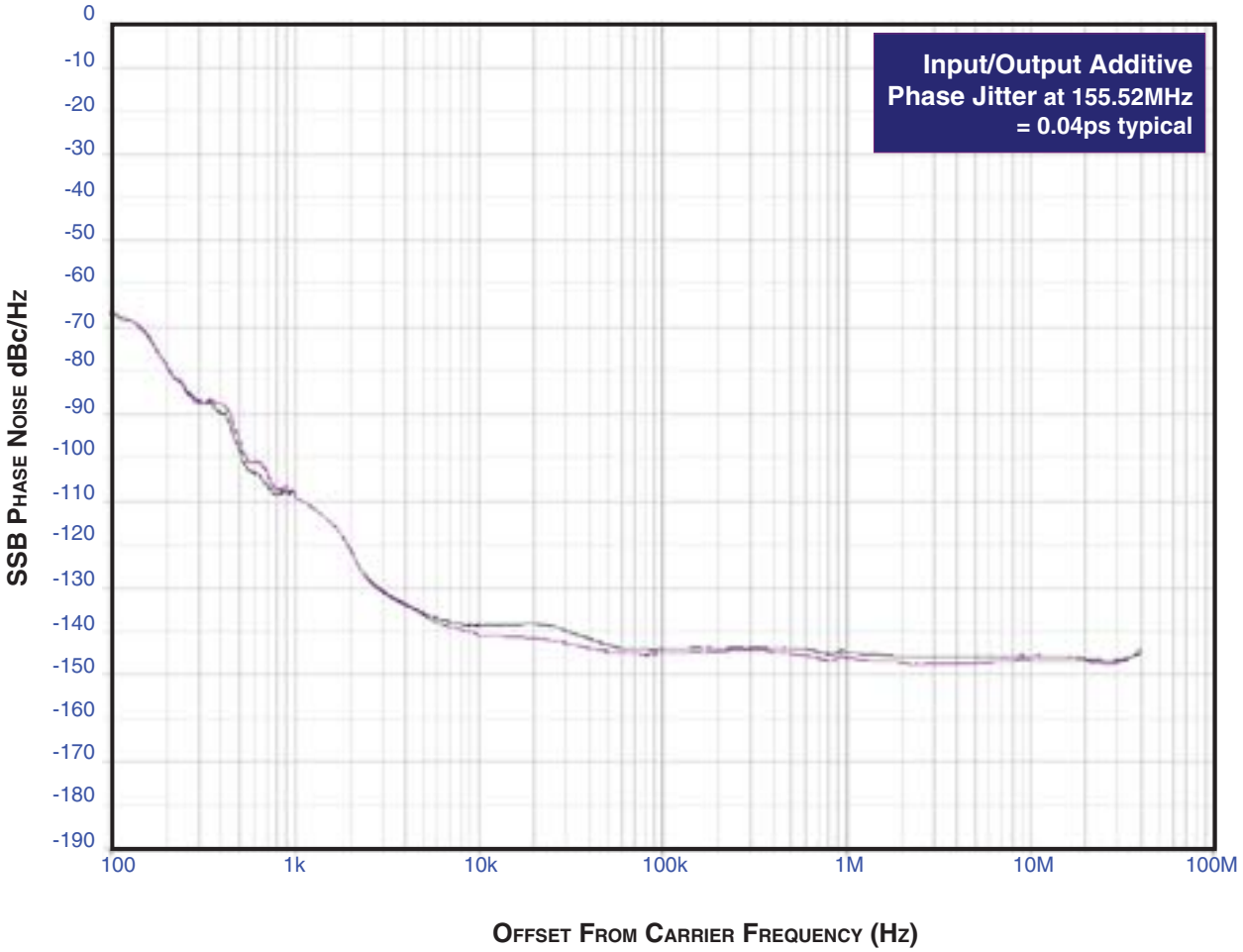
TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					650	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK, nCLK	$f \leq$ 650MHz	1.3		1.7	ns
		PCLK, nPCLK		1.2		1.6	ns
tsk(o)	Output Skew; NOTE 2, 4					60	ps
tsk(b)	Bank Skew; NOTE 4	Bank A				20	ps
		Bank B				35	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4					200	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 5				0.04		ps
t_R	Output Rise Time		20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time		20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle			48	50	52	%

All parameters measured at 500MHz unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Driving only one input clock.

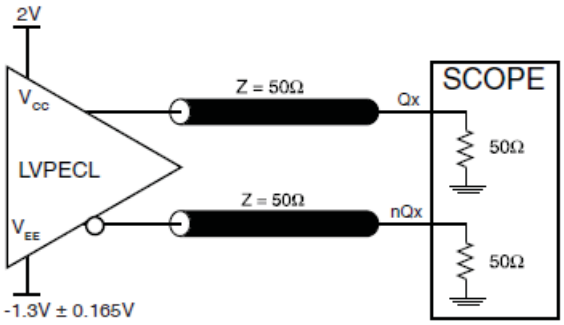
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

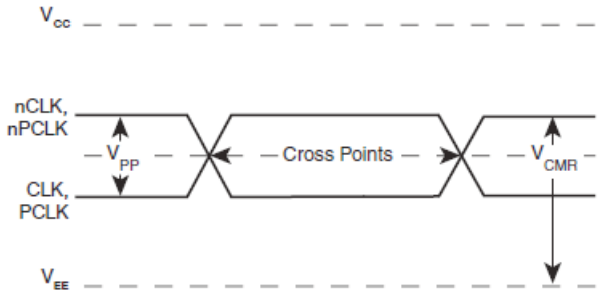


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

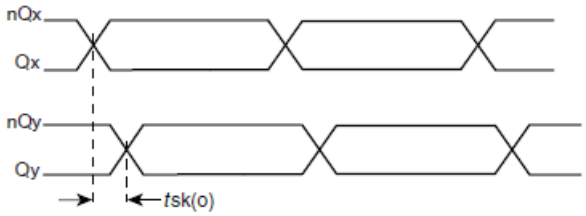
Parameter Measurement Information



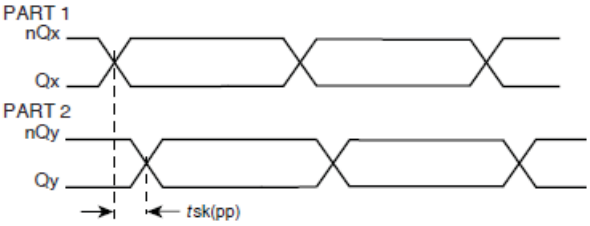
3.3V Output Load AC Test Circuit



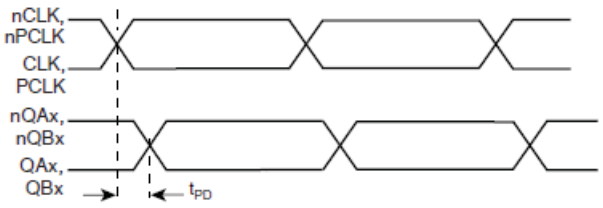
Differential Input Level



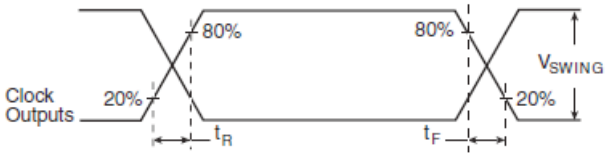
Output Skew



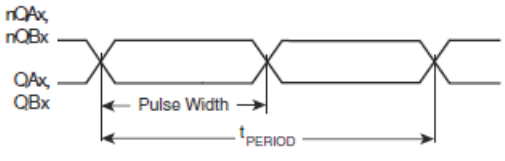
Part-to-Part Skew



Propagation Delay



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ≃ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

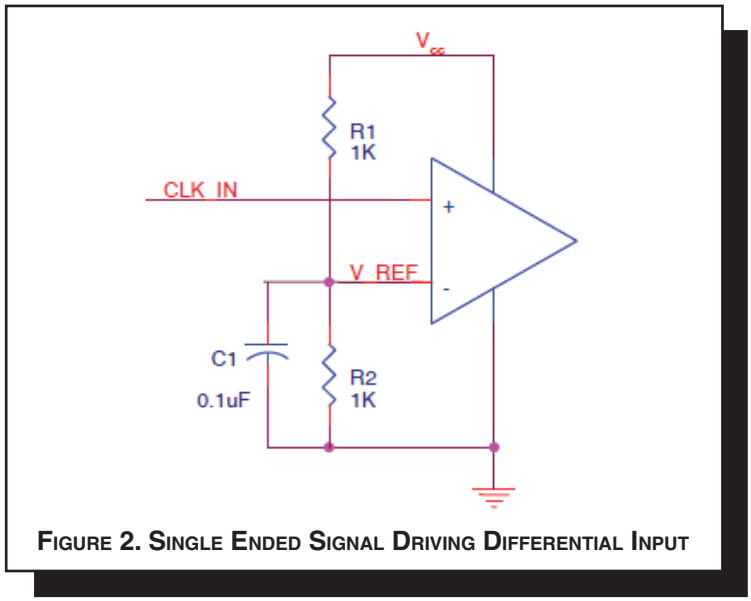


Figure 2. Single Ended Signal Driving Differential Input

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

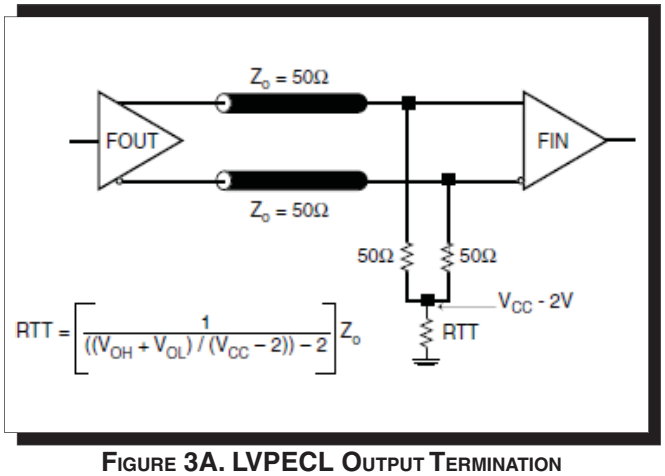


Figure 3A. LVPECL Output Termination

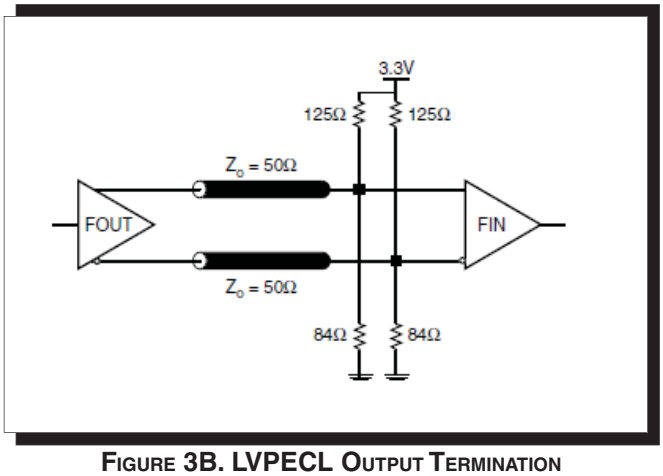


Figure 3B. LVPECL Output Termination

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

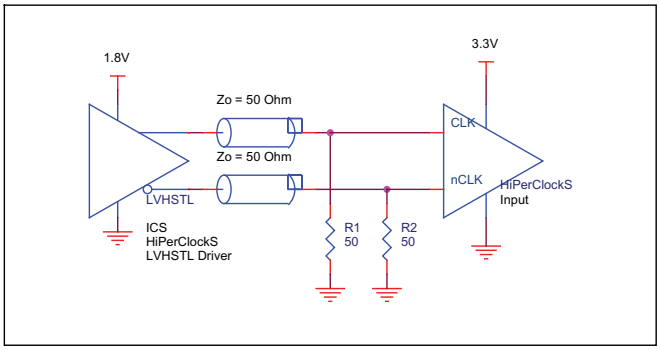


Figure 4A. CLK/nCLK Input Driven by LVHSTL Driver

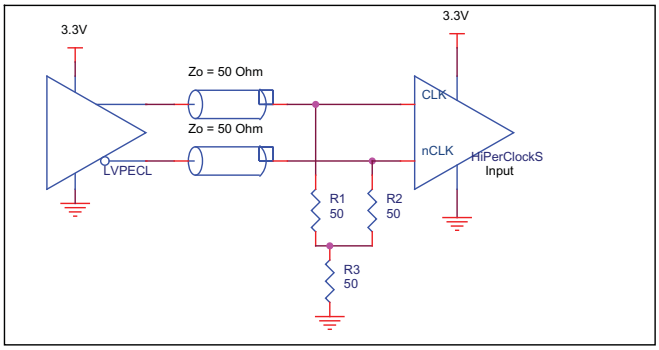


Figure 4B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

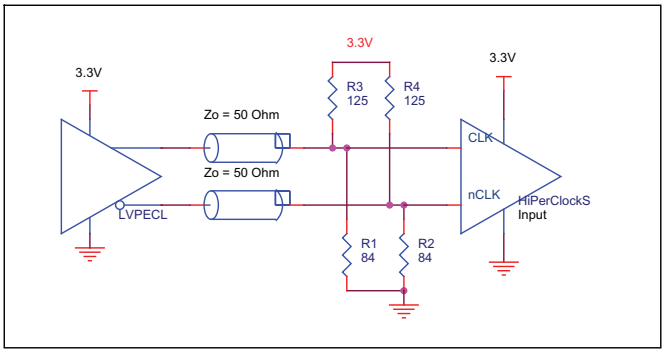


Figure 4C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

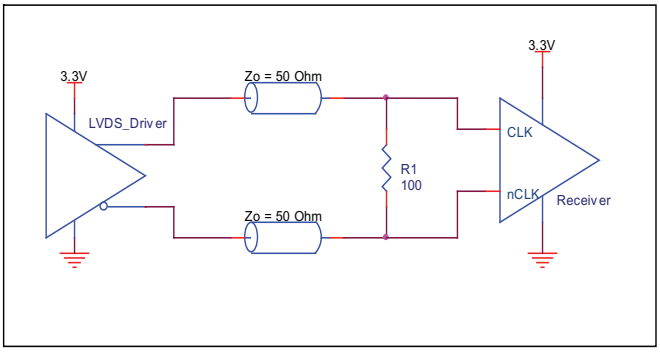


Figure 4D. CLK/nCLK Input Driven by 3.3V LVDS Driver

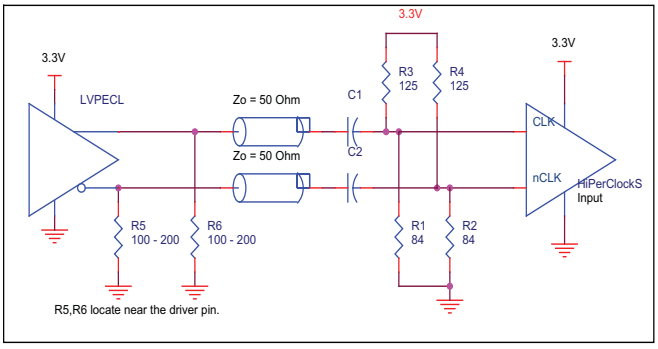


Figure 4E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

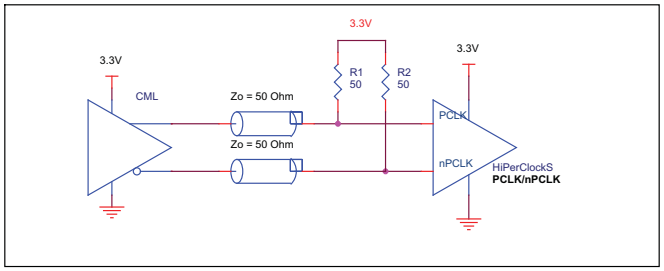


Figure 5A. PCLK/nPCLK Input Driven by a CML Driver

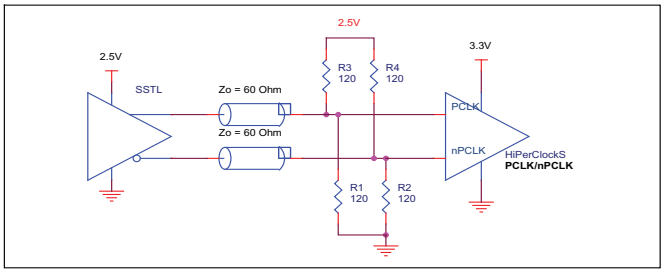


Figure 5B. PCLK/nPCLK Input Driven by an SSTL Driver

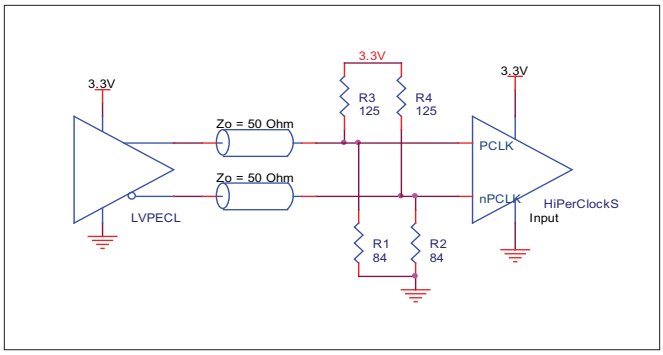


Figure 5C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

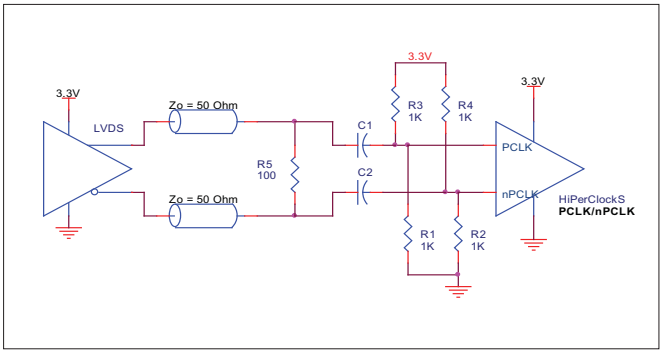


Figure 5D. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

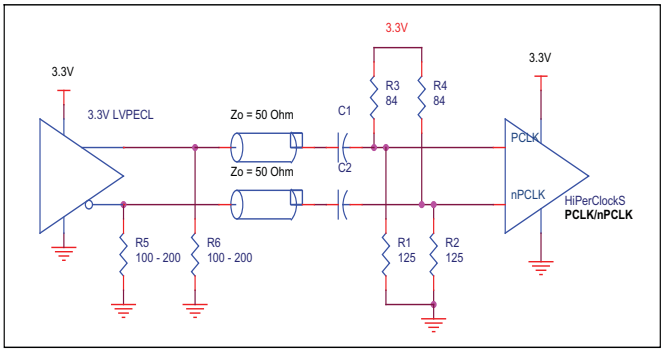


Figure 5E. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8737-11.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 8737-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{CC_MAX} = 3.465V * 50mA = **173.25mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 173.25mW + 120mW = **293.25mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.293W * 66.6°C/W = 89.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 6.*

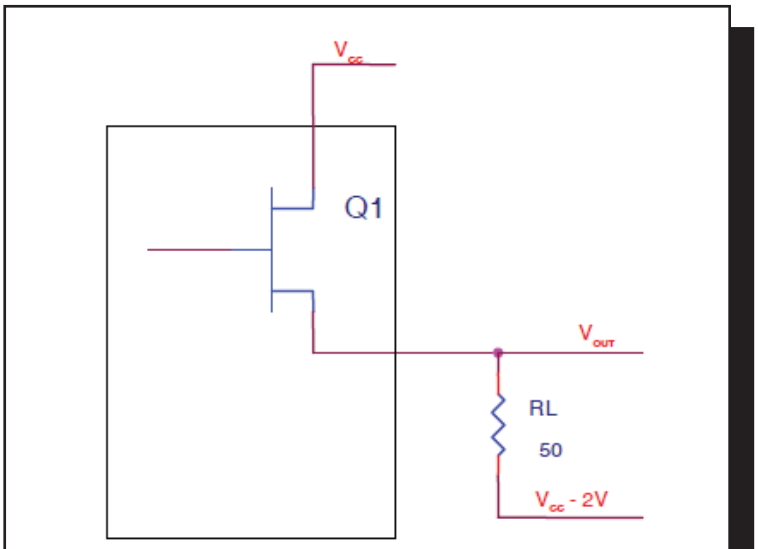


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **$V_{CC\_MAX} – 0.9V$**

  $(V_{CC\_MAX} - V_{OH\_MAX}) =$ **0.9V**

- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **$V_{CC\_MAX} – 1.7V$**

  $(V_{CC\_MAX} - V_{OL\_MAX}) =$ **1.7V**

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 20 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8737-11 is: 510

Package Outline - G Suffix for 20 Lead TSSOP

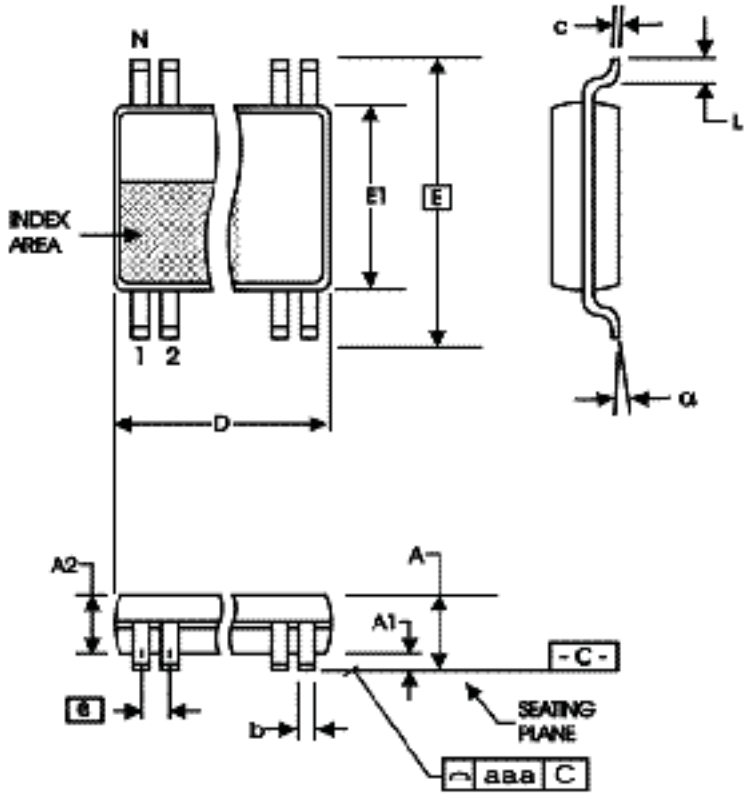


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8737AG-11LF	ICS8737AG11L	20 lead “Lead-Free” TSSOP	tube	0°C to 70°C
8737AG-11LFT	ICS8737AG11L	20 lead “Lead-Free” TSSOP	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		3	Updated Figure 1, CLK_EN Timing Diagram.	10/17/01
A		3	Revised Figure 1, CLK_EN Timing Diagram.	10/31/01
A		8	Added Termination for LVPECL Outputs section.	6/3/02
A	1	2 6 7	Pin Description Table - revised MR description. 3.3V Output Load Test Circuit Diagram, revised VEE equation from "-1.3V ± 0.135V" to " -1.3V ± 0.165V". Revised Output Rise/Fall Time Diagram.	8/19/02
B	T1 T2 T5	2 2 4 5 6 8 9 10	Pin Description Table - revised MR description. Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings, updated Output rating. AC Characteristics Table - added Additive Phase Jitter. Added Additive Phase Jitter Section. Updated LVPECL Output Termination drawings. Added Differential Clock Input Interface section. Added LVPECL Clock Input Interface section. Updated format throughout the data sheet.	2/3/04
B	 T9	1 15	Added Lead-Free bullet to Features section. Added Lead-Free marking to Ordering Information table.	2/10/05
B	 T9	1 15	Features Section - deleted bullet, "Industrial temperature information available upon request." Ordering Information Table - added Lead-Free note.	3/18/05
C	T4D	5 11 - 12	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CC} - 1.0V to V_{CC} - 0.9V; and V_{SWING} max. from 0.9V to 1.0V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4D.	4/13/07
C	T9	 15 17	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/9/10
C	T9	15	Ordering Information - removed leaded devices - PDN CQ-13-02	2/13/15

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 or +408-284-8200
Fax: 408-284-2775
www.IDT.com

Technical Support
email: clocks@idt.com

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