Enpirion® Power Datasheet

EN5364QI 6A PowerSoC Voltage Mode Synchronous Buck PWM DC-DC Converter With Integrated Inductor

Description

The EN5364QI is a Power Supply on a Chip (PwrSoC) DC to DC converter with integrated inductor, PWM controller, MOSFETS, and compensation providing the smallest possible solution size in a 68 pin QFN module. The switching frequency can be synchronized to an external clock or other EN5364QIs with the added capability of phasing multiple EN5364QIs as desired. Other features include precision ENABLE threshold, pre-bias monotonic start-up, margining, and parallel operation.

EN5364QI is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance applications such as set-top boxes/HD DVRs, LAN/SAN adapter cards, audio/video equipment, optical networking, multi-function printers, test and measurement, embedded computing, storage, and servers. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. Operating this converter requires very few external components.

The Altera Enpirion integrated inductor solution significantly helps to reduce noise. The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements.

All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Typical Application Circuit

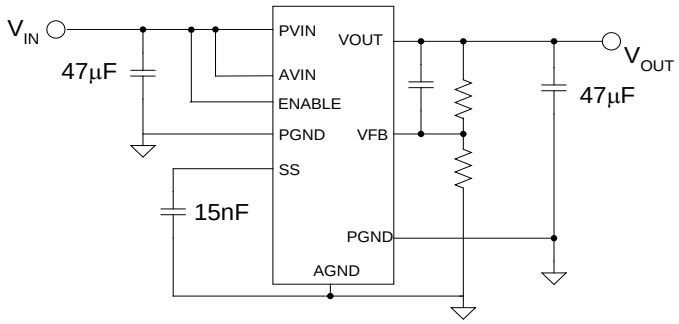


Figure 1: Typical Application Schematic

Features

- Integrated Inductor, MOSFETS, Controller in a 8 x 11 x 1.85mm package
- Wide input voltage range of 2.375V to 6.6V.
- > 20W continuous output power.
- High efficiency, up to 93%.
- Output voltage margining
- Monotonic output voltage ramp during start-up with pre-biased loads.
- Precision Enable pin for accurate sequencing of power converters and Power OK signal.
- Programmable soft-start time.
- Soft Shutdown.
- 4 MHz operating frequency with ability to synchronize to an external system clock or other EN5364's.
- Programmable phase delays between synchronized units to allow reduction of input ripple.
- Master/slave configuration for paralleling multiple EN5364's for greater power output.
- Under Voltage Lockout, Over-current, Short Circuit, and Thermal Protection
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V, 6V rails
- Computing, broadband, networking, LAN/WAN, optical, test & measurement
- A/V, high density cards, storage, DSL, STB, DVR, DTV, Industrial PC
- Beat frequency sensitive applications
- Applications requiring monotonic start-up with pre-bias
- Ripple voltage sensitive applications
- Noise sensitive applications
- Pin compatible with EN5394QI (9A)

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5364QI	-40 to +85	68-pin QFN T&R
EVB-EN5364QI	QFN Evaluation Board	

Pin Configuration

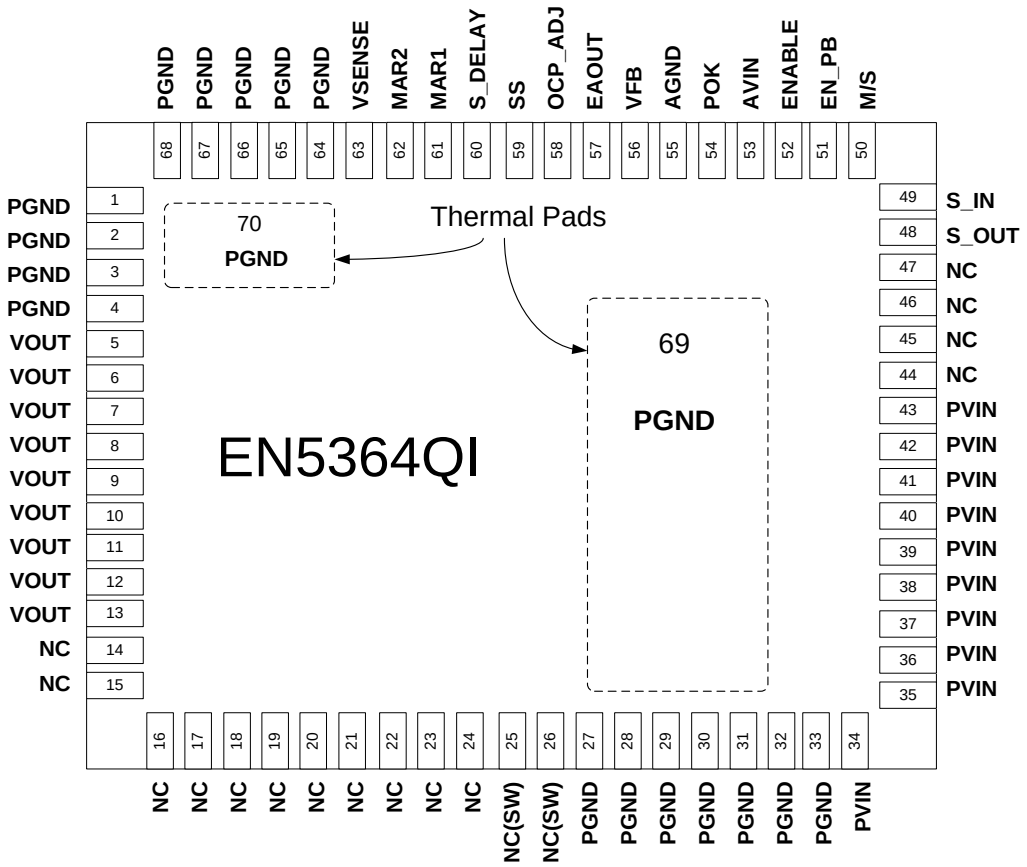


Figure 2: Pinout Diagram (Top View). All perimeter pins must be soldered to PCB.

Pin Descriptions

PIN	NAME	FUNCTION
1-4, 27-33, 64-68	PGND	Input/Output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN descriptions for more details.
5-13	VOUT	Regulated converter output. Connect to the load, and place output filter capacitor(s) between these pins and PGND pins 1-4 and 64-68.
14-24, 44-47	NC	NO CONNECT: These pins must be soldered to PCB but not be electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
25-26	NC(SW)	NO CONNECT: These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
34-43	PVIN	Input power supply. Connect to input power supply, place input filter capacitor(s) between these pins and PGND pins 27-33.
48	S_OUT	Clock Output. Depending on the mode, either a clock signal or the PWM signal is output on this pin. These signals are delayed by a time that is related to the resistor connected between S_DELAY and AGND. Leave this pin floating if not needed.
49	S_IN	Clock Input. Depending on the mode, this pin accepts either an input clock to synchronize the internal switching frequency or the S_OUT signal from another EN5364QI. Leave this pin floating if it is not used.
50	M/S	This is a Ternary Input. Floating the pin disables parallel operation. A low level configures the device as Master and a High level configures the device as a slave.
51	EN_PB	This is the Enable Pre-Bias Input. When this pin is pulled high, the Device will support monotonic start-up under a pre-biased load. There is a 150kΩ pull-down on this pin.
52	ENABLE	This is the Device Enable pin. A high level enables the device while a low level disables the device.
53	AVIN	Input power supply for the controller. Needs to be connected to V_{IN} at a quiet point.
54	POK	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal. Being an open drain output allows several devices to be wired to logically AND the function. Size pull-up resistor to limit current to 4mA when POK is low.
55	AGND	Ground return for the controller. Needs to be connected to a quiet ground.
56	VFB	External Feedback input. The feedback loop is closed through this pin. A voltage divider at V_{OUT} is used to set the output voltage. The mid-point of the divider is connected to VFB. The control loop regulates to make the VFB node voltage 0.6V.
57	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
58	OCP_ADJ	When this pin is pulled to AGND, the overcurrent protection trip point is increased by approximately 30%. Leave floating for default OCP threshold (see Electrical Characteristics table). Tie this pin to AGND for pin compatibility with the EN5394.
59	SS	A soft-start capacitor is connected between this pin to AGND. The value of the capacitor controls the soft-start interval and startup time.
60	S_DELAY	A resistor is connected between this pin and AGND. The value of the resistor controls the delay in S_OUT. This pin can be left floating if the S_OUT function is not used.
61-62	MAR1, MAR2	These are 2 ternary input pins. Each pin can be a logical Lo, Logical Hi or Float condition. 7 of the 9 states are used to modulate the output voltage by 0%, ±2.5%, ±5% or ±10%. The 8th state is used to by-pass the delay in S_OUT. See Functional Description section.
63	VSENSE	This pin senses VOUT when the device is placed in the Back-feed (or Pre-bias) mode.
69, 70	PGND	Device thermal pads to be connected to the system gnd plane. See Layout Recommendations section.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on PVIN, AVIN, VOUT	V_{IN}	-0.5	7.0	V
Voltages on VSENSE, ENABLE, EN_PB, POK,		-0.5	V_{IN} + 0.3	V
Voltages on VFB, EAOUT, SS, S_IN, S_OUT, OCP_ADJ		-0.5	2.7	V
Voltages on MAR1, MAR2, M/S		-0.5	3.6	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ MAX}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.375	6.6	V
Output Voltage Range	V_{OUT}	0.60	$V_{IN} - V_{DO}$ †	V
Output Current	I_{LOAD}	0	6	A
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

† V_{DO} (drop-out voltage) is defined as (I_{LOAD} x Dropout Resistance). Please see Electrical Characteristics table.

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM)††	θ_{JA}	16	°C/W
Thermal Resistance: Junction to Case	θ_{JC}	1	°C/W
Thermal Shutdown Trip Point	T_{SD}	+150	°C
Thermal Shutdown Trip Point Hysteresis	T_{SDH}	20	°C

†† Based on a four-layer board and proper thermal design in line with JEDEC EIJ/JESD 51 Standards.

Electrical Characteristics

NOTE: V_{IN}=5.5V over operating temperature range unless otherwise noted.
Typical values are at T_A = 25°C.

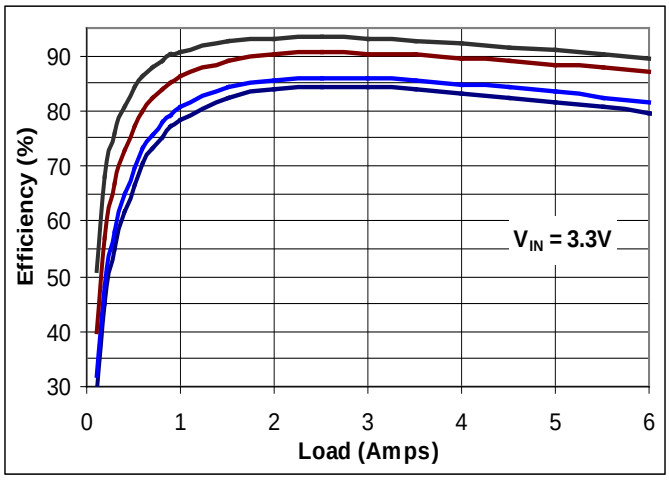
PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		2.375		6.6	V
Under Voltage Lock out threshold	V_{UVLOR} V_{UVLOF}	V_{IN} Increasing V_{IN} Decreasing		2.2 2.1		V
Shut-Down Supply Current	I_S	ENABLE=0V		250		µA
Feedback Pin Voltage	V_{FB}	2.375V ≤ VIN ≤ 6.6V, I_{LOAD} = 1A; T_A = 25°C	0.588	0.600	0.612	V
Feedback Pin Input Leakage Current[1]	I_{FB}		-5		5	nA
Line Regulation	ΔV_{OUT_LINE}	2.375V ≤ V_{IN} ≤ 6.6V		0.035		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ ILOAD ≤ 6A		–0.04		%/A
Temperature Regulation	ΔV_{OUT_TEMP}	-40°C ≤ TEMP ≤ 85°C		0.001		%/°C
V_{OUT} Rise Time	T_{RISE}	Measured from when V_{IN} ≥ V_{UVLOR} & ENABLE pin crosses logic high threshold. (4.7nF ≤ C_{SS} ≤ 100nF)		C_{SS} x 65kΩ		
Rise Time Accuracy[1]	ΔT_{RISE}	4.7nF ≤ C_{SS} ≤ 100nF	-25		+25	%
Output Dropout Voltage[1] Resistance[1]	V_{DO} R_{DO}	V_{INMIN} – V_{OUT} at Full Load Input to Output Resistance		240 40	480 80	mV mΩ
Maximum Continuous Output Current[2]	$I_{OUT\_MAX\_CONT}$		6			A
Current Limit Threshold	I_{OCP}	OCP_ADJ floating		10.5		A
ENABLE pin: Disable Threshold Enable Threshold	 $V_{DISABLE}$ V_{ENABLE}	2.375V ≤ V_{IN} ≤ 6.6V ENABLE pin logic low ENABLE pin logic high	 1.00		 1.0 1.30	V
ENABLE Lock-out time	t_{ENLO}	Time for device to re-enable after a falling edge on ENABLE pin		2		ms
ENABLE Pin Input Current	I_{ENABLE}	V_{IN} = 5.5V		50		µA
Switching Frequency	F_{SWITCH}	Free Running frequency		4		MHz
External S_IN Clock Frequency Lock Range	F_{PLL_LOCK}	Frequency Range of S_IN Input Clock	3.6		4.4	MHz
S_IN Threshold – Low	$V_{S\_IN\_LO}$	S_IN Clock low level			0.8	V
S_IN Threshold – High	$V_{S\_IN\_HI}$	S_IN Clock high level	1.8		2.5	V
S_OUT Threshold – Low	$V_{S\_OUT\_LO}$	S_OUT Clock low level			0.5	V
S_OUT Threshold – High	$V_{S\_OUT\_HI}$	S_OUT Clock high level	1.8			V
S_IN Duty Cycle for External Synchronization[1]	SY_{DC_SYNC}	M/S Pin Float or Low	20		80	%
S_IN Duty Cycle for Parallel Operation[1]	SY_{DC_PWM}	M/S Pin High	10		90	%
Phase Delay vs. S_Delay Resistor value	Φ_{DEL}	Delay in ns / kΩ Delay in phase angle / kΩ - @ 4MHz switching frequency		2 3		ns °

Phase Delay between S_IN and S_OUT[1]	Φ_{DEL}	Phase delay programmable via resistor connected from S_Delay to AGND.	20		150	ns
Phase Delay between S_IN and S_OUT[1]	Φ_{DEL}	Delay By-Pass Mode (MAR1 floating, MAR2 high)			10	ns
Phase Delay Accuracy[1]			-20		20	%
Pre-Bias Level	V_{PB}	Allowable Pre-Bias as a fraction of programmed output voltage (subject to a minimum of 300mV)	20		85	%
Non-Monotonicity	V_{PB_NM}	Allowable non monotonicity		50		mV
POK Lower Threshold as a percent of V_{OUT}[3]	POK_{LT}	V_{OUT} rising V_{OUT} falling		92 90		%
POK Upper Threshold as a percent of V_{OUT}[3]	POK_{UT}	V_{OUT} rising V_{OUT} falling		120 115		%
POK Falling Edge Deglitch Delay[4]				60		µs
POK Output Low Voltage	V_{POKL}	With 4mA current sink into POK			0.4	V
POK Output High Voltage	V_{POKH}	$2.375V \le V_{IN} \le 6.6V$			V_{IN}	V
Ternary Pin Logic Low[5]	$V_{T\text{-}Low}$	Tie pin to GND		0		V
Ternary Pin Logic High[5]	$V_{T\text{-}High}$	Pull up to V_{IN} through an external resistor R_{EXT} – see Figure 5.		see Input Current below		
Ternary Pin Input Current (see Figure 5)[5]	I_{TERN}	$V_{IN} = 2.375V$, $R_{EXT} = 3.32k\Omega$ $V_{IN} = 3.3V$, $R_{EXT} = 15k\Omega$ $V_{IN} = 5.0V$, $R_{EXT} = 24.9k\Omega$ $V_{IN} = 6.6V$, $R_{EXT} = 49.9k\Omega$		50 70 100 85		µA
Binary Input Logic Low Threshold[6]	$V_{B\text{-}Low}$				0.8	
Binary Input Logic High Threshold[6]	$V_{B\text{-}High}$		1.8			

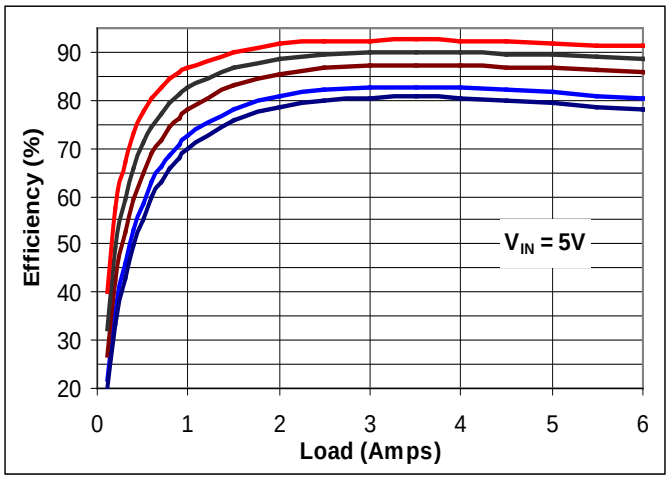
NOTES:

1. Parameter guaranteed by design.
2. Maximum output current may need to be de-rated, based on operating condition, to meet T_J requirements.
3. POK threshold when V_{OUT} is rising is nominally 92%. This threshold is 90% when V_{OUT} is falling. After crossing the 90% level, there is a 256 clock cycle (~50us) delay before POK is de-asserted. The 90%, 92%, 115%, and 120% levels are nominal values. Expect these thresholds to vary by ±3%.
4. On the falling edge of VOUT below 90% of programmed value, POK response is delayed for the duration of the deglitch delay time. Any VOUT glitch shorter than the deglitch time is ignored.
5. M/S, MAR1, and MAR2 are ternary. Ternary pins have three logic levels: high, float, and low. These pins are only meant to be strapped to V_{IN} through an external resistor, strapped to GND, or left floating. Their state cannot be changed while the device is on.
6. Binary input pins are EN_PB and OCP_ADJ.

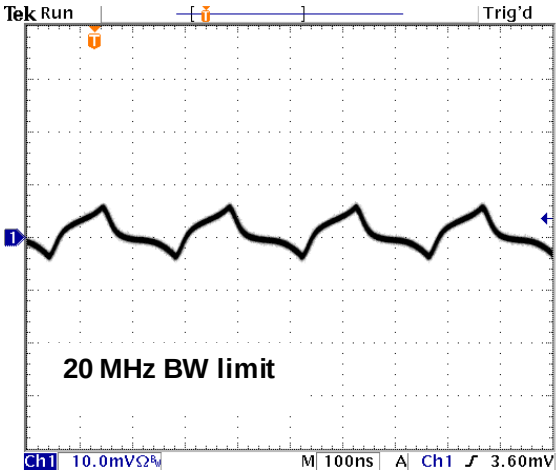
Typical Performance Characteristics



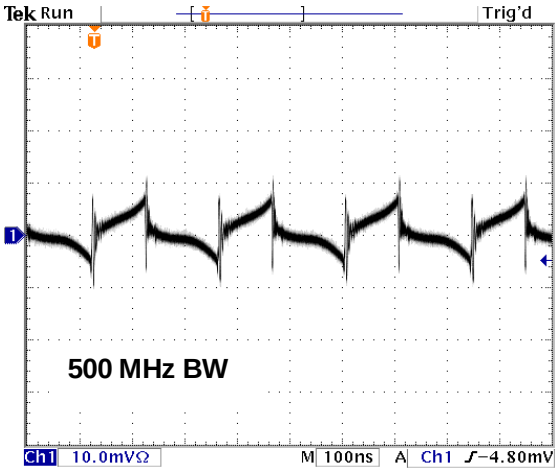
Efficiency V_{IN} = 3.3V
V_{OUT} (From top to bottom) = 2.5, 1.8, 1.2, 1.0V



Efficiency V_{IN} = 5.0V
V_{OUT} (From top to bottom) = 3.3, 2.5, 1.8, 1.2, 1.0V



Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.2V, Iout = 6A
C_{IN} = 2 x 22µF/1206, C_{OUT} = 47µF/1206 + 10uF/0805



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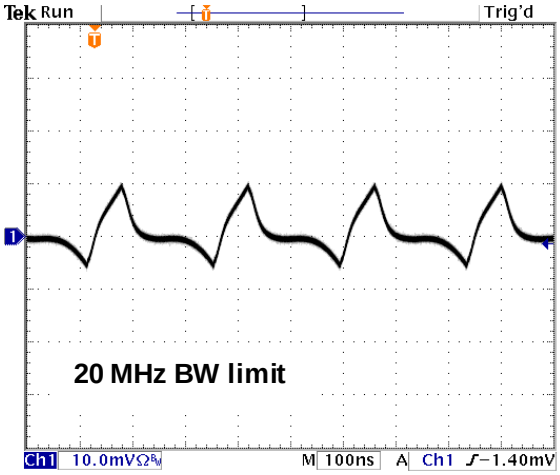

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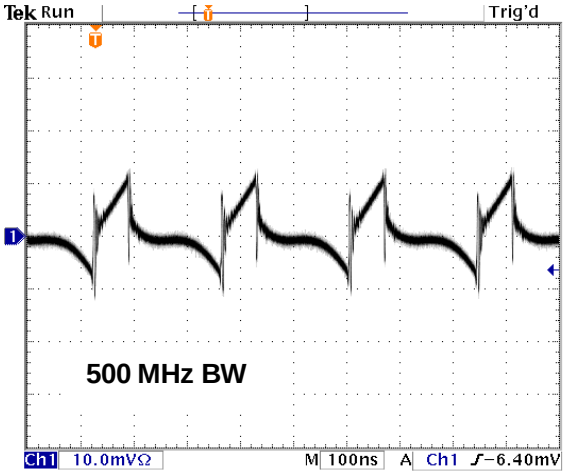

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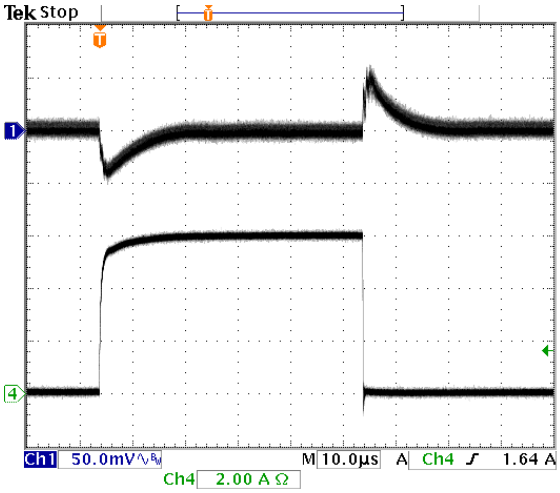
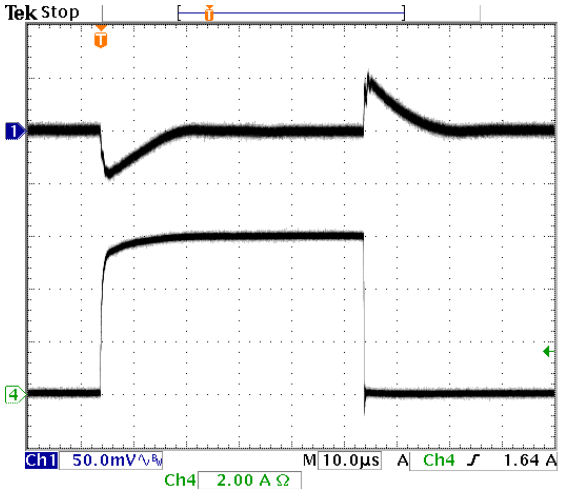
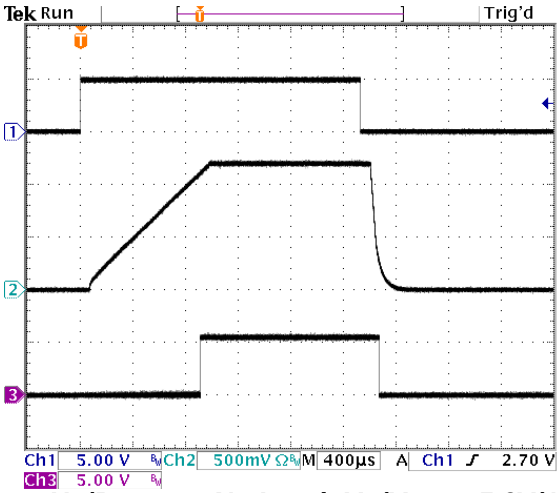


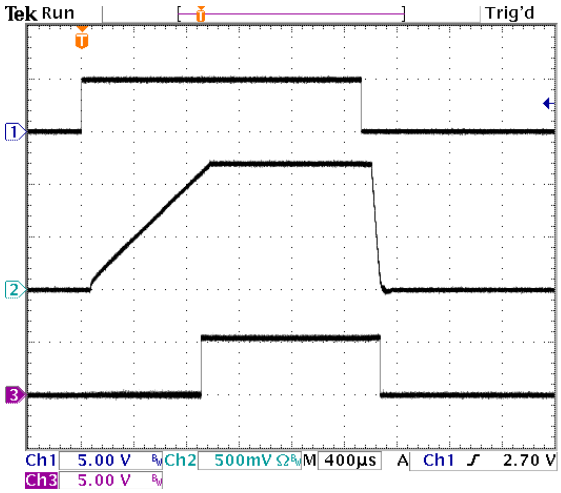
Load Transient: V_{IN} = 5.0V, V_{OUT} = 1.2V
Ch.1: V_{OUT}, Ch.4: I_{LOAD} 0↔6A (slew rate ≥ 10A/µS)
C_{IN} ≈ 50µF, C_{OUT} ≈ 50µF
R_A = 150kΩ, C_A = 27pF (see Figure 4)



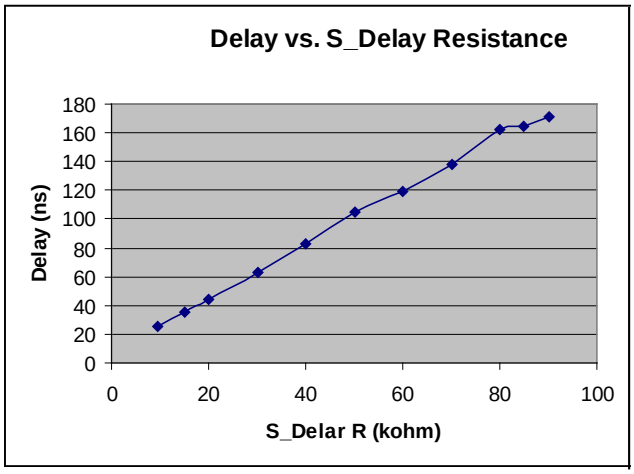
Load Transient: V_{IN} = 3.3V, V_{OUT} = 1.2V
Ch.1: V_{OUT}, Ch.4: I_{LOAD} 0↔6A (slew rate ≥ 10A/µS)
C_{IN} ≈ 50µF, C_{OUT} ≈ 50µF
R_A = 100kΩ, C_A = 47pF (see Figure 4)



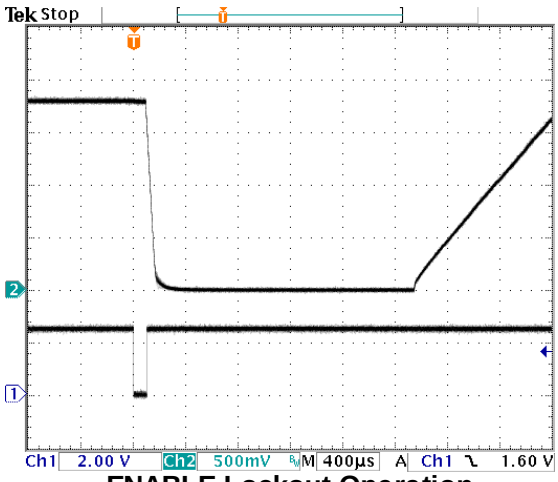
Power Up/Down at No Load: V_{IN}/V_{OUT} = 5.0V/1.2V,
15nF soft-start capacitor,
Ch.1: ENABLE, Ch.2: V_{OUT}, Ch.3; POK



Power Up/Down into 0.2Ω load: V_{IN}/V_{OUT} = 5.0V/1.2V,
15nF soft-start capacitor,
Ch.1: ENABLE, Ch.2: V_{OUT}, Ch.3; POK



Delay vs. S_Delay Resistance



ENABLE Lockout Operation
Ch.1: ENABLE, Ch2: V_{OUT}

Block Diagram

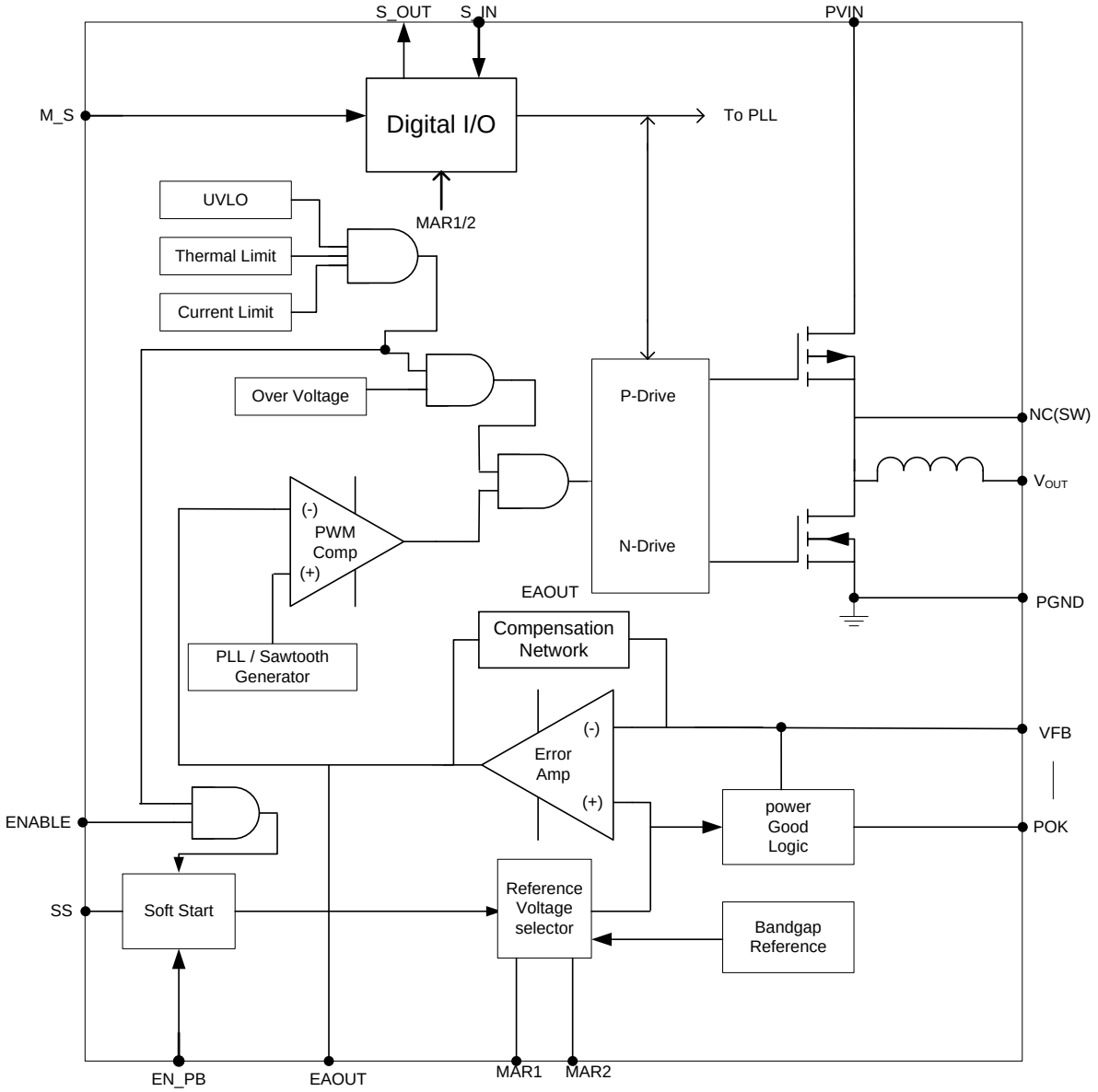


Figure 3. System Block Diagram

Functional Description

Synchronous Buck Converter

The EN5364QI is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.375-6.6V. The output voltage is programmed using an external resistor divider network. The feedback control loop is a type III, voltage-mode, and the device uses a low-noise PWM topology. Up to 6A of continuous output current can be drawn from this converter. The 4MHz operating frequency enables the use of small-size input and output capacitors.

The power supply has the following protection features:

- Over-current protection with hiccup mode.
- Short Circuit protection.
- Thermal shutdown with hysteresis.

- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Enable Operation

The ENABLE pin provides a means to start normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The device will remain shut-down for the duration of the ENABLE lockout time (see Electrical Characteristics Table). If the ENABLE signal is re-asserted during this time, the device will power up with a normal soft-start at the end of the ENABLE lockout time.

The Enable threshold is a precision Analog voltage rather than a digital logic threshold. Precision threshold along with choice of soft-start capacitor helps to accurately sequence multiple power supplies in a system.

Frequency Synchronization

The switching frequency of the DC/DC converter can be phase-locked to an external clock source to move unwanted beat frequencies out of band. To avail this feature, the ternary input M/S pin should be floating or pulled low. The internal switching clock of the DC/DC converter can then be phase locked to a clock signal applied to S_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is within ±10% of the free running frequency (see Electrical Characteristics table). When no clock signal is present, the device reverts to the free running frequency of the internal oscillator. The external clock input may be swept between 3.6 MHz and 4.4 MHz at repetition rates of up to 10 kHz in order to reduce EMI frequency components.

Master / Slave Parallel Operation

Multiple EN5364QI devices may be connected in parallel in a Master/Slave configuration to handle load currents greater than device maximum rating. The device is set in Master mode by pulling the ternary M/S pin low or in Slave mode by pulling M/S pin high to V_{IN} through an external resistor. When this pin is in Float state, parallel operation is not possible. In master mode, the internal PWM signal is output on the S_OUT pin. This PWM signal from the Master can be fed to one or more Slave devices at its S_IN input. The Slave device acts like an extension of the power FETs in the Master. As a practical matter, paralleling more than 4 devices may be very difficult from the view point of maintaining very low impedance in V_{IN} and V_{OUT} lines.

The table below summarizes the different configurations for the S_IN and S_OUT pins depending on the condition of the M/S pin:

When M/S pin is:	High (Slave)	Low (Master)	Float
S_IN input should be:	S_OUT from Master	External Sync input if needed (NC for internal clock)	
S_OUT is equal to (subject to S_DELAY):	Same duty cycle as S_IN	Same duty cycle as internal PWM	S_IN or internal clock

Please contact Altera Power Applications support for more information on Master / Slave operation.

Phase Delay

In all cases, S_OUT can be delayed with respect to internal switching clock or the clock applied to S_IN. Multiple EN5364QI devices on a system board may be daisy chained to reduce or eliminate input ripple as well as avoiding beat frequency components. The EN5364QIs can all be phase locked by feeding S_OUT of one device into S_IN of the next device in a daisy chain. All the switchers now run at a common frequency. The delay is controlled by the value of a resistor connected between S_DELAY and AGND pins. The magnitude of this delay as a function of S_DELAY resistor is shown in the Electrical Characteristics table. See Figures 6 and 7 for an example of using phase delay.

Margining

Using MAR1 and MAR2 pins, the nominal output

voltage can be increased / decreased by 2.5, 5 or 10% for system compliance, reliability or other tests. The POK threshold voltages scale with the margined output voltages. The following table provides the possible combinations:

MAR1	MAR2	Output Modulation
Float	Float	0%
Low	Low	-2.5%
High	Low	+2.5%
Low	High	-5%
High	High	+5%
Low	Float	-10%
High	Float	+10%
Float	High	0%, Delay Bypass
Float	Low	Reserved

Note: Low means tie to GND. High means tie to V_{IN} as shown in Figure 5.

As shown above, when MAR1 is floating, and MAR2 is high, the device enters the delay bypass mode. In this mode, the delay from the internal clock or S_IN to S_OUT is almost eliminated (see Electrical Characteristics table).

Soft-Start Operation

The SS pin in conjunction with a small external capacitor between this pin and AGND provides the soft start function to limit the in-rush current during start-up. During start-up of the converter the reference voltage to the error amplifier is gradually increased to its final level as an internal current source of typically 10uA charges the soft start capacitor. The typical soft-start time for the output to reach regulation voltage, from when AVIN > V_{UVLO} and ENABLE crosses its logic high threshold, is given by:

$$T_{SS} = (C_{SS} * 65K\Omega) \pm 25\%$$

Where the soft-start time T_{SS} is in seconds and the soft-start capacitance C_{SS} is in Farads. Typically, around 15nF is recommended. The soft-start capacitor should be between 4.7nF and 100nF. A proper choice of SS capacitance can be used advantageously for power supply sequencing using the precision Enable threshold.

During a soft-start cycle, when the soft-start capacitor voltage reaches 0.60V, the output has reached its programmed regulation range. Note that the soft-start current source will continue to charge the SS capacitor beyond 0.6V. During normal operation, the soft-start capacitor will charge to a final value of ~1.5V.

Soft-Shutdown Operation

When the Enable signal is de-asserted, the soft-start capacitor is discharged in a controlled manner. Thus the output voltage ramps down gradually. The internal circuits are kept active for the duration of soft-shutdown, thereafter they are deactivated.

Pre-Bias Operation

When EN_PB is asserted, the device will support a monotonic output voltage ramp if the output capacitor is charged to a pre-bias level. Proprietary circuit ensures the output voltage ramps monotonically from pre-bias voltage to the programmed output voltage. Monotonic start-up is guaranteed by design for pre-bias voltages between 20% and 85% of the programmed output voltage. This feature is not supported when ENABLE is tied to V_{IN}.

POK Operation

The POK signal indicates if the output voltage is within a specified range. The POK signal is asserted when the rising output voltage crosses 92% (nominal) of the programmed output voltage. POK is de-asserted ~50us (256 clock cycles) after the falling output voltage crosses 90% (nominal) of the programmed voltage. POK is also de-asserted if the output voltage exceeds 120% of the programmed output. If the feedback loop is broken, POK will remain de-asserted (output < 92% of programmed value), and the output voltage will equal the input voltage. If however, there is a short across the PFET, and the feedback is in place, POK will be de-asserted as an over voltage condition. The power NFET is also turned on, resulting in a large input supply current. This in turn is expected to trip the OCP of the EN5364QI input power supply.

POK is an open drain output. It requires an external pull up. Multiple EN5364QI's POK pins may be connected to a single pull up. The open drain NFET is designed to sink up to 4mA. The

pull-up resistor value should be chosen accordingly for when POK is logic low.

Input Under-Voltage Lock-Out (UVLO)

When the input voltage is below a required voltage level (V_{UVLO}) for normal operation, the converter switching is inhibited. The lock-out threshold has hysteresis to prevent chatter. UVLO is implemented to ensure that operation does not begin before there is adequate voltage to properly bias all internal circuitry.

Over-Current Protection (OCP)

The current limit and short-circuit protection is achieved by sensing the current flowing through a sense P-FET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off. If the over-current condition is removed, the over-current protection circuit will re-enable the PWM operation. If the over-current condition persists, the circuit will continue to protect the device.

The OCP trip point is nominally set to 175% of maximum rated load. In the event the OCP circuit trips, the device enters a hiccup mode. The device is disabled for ~10msec and restarted with a normal soft-start. This cycle can continue indefinitely as long as the over current condition persists. During soft-start at power up or fault recovery, the hiccup mode is disabled and the device has cycle-by-cycle current limiting.

Thermal Overload Protection

Thermal shutdown will disable operation when the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approximately 20ºC, the converter will re-start with a normal soft-start.

Compensation

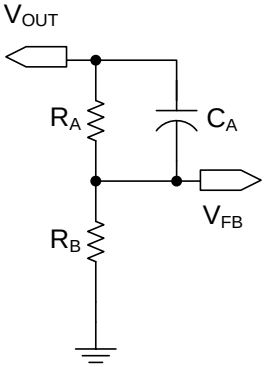
The EN5364 uses of a type III compensation network. Most of this network is integrated. However a phase lead capacitor is required in parallel with upper resistor of the external divider network (see Figure 4). This network results in a wide loop bandwidth and excellent load transient performance. It is optimized for around 50µF of output filter capacitance at the voltage sensing point. Additional decoupling capacitance may be placed beyond the voltage sensing point outside the control loop. Voltage-mode operation provides high noise immunity at light load. Further, voltage-mode control provides superior impedance matching to ICs processed in sub 90nm technologies.

In exceptional cases modifications to the compensation may be required. The EN5364QI provides the capability to modify the control loop response to allow for customization for specific applications. For more information, contact Altera Power Applications support.

Application Information

Output Voltage Programming

The EN5364 output voltage is determined by the voltage presented at the VFB pin. This voltage is set by way of a resistor divider between V_{OUT} and AGND with the midpoint going to VFB. A phase lead capacitor C_A is also required for stabilizing the loop. Figure 4 shows the required components and the equations to calculate their values. Please note the equations below are written to optimize the control loop as a function of input voltage.



$$R_A = 30{,}000 \times Vin \quad \text{(value in } \Omega\text{)}$$

$$C_A = \frac{4.72 \times 10^{-6}}{R_A} \quad (C_A/R_A \text{ in } F/\Omega)$$

Round C_A down to closest standard value lower than calculated value.

$$R_B = \frac{V_{FB} \times R_A}{(V_{OUT} - V_{FB})} \quad \begin{pmatrix} V_{FB} \text{ is } 0.6V \\ \text{nominal} \end{pmatrix}$$

Figure 4: Output voltage resistor divider and phase-lead capacitor calculation. The equations need to be followed in the order written above.

Input Capacitor Selection

The EN5364QI requires between 20-40uF of input capacitance. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors may be needed in parallel with the larger capacitors in order to provide high frequency decoupling.

Recommended Input Capacitors

Description	MFG	P/N
10uF, 10V, 10% X7R, 1206 (2-4 capacitors needed)	Murata	GRM31CR71A106KA01L
	Taiyo Yuden	LMK316B7106KL-T
22uF, 10V, 20% X5R, 1206 (1-2 capacitors needed)	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T
47uF, 6.3V, 20% X5R, 1206 (1 capacitor needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK212BJ476ML-T

Output Capacitor Selection

The EN5364 has been optimized for use with about 50µF of output filter capacitance. Up to 100µF can be placed at the voltage sensing point. Additional capacitance may be placed beyond the voltage sensing point outside the control loop. For the output filter, low ESR X5R or X7R ceramic capacitors are required. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Recommended Output Capacitors

Description	MFG	P/N
47uF, 6.3V, 20% X5R, 1206 (1 capacitor needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK212BJ476ML-T
10uF, 6.3V, 10% X5R, 0805 (Optional 1 capacitor in parallel with 47uF above)	Murata	GRM21BR60J106KE19L
	Taiyo Yuden	JMK212BJ106KG-T

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. At the 4MHz switching frequency, the capacitor impedance, denoted as Z, is comprised mainly of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing multiple capacitors in parallel reduces the impedance and hence will result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Typical ripple versus capacitor arrangement is given below:

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5364QI Evaluation Board)†
1x47uF	30mV
1x47uF + 1x10uF	15mV

† 20 MHz bandwidth limit

Ternary Pin Inputs

The three ternary pins MAR1, MAR2, and M/S have three possible states. In the Low state, the pins are to be tied to GND. In the floating state, nothing is to be connected to the pins. In the High state, they are to be tied to V_{IN} through an external resistor R_{EXT} in order to limit the input current to the pin (see Figure 5). The Electrical Characteristics table lists, as a function of V_{IN}, some recommended values for R_{EXT}, and the resulting input currents.

Frequency Sync & Phase Delay

The EN5364 can be synchronized to an external clock source or to another EN5364 in order to eliminate unwanted beat frequencies. Furthermore, two or more synchronized EN5364's can have a programmable phase delay with respect to each other to minimize input voltage ripple and noise. An example of synchronizing three EN5364's with approximately equal phase delay between them is shown in Figures 6 and 7. The lowest allowable value for the S_DELAY resistor is 10kΩ.

Power Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power

down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

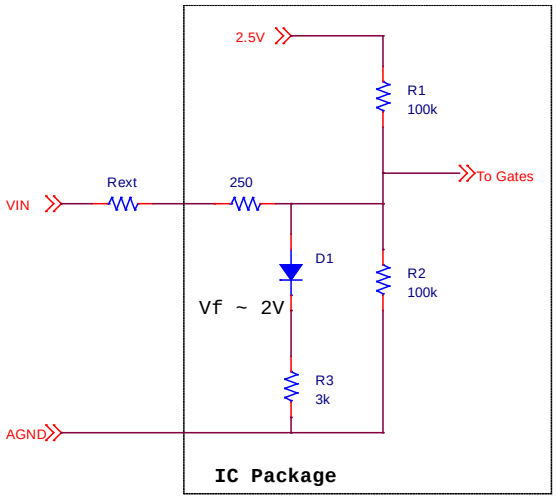


Figure 5: Equivalent circuit of a ternary pin (MAR1, MAR2, or M/S) input buffer. To get a logic High on a ternary input, pull the pin to V_{IN} through an external resistor R_{EXT}. See Electrical Characteristics table for some recommended R_{EXT} values as a function of V_{IN} and the resulting input currents.

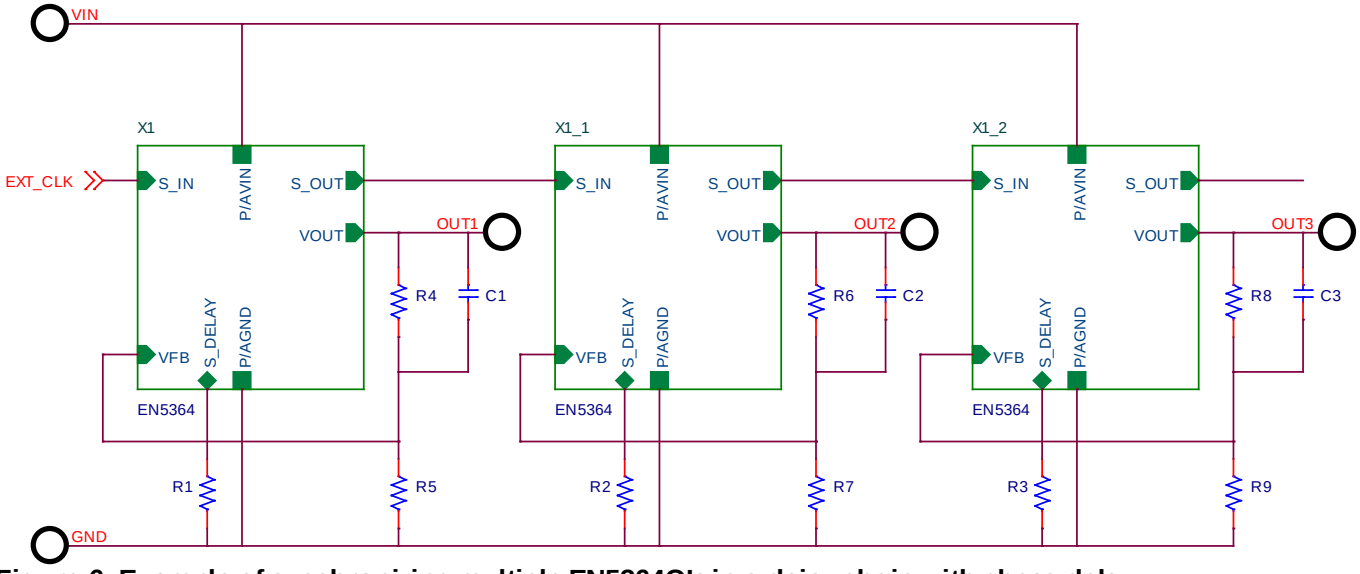


Figure 6: Example of synchronizing multiple EN5364QIs in a daisy chain with phase delay.

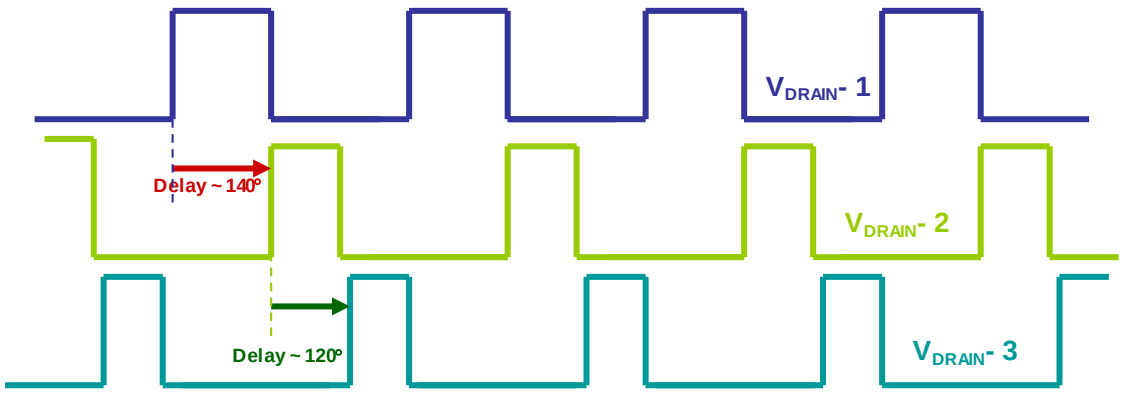
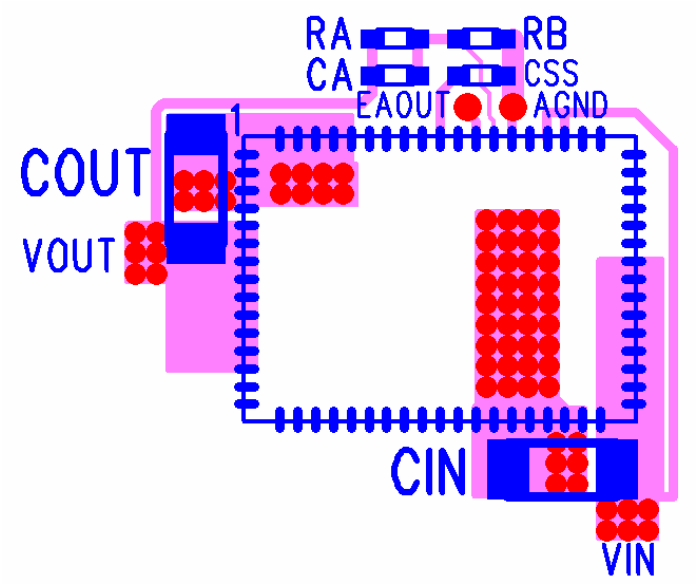


Figure 7: Example of a possible way to synchronize and use delays advantageously to minimize input ripple. R1 ~ 39kΩ, R2 ~ 33kΩ. (Refer to Figure 6 for R1 and R2.) R3 does not matter in this case.

Layout Recommendations



- RA and RB are voltage programming resistors.
- CA is used for loop compensation.
- CSS is the soft-start capacitor.
- AGND via is also a test point.
- Test point added for EAOUT.

Figure 8: Critical Components and Layer 1 Copper for Minimum Footprint

Figure 8 above shows critical components and layer 1 traces of the recommended EN5364 layout for minimum footprint with ENABLE tied to V_{IN}. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files at www.altera.com/enpirion for exact dimensions and other layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5364QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5364QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The system ground plane referred to in recommendations 2 and 3 should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 3: The large and small thermal pads underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see figures: 8, 9, and 10.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 3) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 8 this connection is made at the input capacitor.

Recommendation 6: The layer 1 metal under

the device must not be more than shown in Figure 8. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 7: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.

Recommendation 8: Keep R_A, C_A, and R_B close to the VFB pin (see Figures 4 and 8). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Thermal Considerations

The Altera Enpirion EN5364QI DC-DC converter is packaged in an 11 x 8 x 1.85mm 68-pin QFN package. The QFN package is constructed with copper lead frames that have exposed thermal pads. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C will reduce long-term reliability. The device has a thermal overload protection circuit designed to shut it off at an approximate junction temperature value of 150°C.

The silicon is mounted on a copper thermal pad that is exposed at the bottom of the package. There is an additional thermal pad in the corner of the package which provides another path for heat flow out from the package. The thermal resistance from the silicon to the exposed thermal pads is very low. In order to take advantage of this low resistance, the exposed thermal pads on the package should be soldered directly on to a copper ground pad on layer 1 of the PCB. The PCB then acts as a heat sink. In order for the PCB to be an effective heat sink, the device thermal pads should be coupled to copper ground planes using multiple vias (refer to Layout Recommendations section).

The junction temperature, T_J, is calculated from the ambient temperature, T_A, the device power dissipation, P_D, and the device junction-to-ambient thermal resistance, θ_{JA} in °C/W:

$$T_J = T_A + (P_D)(\theta_{JA})$$

The junction temperature, T_J, can also be expressed in terms of the device case temperature, T_C, and the device junction-to-case thermal resistance, θ_{JC} in °C/W, as follows:

$$T_J = T_C + (P_D)(\theta_{JC})$$

The device case temperature, T_C, is the temperature at the center of the larger exposed thermal pad at the bottom of the package.

The device junction-to-ambient and junction-to-case thermal resistances, θ_{JA} and θ_{JC}, are shown in the Thermal Characteristics table. The θ_{JC} is a function of the device and the 68-pin QFN package design. The θ_{JA} is a function of θ_{JC} and the user's system design parameters that include the thermal effectiveness of the customer PCB and airflow.

The θ_{JA} value shown in the Thermal Characteristics table is for free convection with the device heat sunk (through the thermal pads) to a copper plated four-layer PC board with a full ground and a full power plane following JEDEC EIJ/JESD 51 Standards. The θ_{JA} can be reduced with the use of forced air convection. Because of the strong dependence on the thermal effectiveness of the PCB and the system design, the actual θ_{JA} value will be a function of the specific application.

When operating on a board with the θ_{JA} of the thermal characteristics table, no thermal deratings are needed to operate all the way up to maximum output current.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 9.

Only the two thermal pads and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5364QI should be clear of any metal (copper pours, traces, or vias) except for the two thermal pads. The “grayed-out” area in Figure 9 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the grayed-out area runs the risk of undesirable shorted connections even if it is covered by soldermask. One exposed pad in the grayed-out area can have V_{IN} metal under it as noted in Figure 9.

Figure 10 demonstrates the recommended PCB footprint for the EN5364QI. Figure 11 shows the package dimensions.

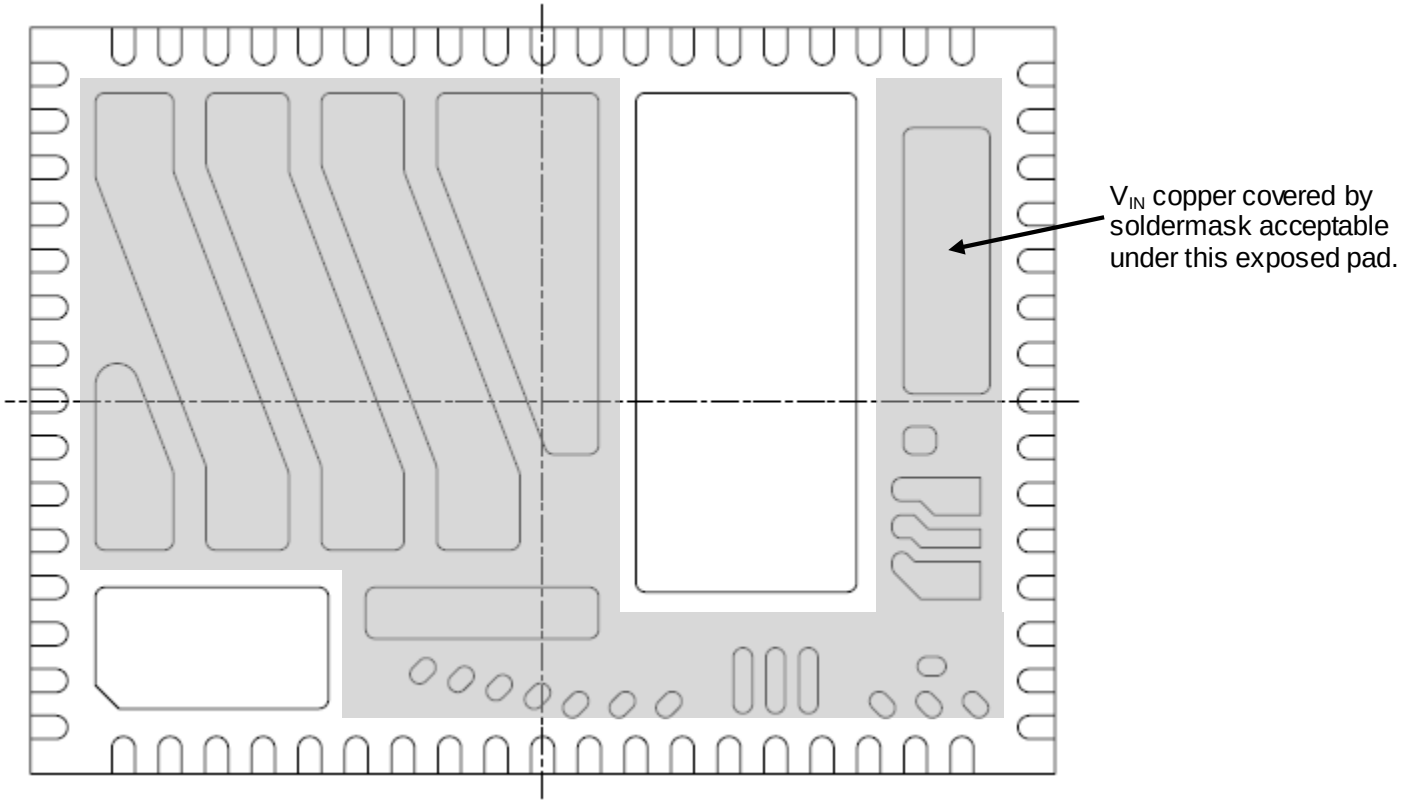


Figure 9: Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

PCB Footprint and Package Dimensions

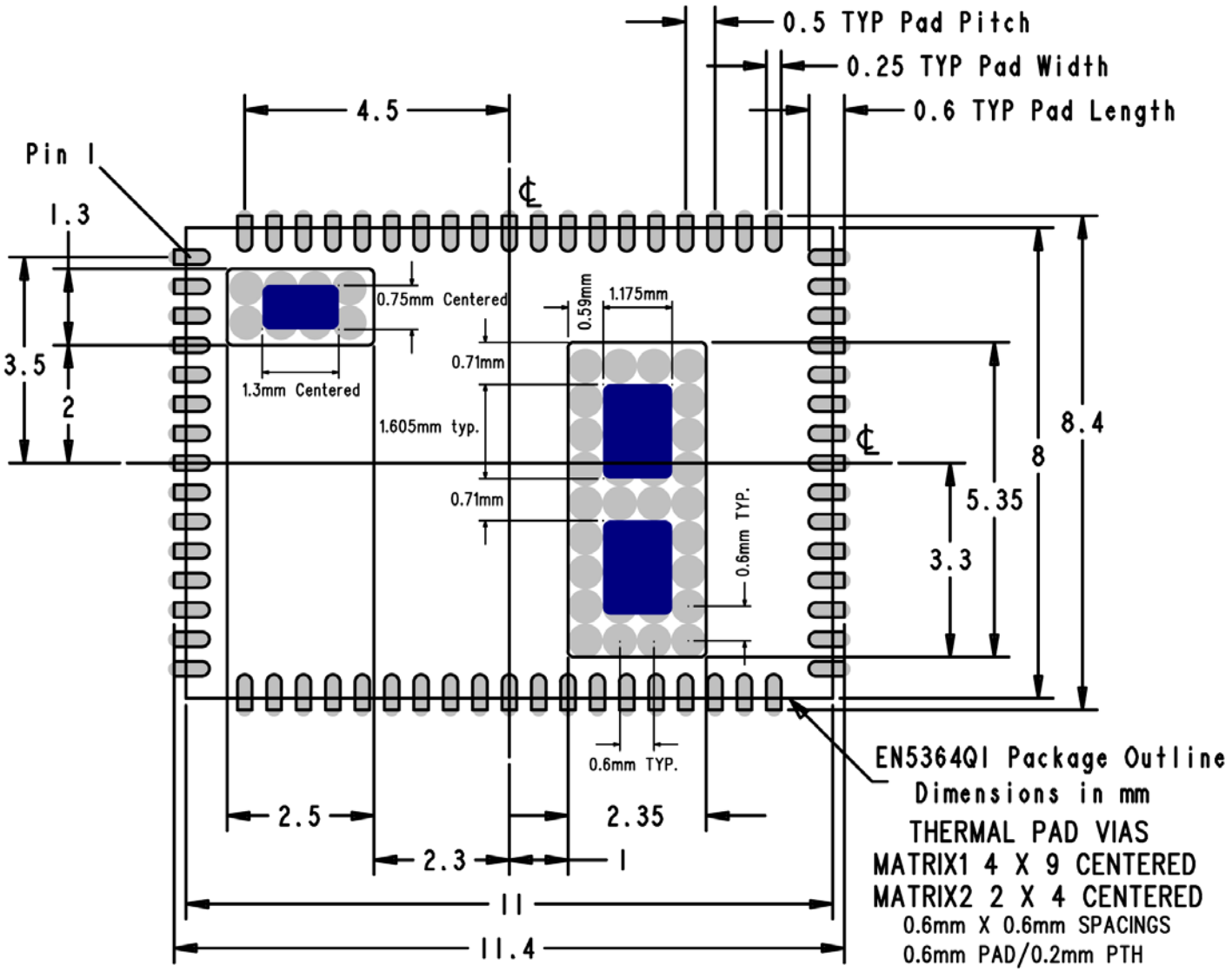


Figure 10: EN5364QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

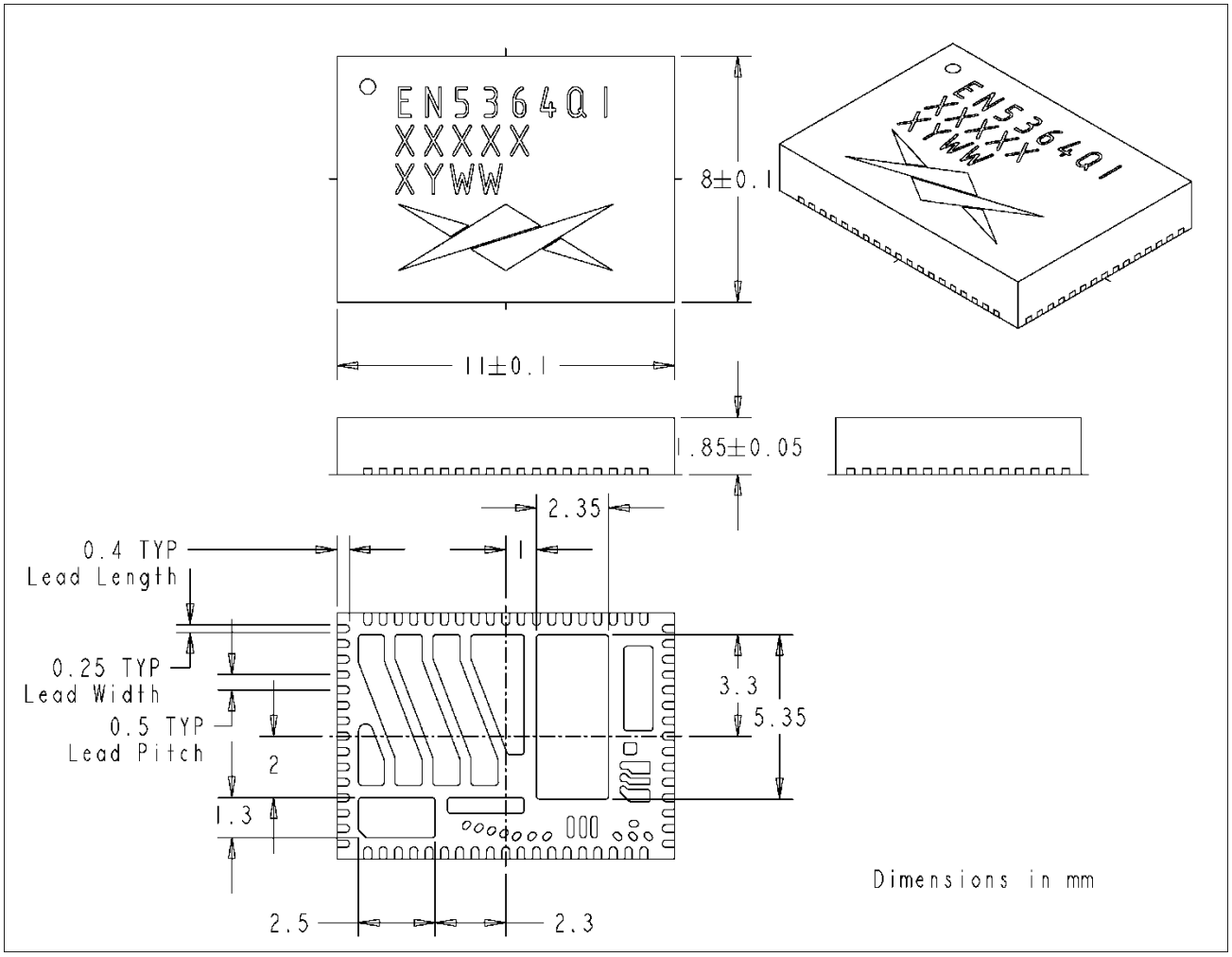


Figure 11. Package Dimensions

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