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UNITE7002 Quick Start Manual

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REVISION HISTORY

The following table shows the revision history of this document:

Date	Version	Description of Revisions
22/10/2015	1.00	Initial version
30/10/2015	1.01	Updated section 4.1, corrected names of the connectors in Figure 20, descriptions of switches and connectors in Table 1

Contents

Table of Figures

1

Introduction

The Lime Development System is a comprehensive hardware and software combination that allows users to evolve and refine a wireless sub-system. It can be combined with a baseband processor such as an FPGA or DSP processor to develop a comprehensive wireless solution.

The UNITE7002 module is a high-speed wireless communication module, based on the LMS7002M fully programmable RF transceiver. It is designed to support 2G, 3G, 4G/LTE radio systems with both time-division duplex (TDD) and frequency-division duplex (FDD) applications, M2M and software defined radios. The wireless communication module covers the frequency range of 100 kHz to 3.8 GHz, including licensed and unlicensed bands. The channel bandwidth is programmable from less than 100 kHz to 108 MHz through a combination of analog and digital filtering via the easy-to-use GUI software.

The UNITE7002 provides system designers with the ability to connect the board to any type of baseband, FPGA or CPU and allow them to implement their ideas for various wireless communication applications.

This document describes how to make a quick start with the LMS7002M using the UNITE7002 module. Section *2* begins by listing the contents of the Quick Start kit. Section *3* gives a general description of the evaluation board features. Section *4* describes the procedure for obtaining and installing the LMS 7 Suite software 'LMS 7 Suite' for both Windows and Linux platforms. Section *5* describes how to connect and use the EVB and LMS 7 Suite for the Quick Start example configurations. Section *6* describes in detail the EVB connectors and hardware options. Section *7* describes in detail how to use the LMS 7 Suite. Section *8.1* describes calibration procedures. Appendix 1 details the recommended test and measurement equipment, and how to set up the test equipment to work with UNITE7002 and the LMS7002M.

2

Development System Content

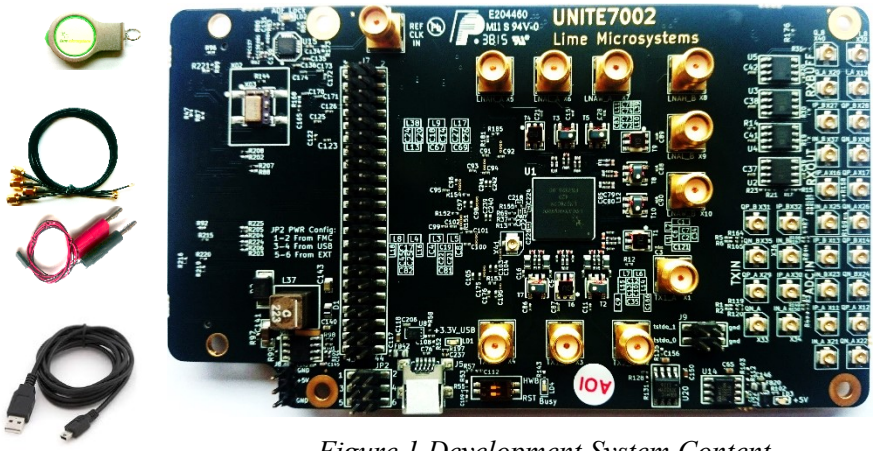

Figure 1 Development System Content

Complete development kit content consists of:

- Hardware
  - 1 x UNITE7002 board
  - 1 x Power supply cable that connects the UNITE7002 board to any lab power supply unit
  - 1 x USB-A to Micro-USB-B cable
  - USB stick with software
  - 4 x SMA to U.FL RF cables
- Software:
  - LMS7002M GUI “lms7suite”
  - Waveforms example files
  - Windows drivers
- Documentation:
  - UNITE7002 Quick Starter Manual
  - LMS7002M Data Sheet
  - UNITE7002 PCB Schematic
  - LMS7002M Programming and Calibration Guide

3

Overview of the Development Board

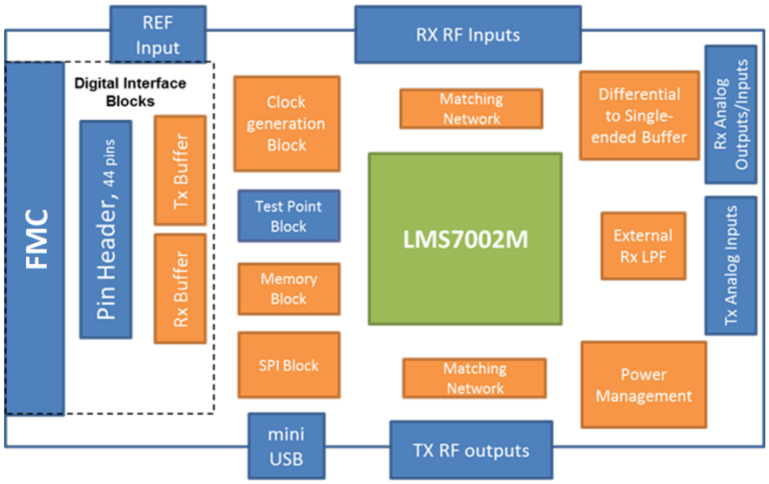

Figure 2 Board block diagram

A photograph of the development board is shown in *Figure 1*. A block diagram of the board is shown in *Figure 2*. The connections are shown in blue, the LMS7002M chip is shown in green, and the other parts are shown in orange. The core of the board is the LMS7002M transceiver chip, which has multiple RF, analogue and digital interfaces.

The evaluation board includes RF matching networks for the LMS7002M. These matching networks include wideband transformers to allow operation over the entire frequency range. However, the matching networks have been optimized for operation over selected frequency bands and offer the best performance in these bands. Connectors are provided for 4 RF transmitter outputs and 6 RF receiver inputs. Further details of the matching networks are provided in section *6.3.5*.

The evaluation board includes connectors for the baseband analogue differential receiver outputs and differential transmitter inputs. Additionally, on board high speed differential to single ended converters allow the UNITE7002 receivers to indirectly drive 50 Ohm test equipment such as spectrum analysers for baseband testing.

The evaluation board includes a clock generation block, which by default, is a standalone 30.72 MHz low phase noise TXCO. TXCOs at other frequencies can also be fitted and three different footprints are supported. The UNITE7002 can be easily modified to operate with external clock sources. It can also be synchronized to the standard 10 MHz reference of measurement equipment via an on board PLL. Details of the required changes on UNITE7002 are given in section *6.3.1* and *6.3.2*.

UNITE7002 includes two kinds of digital I/O, one for control only, and two for data and control.

The USB interface is used to control the LMS7002M SPI via the LMS 7 Suite. The USB port is converted to SPI by an on board microcontroller.

The FMC connector or the 44 pin header can be used for the buffered digital interface and can be connected to compatible platforms such as the Lime "Stream" board. The Lime "Stream" board also provides connections to general purpose lab equipment such as pattern generators and logic analysers. A pin list for the digital interface can be found in section *6.2*. The logic level for the digital interface can be set by modifying UNITE7002 and is described in section *6.3.4*. Additionally these connectors can be used to control the SPI but require the board modifications described in *6.3.3*.

A 7th order LC filter can be selected between the receiver analogue output of the LMS7002M and its receiver ADC external inputs by using the 'LMS 7 Suite' software. This allows additional filtering at 100 kHz (IF BW) for 2G applications.

The board includes memory to work with the LMS7002M internal microcontroller. This is intended to provide calibration support for the LMS7002M and is currently under development. The memory is programmed via the LMS 7 Suite and the USB/SPI interface.

Test points are provided for various test signals including the LMS7002M internal peak and RSSI detectors as well as various PLL test signals.

More detailed information on the connectors for the evaluation board can be found in section *6.1*. Information about PCB options supported is in section *6.3*.

4

Installing the LMS 7 Suite

4.1 Introduction to installing the software

To operate the UNITE7002 board, the latest version of "LMS 7 Suite" has to be downloaded from http://www.limemicro.com/resources under the section 'UNITE7002 Software' and installed. The software consists of four parts.

- The main LMS 7 Suite Software, which provides a GUI to control the chip.
- Waveforms to generate either CW test signal or W-CDMA Test mode 1 signal
- The USB driver "USB to LMS7002M", which provides an interface between the PC and the EVB7 SPI microcontroller.
- The EVB7 microcontroller firmware, which is preinstalled on the board prior to shipping.

Sections *4.2*, *4.3, 4.4* and *4.5* describe the set up for the Windows Operating System. Section *4.2* describes the installing of the "USB to LMS7002M" driver. Section *4.3* describes how to identify which USB port is being used. Section *4.4* describes how to run the kit on Linux OS. Section *4.5* describes how to start running the 'LMS 7 Suite' on Windows. Section *4.6* describes how to connect the UNITE7002 with the 'LMS 7 Suite' via the USB interface.

A simple demonstration of the 'LMS 7 Suite' is given in section *5*. A detailed description of the 'LMS 7 Suite' is given in section *7*.

4.2 Windows USB Setup

The steps to setup "Control LMS7002M" software are as follows (please note that these steps may vary based on the specific version of Windows software being used and you may need to be logged in as Administrator to accomplish them):

1. Connect UNITE7002 board to your PC via the USB cable

2. Go to **Control Panel > System > Device Manager**

3. Locate **USB to LMS7002M** under **Other devices** and press right click to select **Properties** *Figure 3*

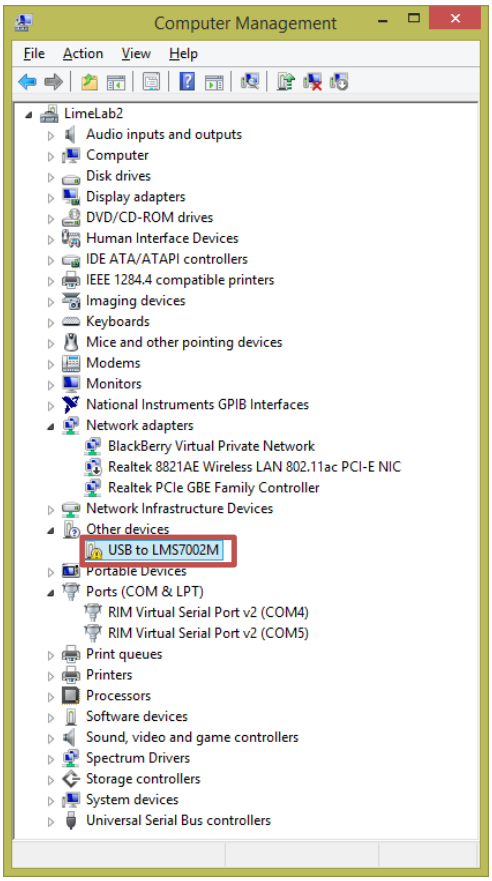

Figure 3 Device Manager content

4. When a new window pops-up press Update driver *Figure 4*

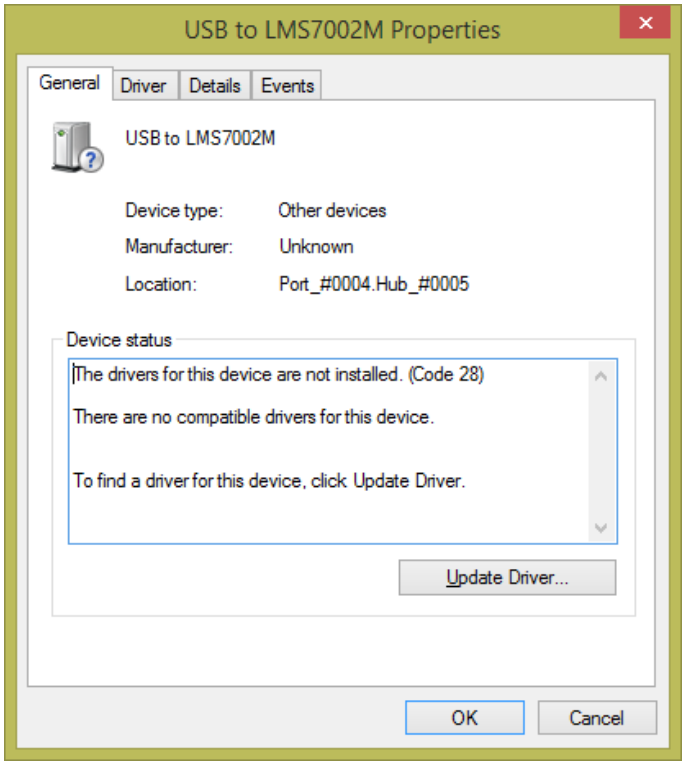

Figure 4 Device properties

5. Select **Browse my computer for driver software,** locate the driver provided with UNITE7002 board and press **Next** *Figure 5*

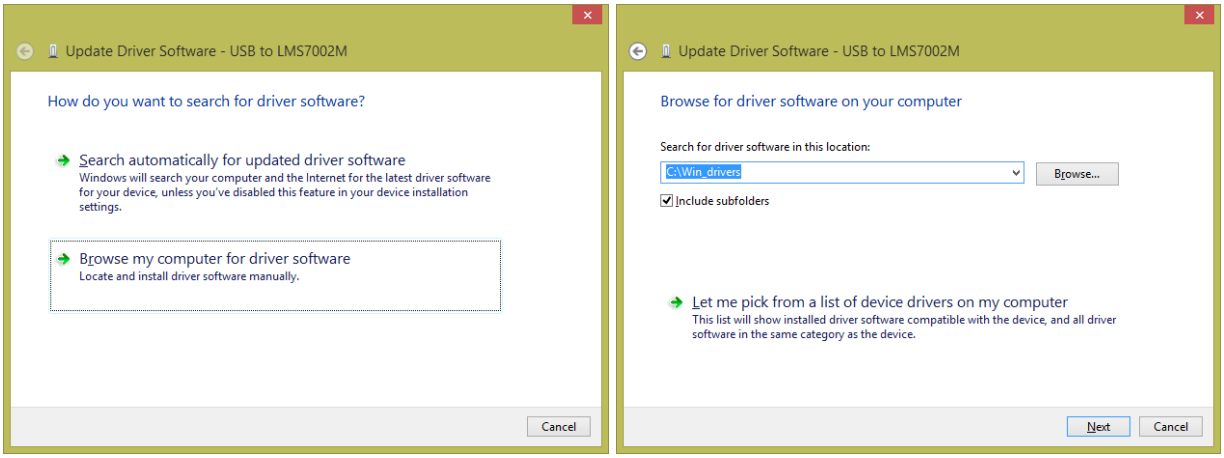

Figure 5 Update Driver Wizard.

6. If the **Windows Security** window appears, select **Install this driver software anyway** *Figure 6*

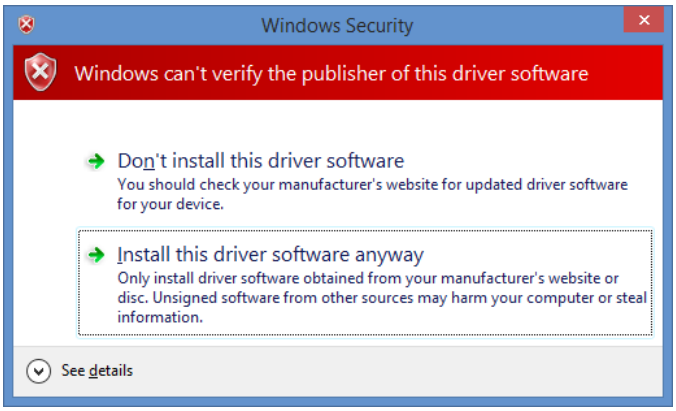

Figure 6 Hardware wizard. Install driver manually

Windows should proceed to install drivers at this stage. Generally, once the above steps have been taken for the UNITE7002, these steps do not need to be repeated.

IMPORTANT:
Before running the control software, unplug then plug your device back into your computer.

4.3 Determining Serial Port

After driver installation, Windows will assign to your UNITE7002 board a serial port. To check your board serial port number, please follow these steps:

1. Go to **Control Panel > System > Device Manager**

2. Locate **USB Virtual Serial Port** under **Ports (COM & LPT)**

Note that in this system example it has enumerated as COM3 *Figure 7*.

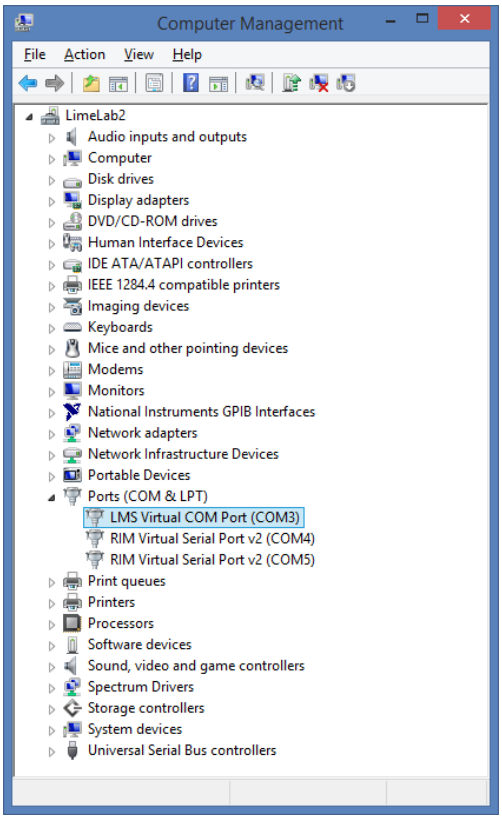

Figure 7 Check for new communication port

NOTE: If you are using Windows 7 64 bit OS, you must disable **Driver Signature Enforcement.** To do this, Restart you PC, press F8 at startup and choose **Disable Driver Signature Enforcement**. This step is required to done once.

NOTE: If you are using Windows 8 or later, to disable driver signature enforcement manual can be found in this [link].

4.4 Linux Setup

For Linux users, there is no need to install USB drivers, as the system will assign drivers automatically once the UNITE7002 board is connected to PC.

To determine port number the easiest is via the command line and type command:

```
$ setserial -g /dev/ttyS[0123]
```

4.5 Starting LMS 7 Suite Software

Apply +5V to the board and start 'LMS 7 Suite' software. The application must be run under administrator privileges. To do that, right click on the 'LMS 7 Suite' icon and select **Run as an Administrator**. This will provide administrator privileges, which are required for UNITE7002 board communication via USB.

4.6 Connecting

Once the Windows driver is installed and the control software has been lunched, click on **Options>Connection Settings.** The **Connection Setting** windows will pop-up *Figure 8*.

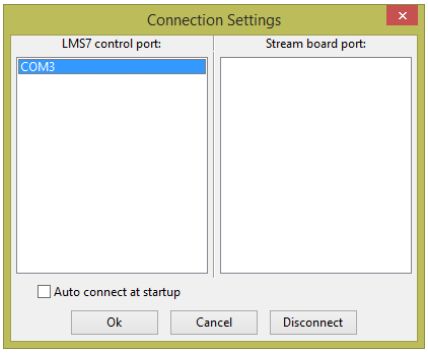

Figure 8 GUI communication settings.

Select the dedicated USB port number of the EVB board. In this case, it is COM3, and press OK.

The GUI device name and firmware version will appear in the bottom *Figure 9*, once connection with the board is established.

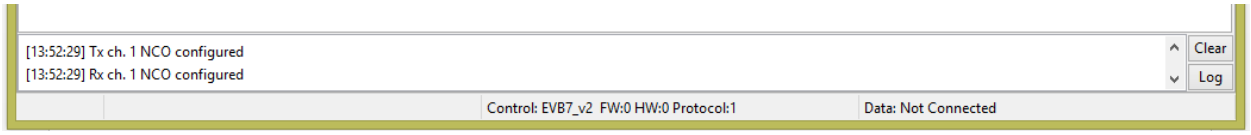

Figure 9 GUI detected device and firmware version

5

Getting started with the UNITE7002

5.1 Introduction to using the UNITE7002

The UNITE7002 allows powerful demonstrations of the LMS7002M transceiver. In this quick start guide, we demonstrate the board operating with analogue inputs and outputs. The Lime "Stream" board is used to demonstrate the board operating with digital inputs and outputs.

Section *5.2* describes the set up of the transmitter, with section *0* describing how to set up the SXT (TX PLL) and section *0* describing how to set up the TX analogue baseband and RF tabs of the LMS 7 Suite. Section *5.4* describes the set up of the transceiver for basic tests, with section *5.4.1* describing how to set up the SXR (RX PLL) and section *0* and *5.4.3* describing how to set up the RX analogue baseband and RF tabs of the LMS 7 Suite.

The analogue quick start demonstration assumes the user has all the equipment listed in Appendix *8.2*. Users with less equipment can use the set up of Section *5.6*.

5.2 Transmitter Setup and Basic Testing

To test the Tx path, the Keysight (formerly Agilent) MXG N5182A generator is used as an external baseband source. This is connected to the Tx path via the analog inputs and generates a WCDMA modulation signal at socket X1 (TX1_A) as shown in *Figure 10*. To generator settings are described in section *8.3* (Appendix A).

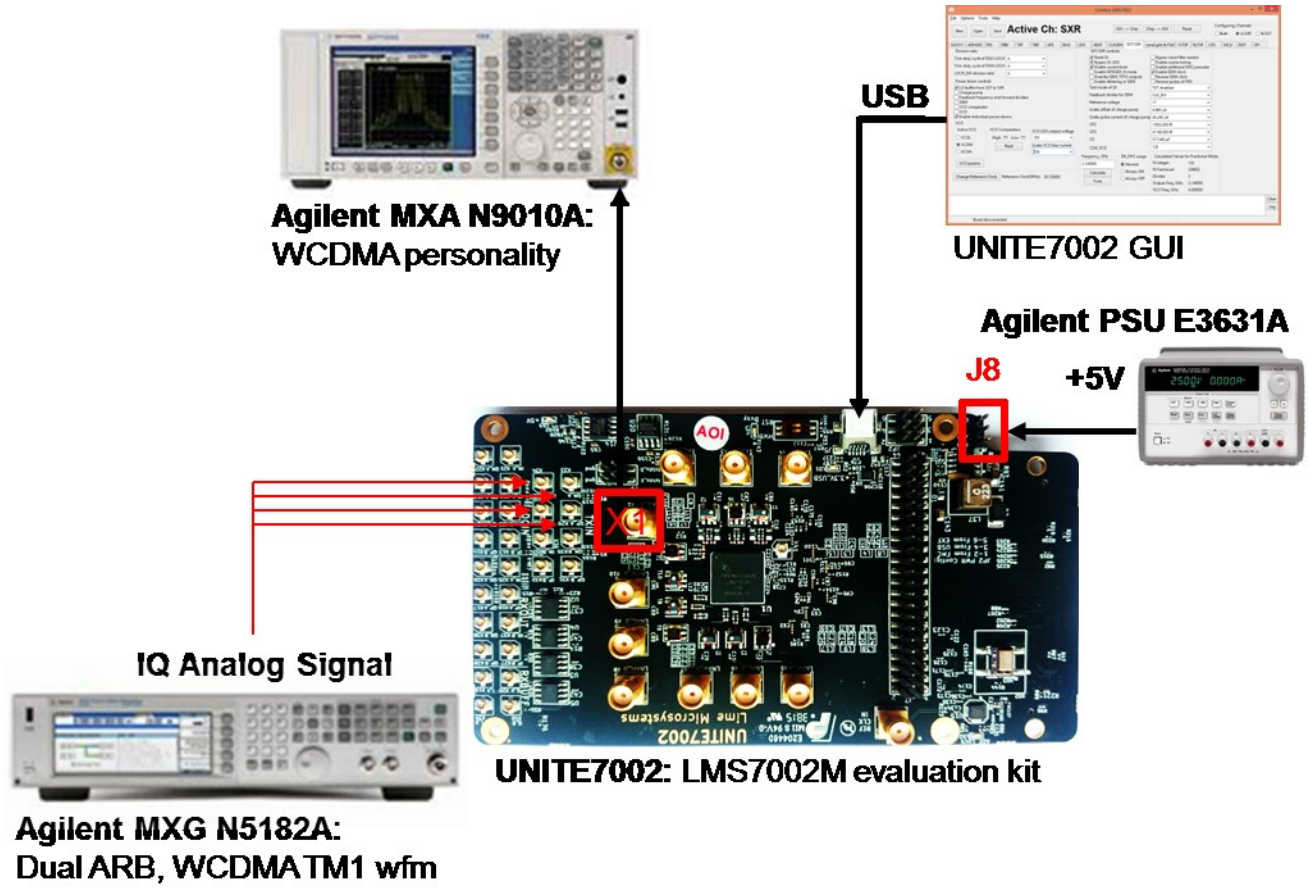

Figure 10 Tx Test Setup

5.2.1. SXT/SXR tab setup

After power up, connect the GUI to the board and select the **SXT/SXR** tab. To configure the Tx LO to 2140 MHz, do the following:

1. Select the **B/SXT** in the configuration channels window to control TxPLL
2. Enable Tx PLL **VCO** (Deselect)
3. Type the wanted frequency in **Frequency, GHz** box. In this case, 2140 MHz
4. Press **Calculate** followed by **Tune**

See *Figure 11* below to check selections.

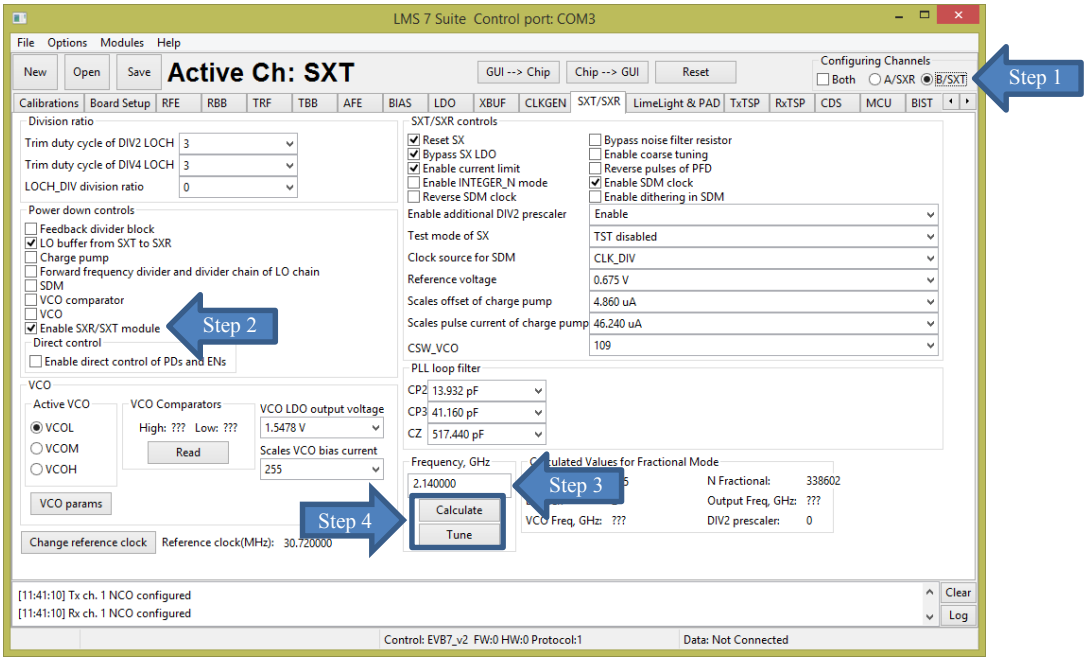

Figure 11 SXT register setup procedure

5.2.2. TRF tab setup

The TRF tab controls the TX RF gain and output path. By default the Tx RF gain is set to maximum (**TXPAD gain control** set to '0') and **TXFE output selection** set to **Band 1** (to X1 on UNITE7002 board) as the output path. For this test, we are not going to change these settings.

5.2.3. TBB tab setup

In the **TBB** tab the baseband gain and filter bandwidth are controlled. Follow the instructions below set up TBB:

1. Select the **A/SXR** to control channel A
2. **Enabled Tx IQ analog input** path **to current amplifier**
3. Set **Frontend gain** to your wanted
4. Configure the base band filter settings. By default, high band filter (**LPFH_TBB**) is power on

See *Figure 12* below to check selections.

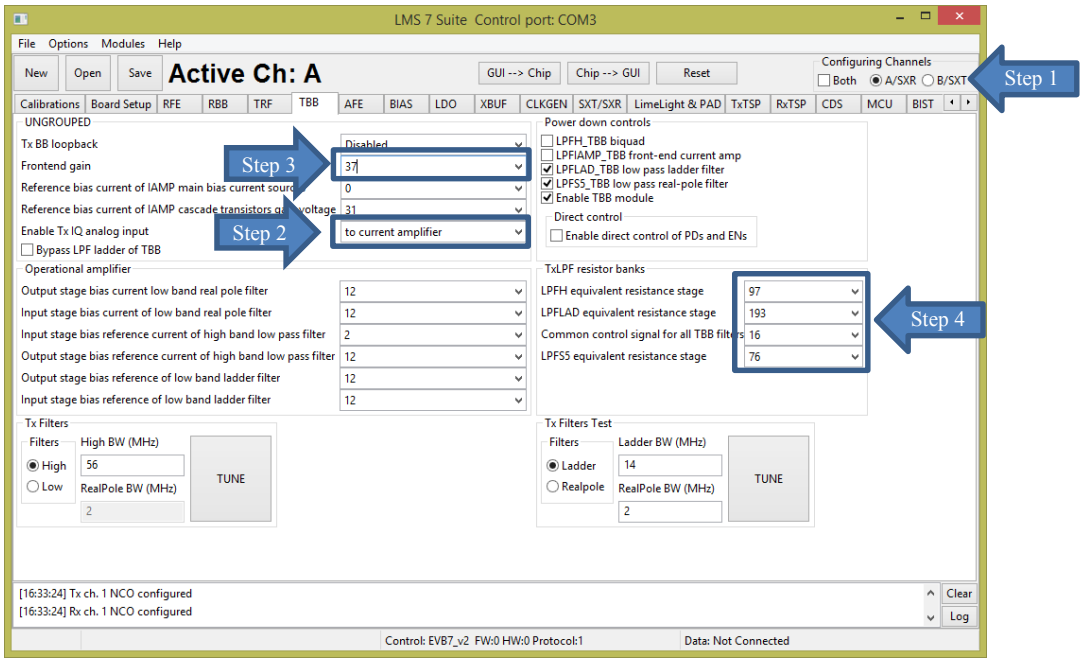

Figure 12 TBB register setup procedure

Note: the register preset file for Tx test *'TX_2140_MHz_demo_setup.ini'* is supplied with design kit. You can load it by clicking menu button **Open>>** locate and select the file in ../**LMS7GUI** folder/ ***'TX_2140_MHz_demo_setup.ini'*** >> select **Open,** followed by **GUI--> Chip** button. The select **SXT/SXR** tab and retune synthesizer.

5.3 Testing the TX Output

When the transmitter is configured as shown in section *5.2*, the TX1_A output (socket X1) can be connected to a spectrum analyzer (SA). With the SA you can now observe the results of this basic operational test *Figure 13*. The test is looking at the DC offset from the un-programmed data DAC as LO leakage and the example shown below is measuring a value of -26.8 dBm.

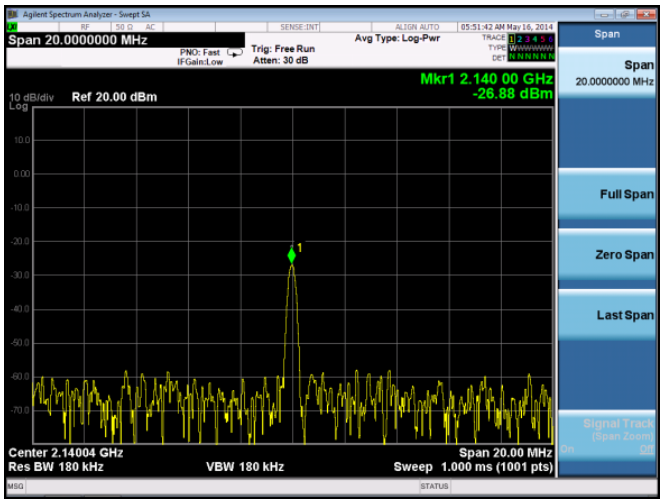

Figure 13 Basic TX testing using DC offset resulting in LO leakage

When the baseband is enabled, the WCDMA modulation can be tested and the results of *Figure **14*** can be obtained with the MXG Spectrum Analyser.

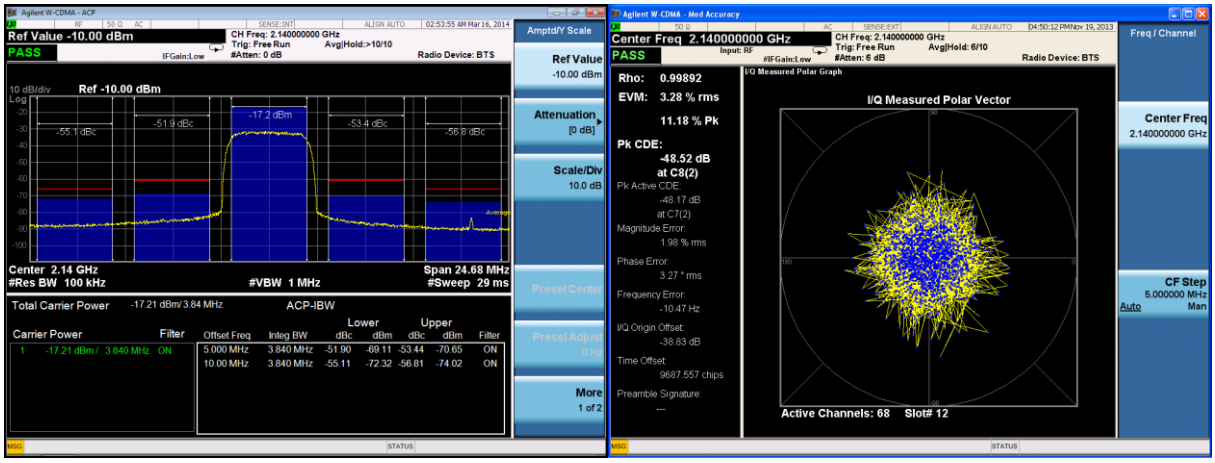

Figure 14 Basic TX testing using WCDMA modulation

5.3.1. TX Basic Operation Checks

To check the basic TX frequency and gain control, conduct some tests changing frequencies and gain settings. The following tests are recommended:

TRF – TXPAD gain change setting from 0 to 31 and observe results. LO should vary by approx. 1 dB steps, 31dB range.
Change frequency from 2.14 GHz to 2.11 GHz and press '**Calculate'/'Tune'** (CAP value should change), check the Spectrum Analyzer.
Change frequency from 2.11 GHz to 2.17 GHz and press '**Calculate'/'Tune'** (CAP value should change), check the Spectrum Analyzer.

5.4 Receiver Setup and Basic Testing

The test bench for the receiver is shown in *Figure 15*. Basic functionality checks on the receiver side are achieved by using the Analog output from connector X20.

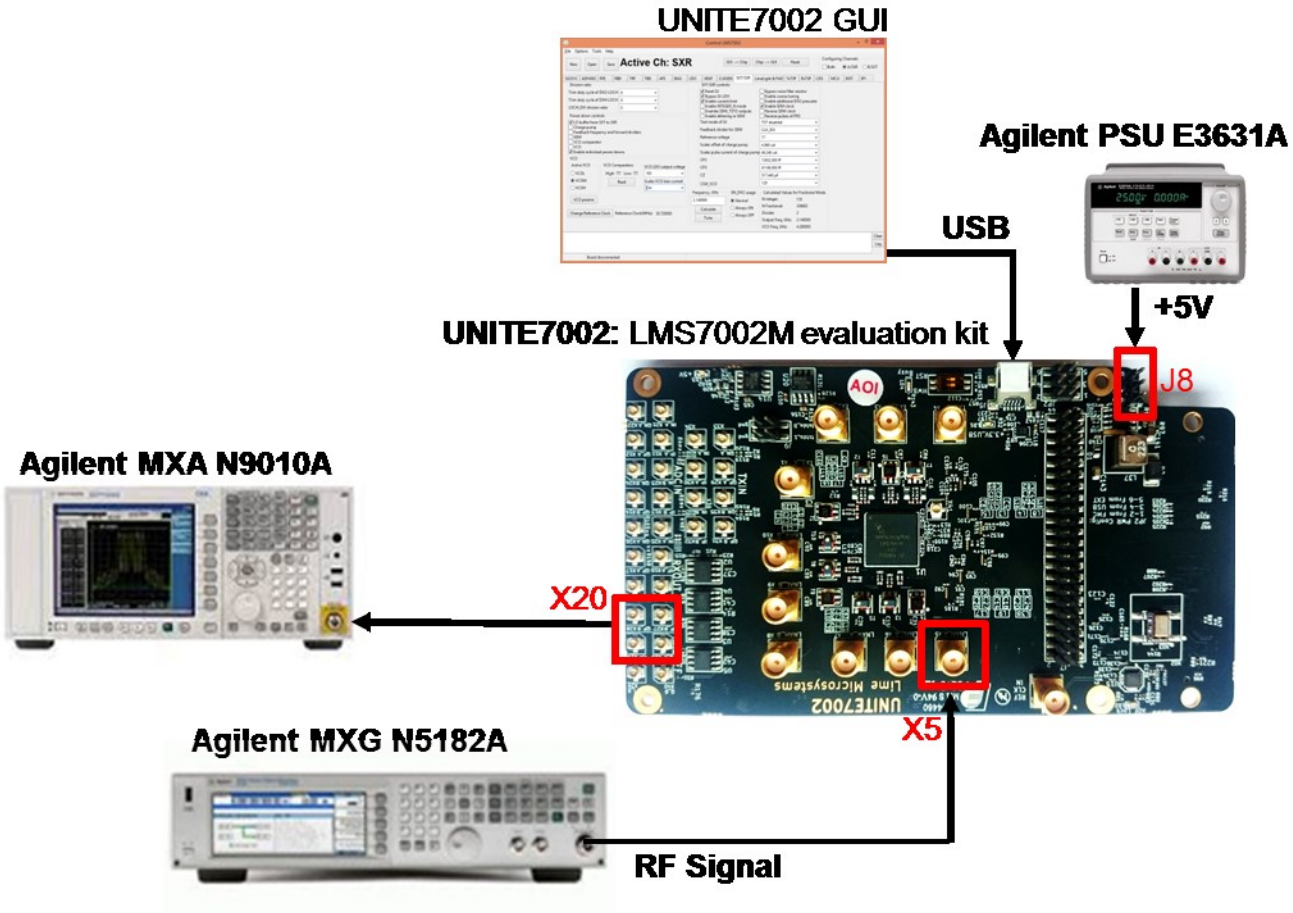

Figure 15 Rx Test Setup

5.4.1. SXT/SXR tab setup

Select the **SXT/SXR** tab. To configure the Rx LO to 1950 MHz, do the following:

1. Select the **A/SXR** in the configuration channels window to control RxPLL
2. Enable Rx PLL **VCO** (Deselect).
3. Type the wanted frequency in **Frequency, GHz** box. In this case, 1950 MHz.
4. Press **Calculate** followed by **Tune**.

See *Figure 16* below to check selections.

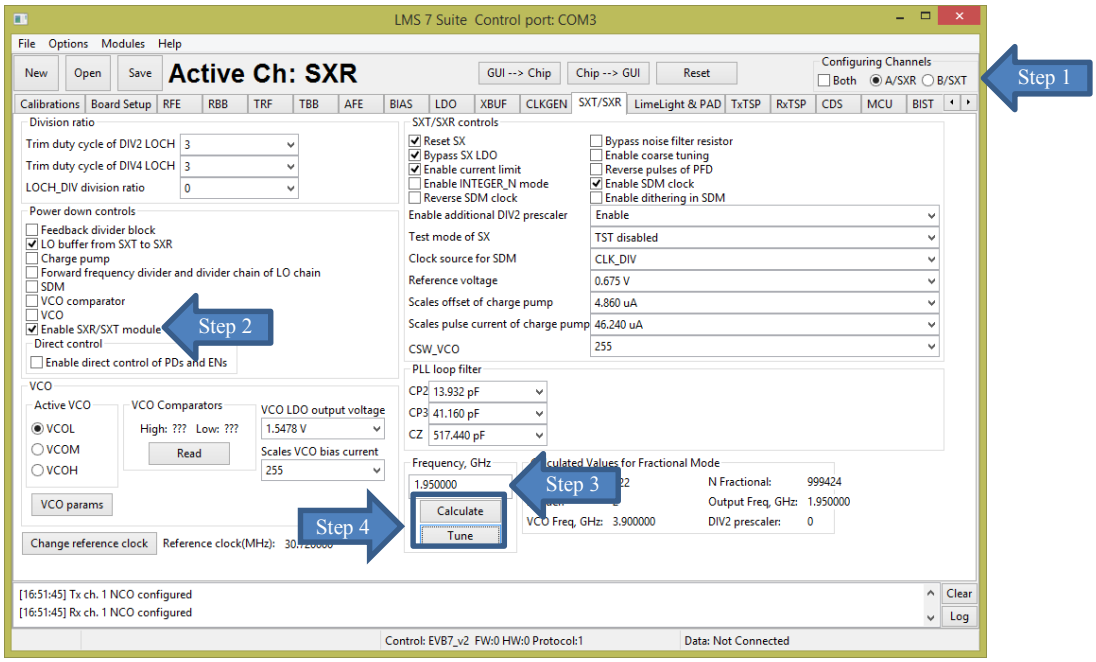

Figure 16 SXR register setup procedure

5.4.2. RFE tab setup

Select the RFE tab to configure the receiver RF front–end. Follow the configuration steps below:

1. Enable **LNA_RFE**, **RXFE mixer LO buffer** and **RFFE Quadrature LO generator**.
2. Select **Active path to the RXFE**. Select **LNAH** for this test. The LNAH is a default setting.
3. The **LNA** and **TIA** gain are preset to maximum.

See *Figure 17* below to check selections.

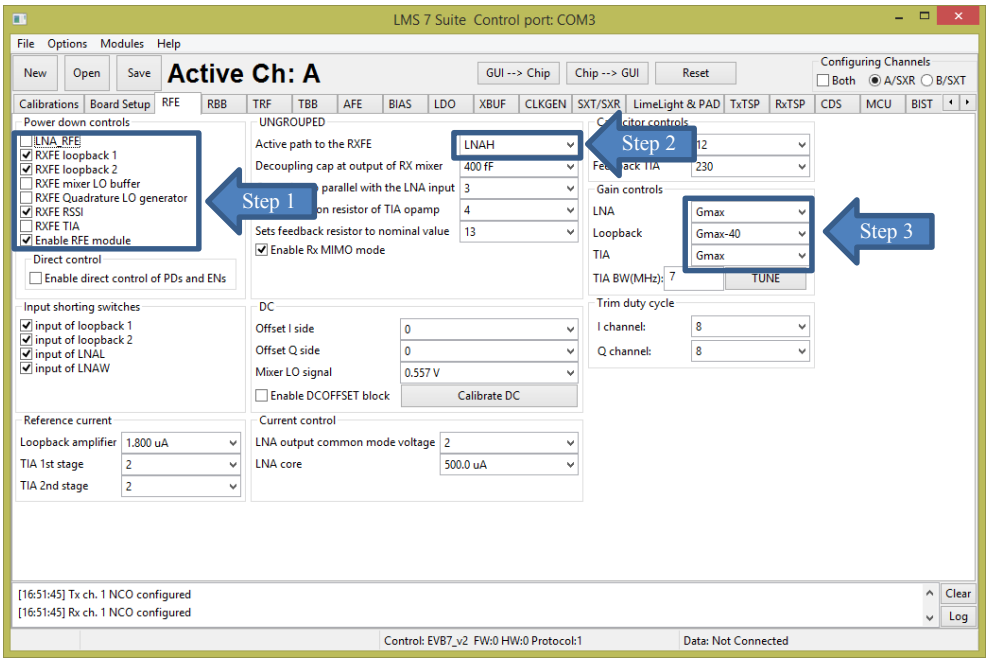

Figure 17 SXR register setup procedure

5.4.3. RBB tab setup

Select the TBB tab to configure the PGA gain and baseband filter bandwidths. Follow the configuration steps below:

1. Select PGA output to **output pads**. This selection enables receiver analog outputs
2. Set **PGA gain** to 19 dB
3. Configure filter bandwidth. By default the LPFL is selected

See *Figure 18* below to check selections.

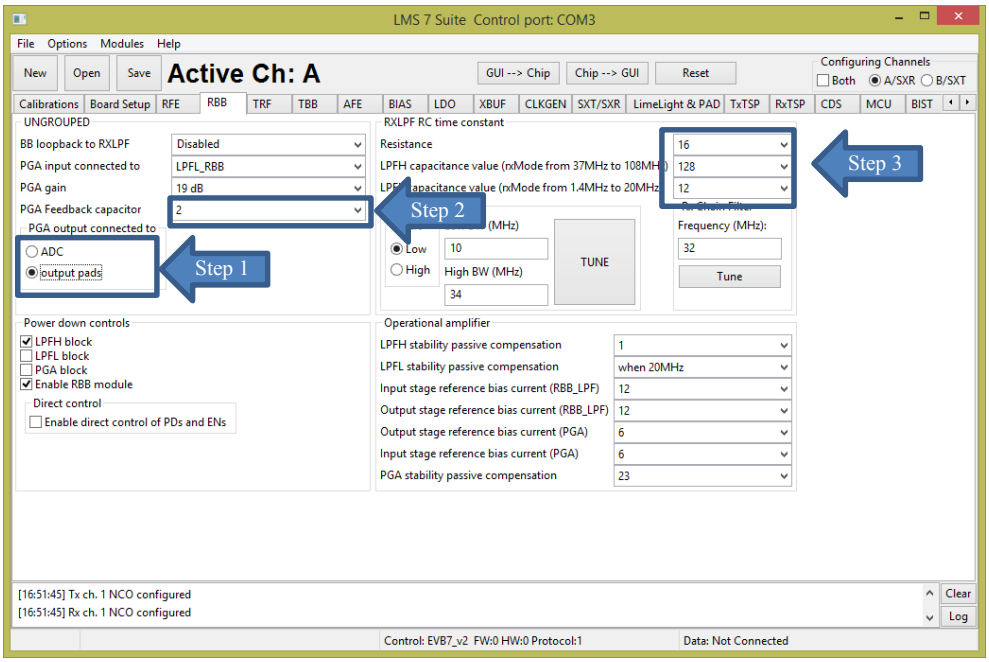

Figure 18 SXR register setup procedure

Note: the register preset file for Rx test *'RX_1950MHz_demo_setup.ini'* is supplied with design kit. You can load it by clicking menu button **Open>>** locate and select the file in ./**LMS7GUI** folder/ ***'RX_1950MHz_demo_setup.ini'*** >> select **Open,** followed by **GUI--> Chip** button. The select **SXT/SXR** tab and retune synthesizer.

5.5 Testing the RX Output

Set the signal generator to 1955 MHz (i.e. 5 MHz offset from PLL frequency selected) and input a sine wave at -70 dBm into the evaluation board antenna connector (LNAH_A, connector X4). Configure the receiver as showed in section *0*. Connect an Analyser to X20 or X19. If everything is correctly setup, you should see the 1 MHz peak. See *Figure 19* below.

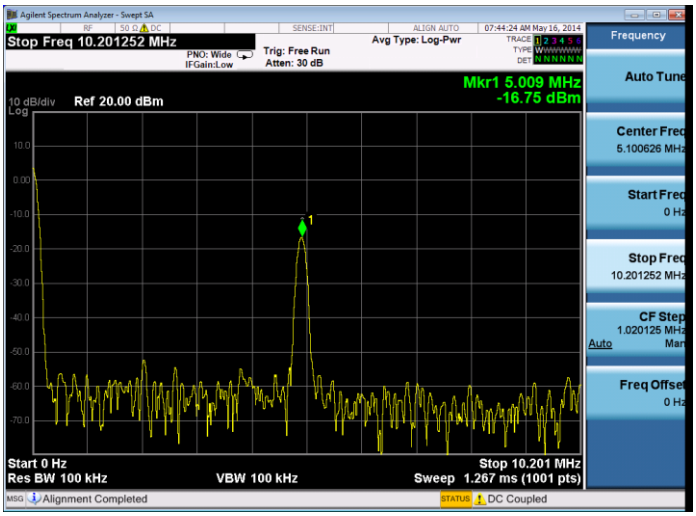

Figure 19 RX analog output on Spectrum Analyser.

5.5.1. RX Basic Operation Checks

To check the basic Rx frequency and gain control, conduct some tests changing frequencies and gain settings. The following six tests are recommended:

a. RBB – change PGA gain setting from 19 dB to -12 dB, observe results, gain should decrease
b. RFE – change TIA gain settings from Gmax to Gmin, observe results, gain should decrease
c. RFE – LNA gain change from Gmax to Gmax -30, observe results, gain should decrease
d. Change frequency from 1.95 GHz to 1.92 GHz and press '**Calculate'/'Tune'**. Change Signal Generator to 1.925 GHz (1 MHz offset from PLL). Observe results
e. Change frequency from 1.92 GHz to 1.98 GHz and press '**Calculate'/'Tune'**. Change Signal Generator to 1.985 GHz (1 MHz offset from PLL). Observe results

5.6 Testing With Minimal Equipment

For users without all the equipment specified in section *8.2* (Appendix A) it is possible to link the TX1_A output (X1) to the receiver input LNAH_A input (X4) and rely on the LO leakage to provide an input signal to the RX.

Using the methods of section *5.2* and section *5.4* set the SXT to 2140 MHz and SXR to 2145 MHz and measure a 5 MHz signal with an oscilloscope to observe the RXI output at X19. The magnitude of the output signal can be controlled with the various gain controls in the RFE and TRF.

6

UNITE7002 Connectors and Options

6.1 Introduction to the UNITE7002 Connectors and Options

Section *6.2* describes the various connectors available on the UNITE7002. Section *6.3* describes the hardware options available on the UNITE7002, including reference clocks and the SPI control. The top and bottom of the board are shown in *Figure 20* and Figure *21* respectively.

6.2 Board Connections

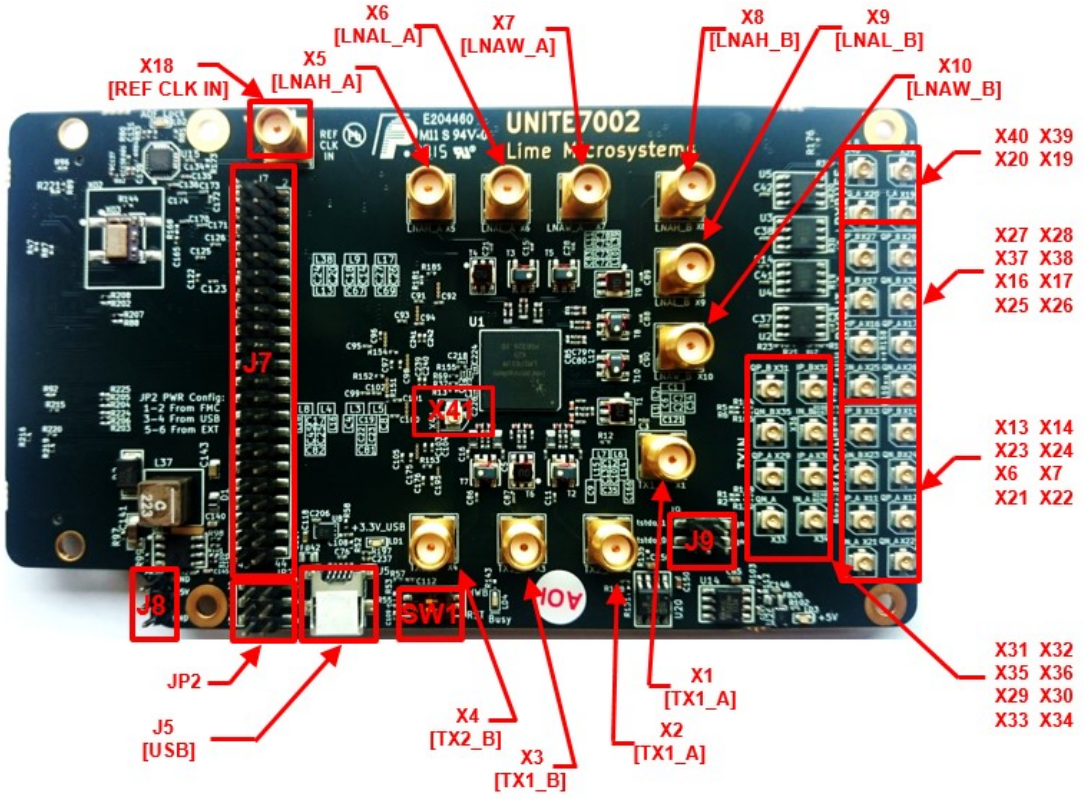

Figure 20 Design kit connection descriptions, Top view.

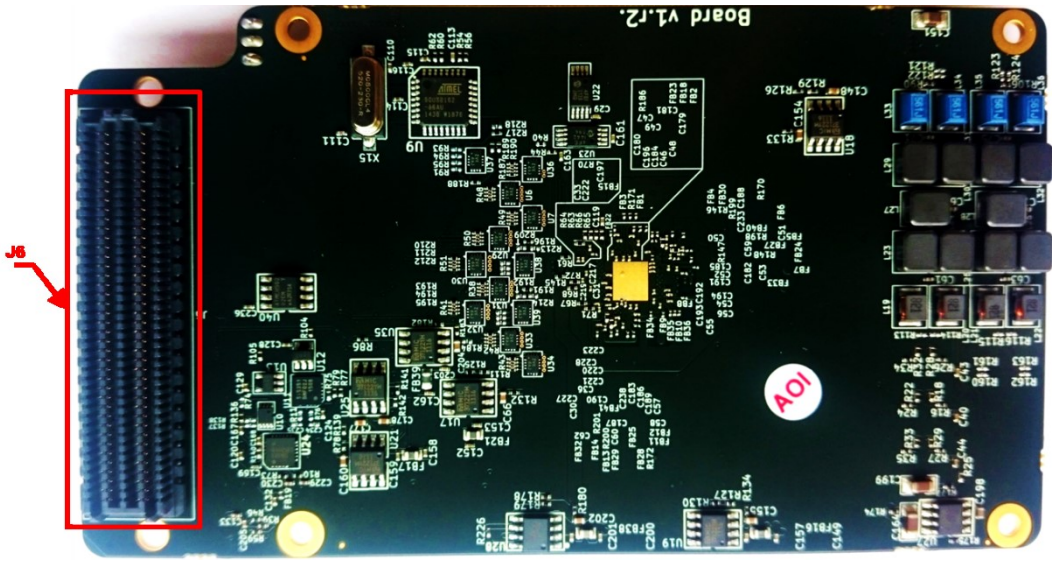

Figure 21 Design connection descriptions, Bottom view.

Table 1 describes the high level pin assignment for each connector on the design kit.

Table 1 Design kit connectors and switches

Connector	Schematic name	Description
JP2	+5V Power Supply Jumper	This jumper enables the choose what power supply is used. Selection can be from laboratory power supply (via J8) or USB (via J5) or FPGA development kit (via J6). For FPGA selection U16 is a voltage regulator that converts +12 V to +5 V
J5	USB	USB Connector to PC
J6	FMC	The FMC (HPC) is a standard connector used to interface the Lime board directly to an FPGA design kit. The signal pin description is shown in *6.2.1* section.
J7	Digital I/O Connector	This connector provides access to externally buffered, LMS70002M digital interface and SPI interface. Signal pin description showed in *6.2.2* section.
J8	+5V Power Supply	+5 V supply connector
J9	ATP	Analog Test Point
X41	TP	Test Point
X1	TX1_A	Transmitter TX1 output, channel A. Wideband transmitter output
X2	TX2_A	Transmitter TX2 output, channel A. Lower bands transmitter output

X3	TX1_B	Transmitter TX1 output, channel B. Wideband transmitter output
X4	TX2_B	Transmitter TX2 output, channel B. Lower bands transmitter output
X5	LNAH_A	Receiver LNA_H input, channel A. Higher bands receiver input
X6	LNAL_A	Receiver LNA_L input, channel A. Lower bands receiver input
X7	LNAW_A	Receiver LNA_W input, channel A. Wideband receiver input
X8	LNAH_B	Receiver LNA_H input, channel B. Higher bands receiver input
X9	LNAL_B	Receiver LNA_L input, channel B. Lower bands receiver input
X10	LNAW_B	Receiver LNA_W input, channel B. Wideband receiver input
X18	REF CLK I/O	Reference clock input used to synchronize test equipment with UNITE7002 board to calibrate frequency error. A 10 MHz reference from the test equipment connects to X18 connector.
X19, X20, X39, X40	RXBUFFI/Q	Receiver analog single-ended outputs
X16, X17, X25-X28, X37, X38	RXOUTI/Q	Receiver analog differential outputs
X6, X7, X21-X23, X13, X14	ADCINI/Q	Receiver analog differential inputs
X29-X36	TXINI/Q	Transmitter analog differential inputs
SW1	U9 Reset	Switch to reset AT90USB162-16U and load new software. By default set to off

6.2.1. FMC connector pin description

The digital baseband interface can be established via the FMC connector J6. The signal pin description is shown in *Table 2*.

Note: FMC HPC connector has 400 pins, but not all pins are used. Some pins are not connected and some are connected to GND. Please refer to UNITE7002 schematic for more details.

Table 2 FMC connector signal pin description

Pin number	Schematic name	Function
D8	SyntCLK1	Clock Out, CMOS
D9	SyntCLK2	Clock Out, CMOS
H7	IQSEL2_DIR	IQSEL direction control for port 2. If '1' – input, '0' – output
H8	DIO_DIR_CTRL1	Data direction control for port 2. If '1' – input, '0' – output
G9	SDIO	Serial port data in/out, CMOS
G10	DIG_RST	
H10	INTR	I2C port interrupt line, CMOS
H11	SCLK	Serial port clock, positive edge sensitive, CMOS
H13	RXFCLK	Clock from BBIC to RFIC during JESD207 mode, Port 2
H14	RXEN	RX hard power off
G12	RXMCLK	Clock from RFIC to BBIC during JESD207 mode, Port 2
G13	RXIQSEL	IQ flag in RXTXIQ mode enable flag in JESD207 mode, Port 2
D14	RESET	Hardware reset, active low, CMOS
D15	IQSEL1_DIR	IQSEL direction control for port 1. If '1' – input, '0' – output.
C14	SDO	Serial port data out, CMOS
C15	DIO_DIR_CTRL2	Data direction control for port 1. If '1' – input, '0' – output.
H16	RXD11	DIQ bus, bit 11, Port 2
H17	RXD8	DIQ bus, bit 8, Port 2
G15	TXNRX1	LimeLight protocol control
G16	RXD10	DIQ bus, bit 10, Port 2
D17	SAEN	Serial port A enable, active low, CMOS
H19	RXD7	DIQ bus, bit 7, Port 2
H20	RXD4	DIQ bus, bit 4, Port 2
G18	RXD9	DIQ bus, bit 9, Port 2
G19	RXD6	DIQ bus, bit 6, Port 2
H22	RXD3	DIQ bus, bit 3, Port 2
H23	RXD2	DIQ bus, bit 2, Port 2
G21	TXNRX2	LimeLight protocol control
G22	RXD5	DIQ bus, bit 5, Port 2
H25	TXMCLK	Clock from RFIC to BBIC during JESD207 mode, Port 1
H26	TXIQSEL	IQ flag in RXTXIQ mode enable flag in JESD207 mode, Port 1
G24	RXD0	DIQ bus, bit 0, Port 2
G25	RXD1	DIQ bus, bit 1, Port 2
D24	SBEN	Serial port B enable, active low, CMOS

H28	TXFCLK	Clock from BBIC to RFIC during JESD207 mode, Port 1
H29	TXD10	DIQ bus, bit 10, Port 1
G27	TXEN	TX hard power off
G28	TXD11	DIQ bus, bit 11, Port 1
H31	TXD8	DIQ bus, bit 8, Port 1
H32	TXD6	DIQ bus, bit 6, Port 1
G30	TXD9	DIQ bus, bit 9, Port 1
G31	TXD7	DIQ bus, bit 7, Port 1
H35	TXD4	DIQ bus, bit 4, Port 1
G33	TXD5	DIQ bus, bit 5, Port 1
H37	TXD2	DIQ bus, bit 2, Port 1
H38	TXD0	DIQ bus, bit 0, Port 1
G36	TXD3	DIQ bus, bit 3, Port 1
G37	TXD1	DIQ bus, bit 1, Port 1
F10	G_PWR_DWN	
F11	DIO_BUFF_OE	DIO port buffer enable/disable. If '1' – disable, '0' – enable.
C31	SDA	I2C port data line, CMOS
C30	SCL	I2C port clock line, CMOS
D12	RSSI_ADC0	Analog test point
C10	RSSI_ADC1	Analog test point

6.2.2. Digital I/O connector pin description

The DIO card can be connected to UNITE7002 via Digitail I/O connector J7. Connectr has 44 pins. The pin description showed in the *Table 3*.

Table 3 Digital I/O connector pin description

Pin number	Schematic name	Function
1	TXD0	DIQ bus, bit 0, Port 1
2	TXD1	DIQ bus, bit 1, Port 1
3	TXD2	DIQ bus, bit 2, Port 1
4	TXD3	DIQ bus, bit 3, Port 1
5	TXD4	DIQ bus, bit 4, Port 1
6	TXD5	DIQ bus, bit 5, Port 1
7	TXD6	DIQ bus, bit 6, Port 1
8	TXD7	DIQ bus, bit 7, Port 1
9	TXD8	DIQ bus, bit 8, Port 1
10	TXD9	DIQ bus, bit 9, Port 1
11	TXD10	DIQ bus, bit 10, Port 1
12	TXD11	DIQ bus, bit 11, Port 1
13	TXFCLK	Clock from BBIC to RFIC during JESD207 mode, Port 1
14	SyntCLK2	Clock Out, CMOS.
15	VDIO	+3.3V supply

16	TXIQSEL	IQ flag in RXTXIQ mode enable flag in JESD207 mode, Port 1
17	TXMCLK	Clock from RFIC to BBIC during JESD207 mode, Port 1
18	TXEN	TX hard power off
19	GND	GND
20	GND	GND
21	RXD0	DIQ bus, bit 0, Port 2
22	RXD1	DIQ bus, bit 1, Port 2
23	RXD2	DIQ bus, bit 2, Port 2
24	RXD3	DIQ bus, bit 3, Port 2
25	RXD4	DIQ bus, bit 4, Port 2
26	RXD5	DIQ bus, bit 5, Port 2
27	RXD6	DIQ bus, bit 6, Port 2
28	RXD7	DIQ bus, bit 7, Port 2
29	RXD8	DIQ bus, bit 8, Port 2
30	RXD9	DIQ bus, bit 9, Port 2
31	RXD10	DIQ bus, bit 10, Port 2
32	RXD11	DIQ bus, bit 11, Port 2
33	TXNRX1	LimeLight protocol control
34	SynCLK1	Clock Out, CMOS
35	RXFCLK	Clock from BBIC to RFIC during JESD207 mode, Port 2
36	RXIQSEL	IQ flag in RXTXIQ mode enable flag in JESD207 mode, Port 2
37	RXMCLK	Clock from RFIC to BBIC during JESD207 mode, Port 2
38	RXEN	RX hard power off
39	TXNRX2	LimeLight protocol control
40	SAEN	Serial port A enable, active low, CMOS
41	SCLK	Serial port clock, positive edge sensitive, CMOS
42	SDIO	Serial port data in/out, CMOS
43	SDO	Serial port data out, CMOS
44	RESET	Hardware reset, active low, CMOS

6.3 Hardware options

This section describes the configuration options and set up procedures for:

- TCXO's and data clocks distribution
- UNITE7002 Synchronization
- SPI connection options

The board is shipped with the default mode which means a basic operation using an external digital I/O source via the FMC connector. Various configurations are available depending on the system requirements for development work. The configurations are summarized and the following sections describe the board modifications required to achieve these configurations.

6.3.1. TCXO's Configuration

The LMS7002M device provides a flexible clocking scheme which allows the PLL reference clock and digital interface clock to be independently clocked. In addition, the digital interface clock can be generated internally in LMS7002M.

The UNITE7002 board is shipped with a 30.72 MHz TCXO. In order to meet the demanding phase noise specifications of the various standards, Lime Microsystems has worked with Rakon to develop a new part, called E6245LF that enables the board to meet the required specifications. This new part come with the board.

The board can accept three different types of TCXO's as described in *Table 4*.

Table 4 TCXO Configurations

Size	Reference number	Part Number	Description
14.7 x 9.2	XO2	E5405LF	61.44 MHz Crystal oscillator, used in combination with divider /2 (U10) for performance improvements
7 x 5 (4pin)	XO1	E5280LF	30.72 MHz crystal shipped with the board as a default
7 x 5 (6pin)	XO3	E6245LF	30.72 MHz high performance crystal oscillator.

6.3.2. UNITE7002 synchronization

The LMS7002M board provides options to synchronize the on-board TCXO with the base band or test equipment systems. To do that, connect a 10 MHz reference clock generated by the test equipment to UNITE7002 board X18 SMA connector. Program the on-board PLL via the GUI ADF4002 page. When the board is synchronized the LED 'ADF Lock' (LD2) will illumine.

A board that is synchronized with the test equipment or any other RF device will not have frequency error.

6.3.3. SPI Control Configuration

The LMS7002M SPI interface is controlled from a USB connection by default. The SPI interface can also be controlled from baseband interface connectors J6 and J7. Please note only one SPI master can be connected to the bus at the time.

If the SPI is controlled via the baseband connector J6 do not connect either a USB cable to J5 nor J7 connector. This removes any possible bus contention. Please note that NF denotes component is Not Fitted.

Table 5 SPI Control Options

SPI control		
Configuration	**DEFAULT MODE USB connector or baseband connector J7**	**SPI controlled via J6 baseband connector**
Description / Component	**SPI controlled via USB or J7 connector**	**SPI connected to BB via connector J6 FMC**
R91	NF	0R
R92	NF	0R
R93	NF	0R
R94	NF	0R
R95	NF	0R
R96	NF	0R

All of these components are located on the underside of the board.

Note. The USB interface must be left disconnected when the external SPI control is being used to prevent bus contention. Additionally the components R91 – R96 should be fitted as listed in *Table 5*.

6.3.4. Baseband Digital Interface Voltage

The default digital interface voltage is 3.3 V. It can be adjusted by changing R183 to the values listed in *Table 6*.

Table 6 Digital IO Voltage Control

R183	Interface Voltage
0.8 k	1.8 V
1.5 k	2.5 V
2.32 k	3.3 V

6.3.5. UNITE7002 Matching networks

The matching networks that are fitted to UNITE7002 at manufacture are listed in *Table 7*.

Table 7 Default bands matched to UNITE7002

Connector	Schematic name	Matching network
X1, X42	TX1_A	Broadband from 10 – 6000 MHz, using TCM1-63AX+ Balun
X2, X43	TX2_A	Broadband from 4.5 – 3000 MHz, using TC1-1-13MA+ Balun
X3, X44	LNAL_A	Broadband from 4.5 – 3000 MHz, using TC1-1-13MA+ Balun
X4, X45	LNAH_A	Broadband from 10 – 6000 MHz, using TCM1-63AX+ Balun
X5, X46	LNAW_A	Broadband from 10 – 6000 MHz, using TCM1-63AX+ Balun
X8, X47	TX1_B	Broadband from 10 – 6000 MHz, using TCM1-63AX+ Balun
X9, X48	TX2_B	Broadband from 4.5 – 3000 MHz, using TC1-1-13MA+ Balun
X10, X49	LNAL_B	Broadband from 4.5 – 3000 MHz, using TC1-1-13MA+ Balun
X11, X50	LNAH_B	Broadband from 10 – 6000 MHz, using TCM1-63AX+ Balun
X12, X51	LNAW_B	Broadband from 10 – 6000 MHz, using TCM1-63AX+ Balun

7

Detailed Guide to LMS 7 Suite

7.1 LMS 7 Suite – Software Description

This section describes the LMS 7 Suite software GUI and each of the menus, buttons and embedded controls. Most of the pages in the tool corresponds to the top level sections of the SPI programming map, with the exception of the 'Board Setup' and the 'SPI' page.

7.2 LMS 7 Suite – Window Panels.

The 'LMS 7 Suite' GUI is comprised in three main pieces: GUI control panel, LMS7002M register and UNITE7002 board configuration panel, and LOG panel. These are shown in *Figure 22*.

7.2.1. GUI Control panel

GUI Control panel includes menu bar and various control buttons for controlling the software. These will be described in detail in section . The GUI control panel is shown in *Figure 23*.

7.2.2. Configuration panel

Configuration panel controls the LMS7002M registers and some evaluation board setup and is shown in *Figure 24*.

Each configuration panel has specific register control on internal LMS7002M blocks. There are 17 different configuration panels for controlling the LMS7002M chip and 2 for controlling other devices on the UNITE7002. Every control of the panel is described in sections *7.4* to *7.22*.

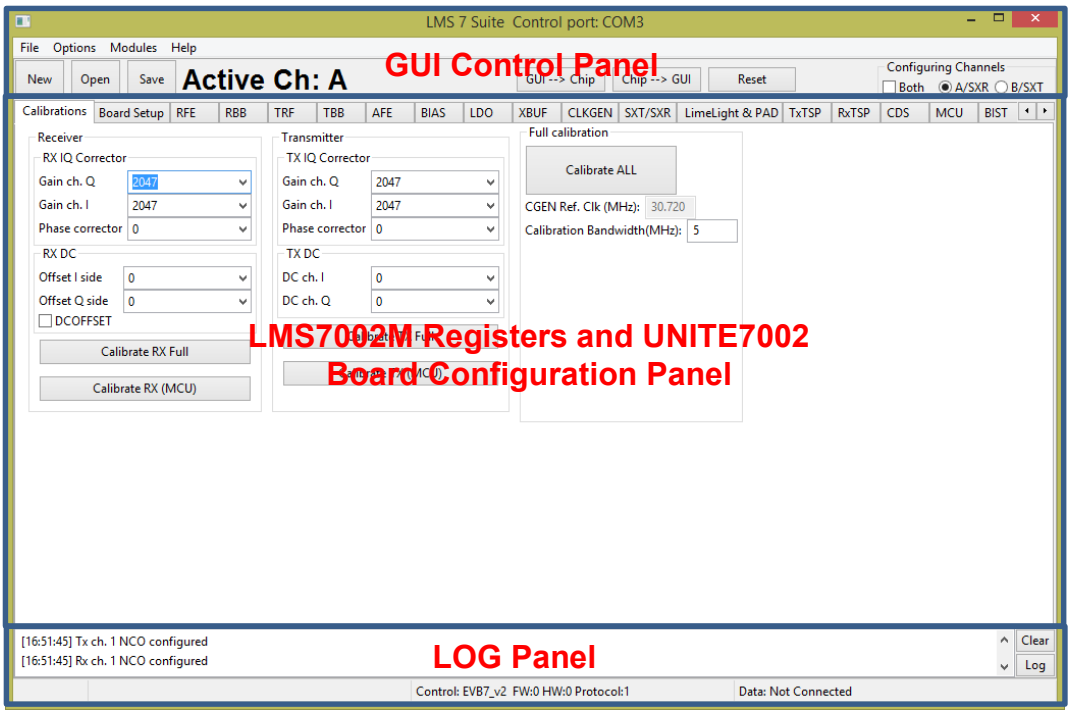

Figure 22 GUI window diagram

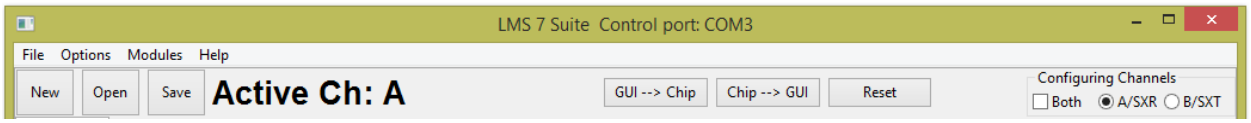

Figure 23 GUI Control Panel window

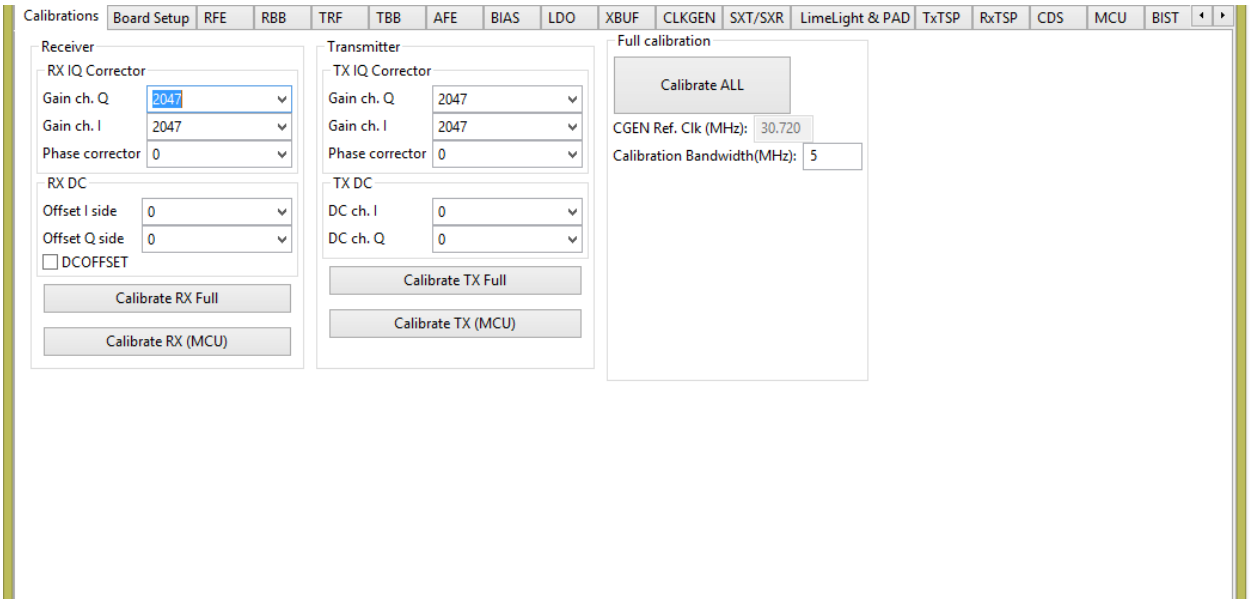

Figure 24 GUI Configuration Board Setup window

7.2.3. Log panel

Log panel section logs all activity executed with the GUI and is shown in *Figure 25*.

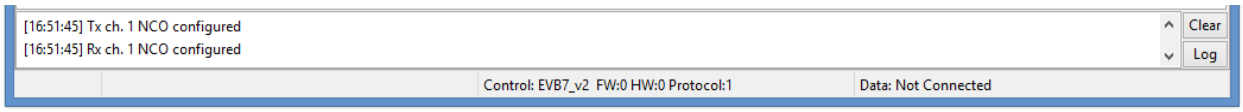

Figure 25 GUI Log panel

The **Clear** button deletes previously registered activity.

When **Log** button pressed, the **Message Log** configuration pop-up, as shown in *Figure 26*.

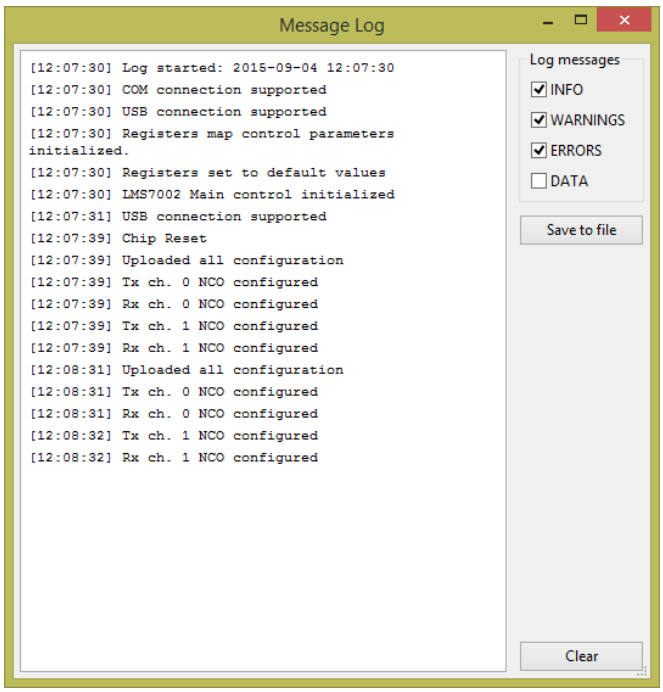

Figure 26 GUI Message Log tab

This allows you to select the type of the information you want to log. The logged messages can be saved into *.txt file.

In the lower left corner of the log tab, the evaluation board version and firmware version is displayed.

7.3 The Menu Bar

7.3.1. The File Menu

In the **File** menu there is a function 'Quite' for closing the control software when you want to restart the software or finish the work.

7.3.2. The Option Menu

In the **Options** menu**,** you can select the COM port to which evaluation board is attached.

7.3.3. The Modules Menu

This section has few extra control options for different RF and BB platforms, which are related with LMS7002M transceiver. When the **Modules** option is selected, new window will pop-up showing all module options available on GUI, as it is shown in *Figure 27*.

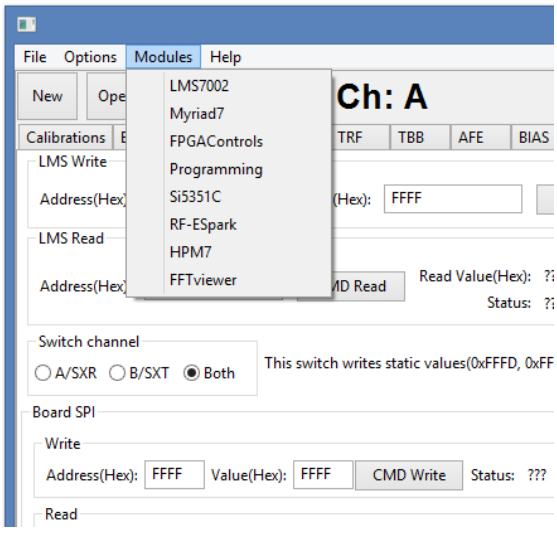

Figure 27 GUI Modules pop-up window

7.3.4. The Help Menu

The help menu contains one option giving the software version and build date. It also contains the contact details for Lime Microsystems.

7.3.5. The Button Menu

The button menu contains 6 buttons controls and 3 other minor controls.

The **NEW** button, enables to start new projects.

The **OPEN** button, opens previously saved project.

The **SAVE** button allows to save current GUI project (saved in *.ini or *.txt format). Saved project file contains complete register setup for LMS7002M. These files can be transferred to any other computer or used as a register initialization setup for LMS7002M in baseband.

The .ini format is machine readable only.
The .txt format is human and machine readable.

To write register configuration from the "LMS 7 Suite" software to the chip, press **GUI→Chip** button.

To read register configuration from the chip to the "LMS 7 Suite" software, press **Chip→GUI** button.

The **RESET** button performs a manual reset on the chip and updates the "LMS 7 Suite" software.

7.3.6. The Configuring Channel Controls

Configuring Channels window select which channel or PLL is currently controlled. The activated channel is always displayed in a front panel:

If selected **Both**, front panel will display: **Active Ch: SXR&SXT** or **Active Ch: A&B**.

If selected **A/SXR,** front panel will display: **Active Ch: SXR** or **Active Ch: A**.

If selected **B/SXT,** front panel will display: **Active Ch: SXT** or **Active Ch: B.**

The display shows information depending which configuration tab you are currently and which channel is selected.

The SXR option is used for setting the receive synthesizer parameters in the SXT/SXR tab (see section *7.15*). The SXT option is used for setting the transmitter synthesizer parameters in the SXT/SXR tab. The A and B channel to the A and B channels for the TX and RX MIMO channels of the RFE, RBB, TRF,TBB and AFE tabs.

7.4 Calibrations

Calibration page has ‘Receiver’, ‘Transmitter’, ‘Full Calibration’ tabs as it is shown in *Figure **28***.

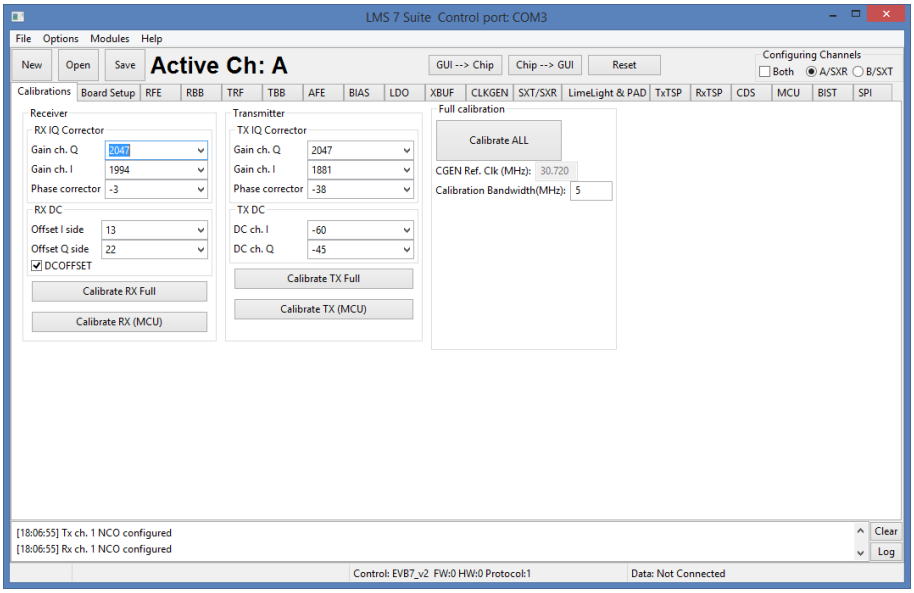

Figure 28 GUI Calibrations tab

Tabs ‘Receiver’ and ‘Transmitter’ has almost identical functions of calibrating Image and LO Leakage levels on respectful paths. An Image can be calibrated by controling IQ Correction in ‘Gain ch. Q’ and ‘Gain ch. I’ fields and also changing Phase on ‘Phase corrector’. LO Leakage can be calibrated be controlling ‘Offset I side’ and ‘Offset Q side’ on subtab ‘RX DC’subtab and controlling ‘DC ch. I’ and ‘DC ch. Q’ on ‘TX DC’ subtab.

On RX DC subtab there is an option ‘DCOFSET’. Selecting it enables DC Offset correction.

There are 2 additional buttons on both TX and RX paths dedicated to perform full automatic calibration routine on wanted path.

Button **CALIBRATE RX FULL** performs automatic calibration of Image and LO Leakage signals on RX path

Button **CALIBRATE TX FULL** performs automatic calibration of Image and LO Leakage signals on TX path

Button **CALIBRATE RX (MCU)** performs automatic calibration of Image and LO Leakage signals on RX path directly from internal MCU of LMS7002M.

Button **CALIBRATE TX (MCU)** performs automatic calibration of Image and LO Leakage signals on TX path directly from internal MCU of LMS7002M.

7.5 Board Setup (Si5351C and ADF4002)

These tabs control two other devices on the UNITE7002 board.

The ADF4002 is a PLL to lock an external reference (usually 10 MHz on X18) with the on board TXCO (usually 30.72 MHz or 52.00 MHz). This 30.72 MHz reference is supplied to the LMS7002M synthesizers. This is normally used to synchronize the measurement equipment with the UNITE7002 board remove very minor frequency differences typically a few kHz. To synchronize board:

- Press 'Synchronize' button to program the ADF4002, if all is correct the green PLL locked LED 'ADF Lock' (LD2) on the interface board should illuminate. LD2 is located in the upper left hand corner of the interface board.

Make sure that the Fxo value corresponds to the frequency of TCXO.

The Si5351C is a dual PLL for frequency conversion in the 10 – 100 MHz range. It can be used to provide programmable clock signals to external hardware through the external digital interfaces and also to the LMS7002M RX and TX PLL Clocks. This allows the clock rates to be independent of the TXCO frequency. The tab is shown in *Figure 29*.

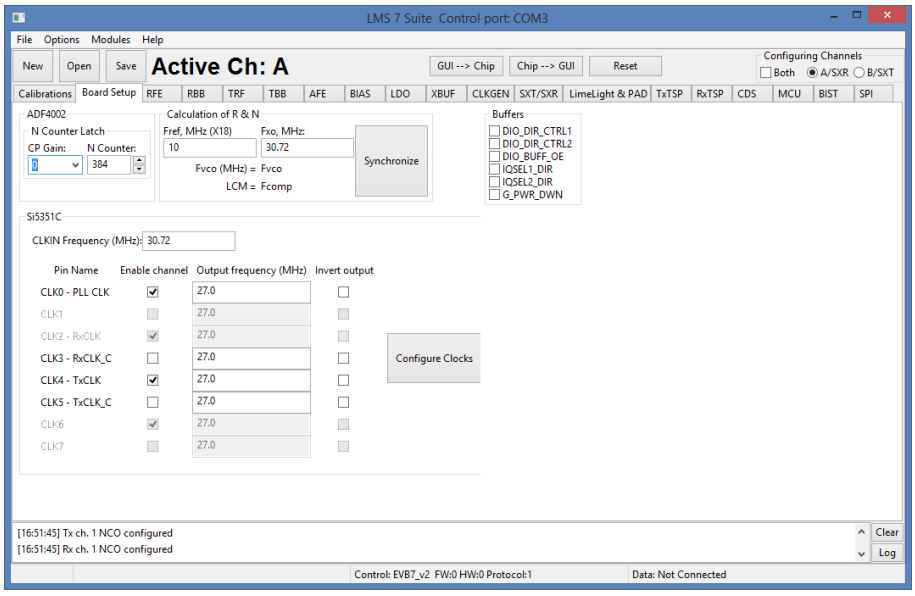

Figure 29 GUI Board Setup tab

By default, the UNITE7002 is configured to supply LMS7002M RX and TX PLL reference clock pins directly from TCXO. With a simple board modification, remove R10, R73, C229, C230 and fit R11, R76, C234, C 235, RX and TX PLL clocks can be supplied directly from the Si5351C clock generator.

Using this feature:

- Type to CLKIN Frequency (MHz) window the onboard TCXO frequency
- Enable clock channel
- Enter the desired output frequency
- Press “Configure Clocks”

The Buffers controls on board buffer directions for the LMS7002M digital interface. As well, LOGIC_RESET pin and CORE_LDO _EN pins are controlled from this window.

Table 8 GUI SPI control description

Parameter	Description
Buffers	
DIO_DIR_CTRL1	On board buffers direction control for Port 1. If selected, Port 1 is receiver.
DIO_DIR_CTRL2	On board buffers direction control for Port 2. If selected, Port 2 is receiver.
DIO_BUFF_OE	If selected, sets onboard buffers to Hi-Impedance state.
IQSEL1_DIR	On board buffers IQSEL pin direction control for Port 1. If selected, Port 1 is receiver.
IQSEL2_DIR	On board buffers IQSEL pin direction control for Port 2. If selected, Port 2 is receiver.
G_PWR_DWN	External enable control signal for the internal LDO’s.
DIG_RST	Controls hardware pin logic reset.

7.6 RFE

RFE tab controls the RX Front End stages, including LNA selection, LNA gain, TIA gain and RX LO cancellation. A picture of the tab is shown in *Figure 30*. A description of each function available in this tab is shown below in *Table 9*.

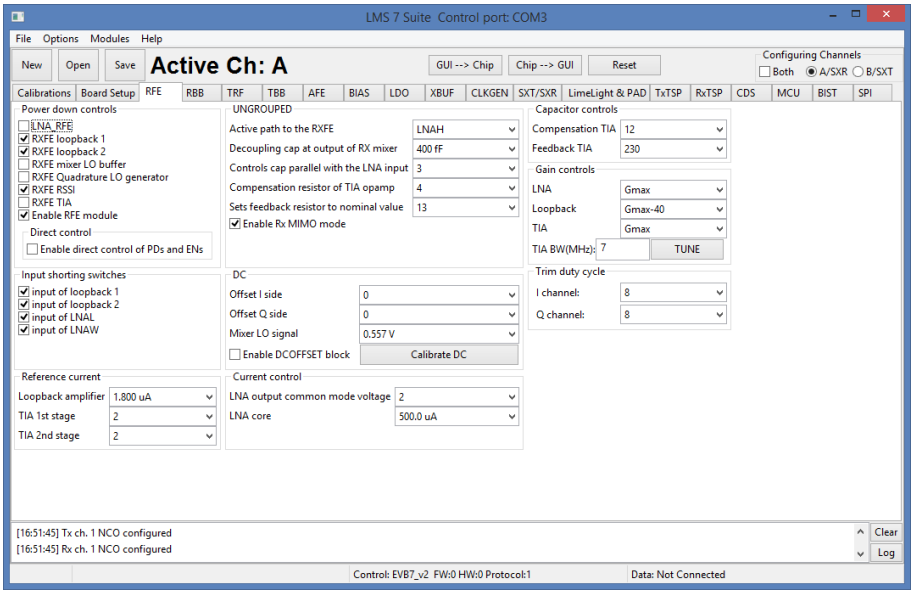

Figure 30 GUI RFE tab

Table 9 GUI RFE control description

Parameter	Description
Power down controls	
LNA_RFE	Power control for LNA. Must be deselected in normal operation.
RXFE loopback1	Power control signal for RXFE loopback to LNAL from TXRF. Used only for RF loopback.
RXFE loopback2	Power control signal for RXFE loopback to LNAW from TXRF. Used only for RF loopback.
RXFE mixer LO buffer	Power control signal for RXFE mixer lo buffer. Must be deselected in normal operation.
RXFE Quadrature LO generator	Power control signal for RXFE quadrature LO generator. Must be deselected in normal operation.
RXFE RSSI	Power control signal for RXFE RSSI. Enables RSSI readings when powered on.
RXFE TIA	Power control signal for RXFE TIA. Must be deselected in normal operation.
Enable RFE module	Major power down for RXFE modules. All modules will be power down when deselected.
Direct control	Enables direct control of PDs and ENs for RFE. Enabled when selected.
Input shorting switches	
Input of loopback 1	Enables the input shorting switch at the input of the loopback with LNAL. Should be selected when RXFE Loopback1 is NOT active.
Input of loopback 2	Enables the input shorting switch at the input of the loopback with LNAW. Should be selected when RXFE Loopback2 is NOT active.
Input of LNAL	Enables the input shorting switch at the input of the LNAL. Should be selected when LNAH is NOT active or during very high signal conditions.

Input of LNAW	Enables the input shorting switch at the input of the LNAW. Should be selected when LNAW is NOT active or during very high signal conditions.
Reference current	
Loopback amplifier	Controls reference current of the RXFE loopback amplifier. Recommended value is 1.8 uA.
TIA 1st Stage	Controls reference current of the RXFE TIA first stage. Recommended value is 2.
TIA 2nd Stage	Controls reference current of the RXFE TIA second stage. Recommended value is 2.
Capacitor controls	
Compensation TIA	Compensation capacitor for TIA. Recommended value is 15.
Feedback TIA	Feedback capacitor for TIA. Controls the 3 dB BW of the TIA. Recommended value is 230.
Trim Duty Cycle	
I channel	Trims the duty cycle in I channel. Default value set to 8.
Q channel	Trims the duty cycle in Q channel. Default value set to 8.
UNGROUPED	
Active path to the RXFE	Selects the active LNA of the RXFE between LNAL, LNAH and LNAW. Default value is no path active.
Decoupling cap at the output of RX mixer	Control the decoupling cap at the output of the RX Mixer. The capacitor range is from 80 fF to 2560 fF, with step size of 80 fF (32 steps). Default value is 640 fF.
Controls cap parallel with the LNA input	Controls the Q of the input LNA matching circuit and provides tradeoff between gain/NF and IIP2/3. The higher the frequency, the lower value should be. Also, the higher value lower the Q. Default value is 6.
Compensation resistor of TIA opamp	Controls the compensation resistors of the TIA operational amplifier. Recommended value is 5.
Sets feedback resistor value	Sets the TIA feedback resistor value. Default vale is 13.
Enable Rx MIMO	Enables MIMO mode when MIMO is selected. If SISO mode is selected only Channel A is in operation.
DC	
Offset I side	Controls DC offset of the I channel at the output of the TIA by injecting current to the input of the TIA. Control range from 0 to 127. Default value is 0.
Offset Q side	Controls DC offset of the Q channel at the output of the TIA by injecting current to the input of the TIA. Control range from 0 to 127. Default value is 0.
Mixer LO signal	Controls DC voltage of the mixer LO signal. Control range from 0.44 V to 0.621 V. Default value is 0.557 V.
Enable DCOFFSET block	Enables the DC offset block for the RXFE. Select before calibrating DC offset of the Rx path
Current Control	
LNA output common mode voltage	Controls the LNA output common mode voltage. Control range from 0 to 31. Default value is 2.
LNA Core	Controls the current of the LNA core. Control range from 0uA to 1291.7 uA. Default value is 500 uA.
Gain Controls	
LNA	Controls selected LNA gain. Control range from Gmax to Gmax-30. Default value is Gmax.
Loopback	Controls RXFE loopback gain. Control range from Gmax to Gmax-40. Default value is Gmax-40 dB.
TIA	Controls TIA Gain. Three gain stages: Gmax, Gmax-3 dB and Gmax-12 dB. Default value is Gmax.

7.7 RBB

RBB tab controls the receiver IF stage bandwidth, PGA gain and loopback.

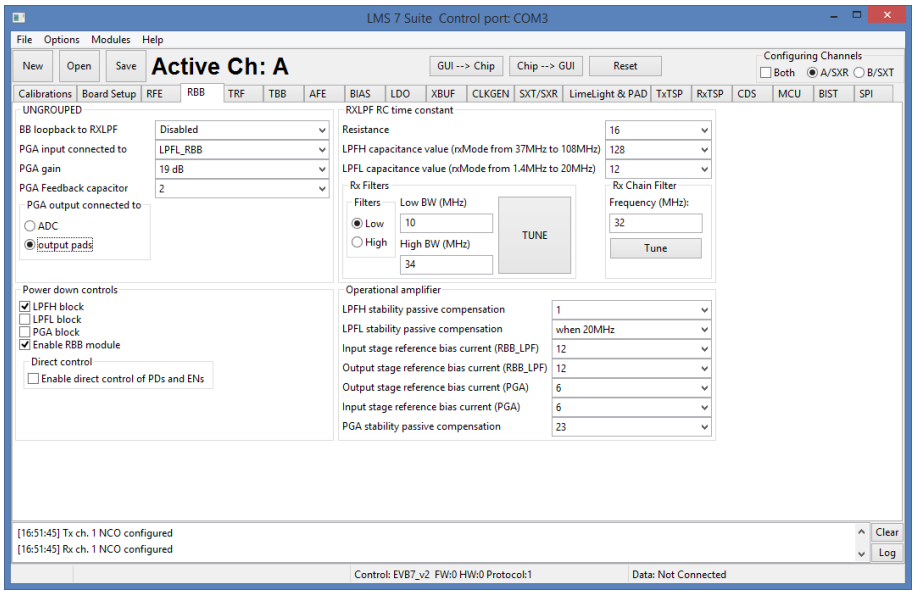

Figure 31 GUI RXBB tab

A picture of the tab is shown in *Figure 31*. A description of each function available in this tab is shown below in *Table 10*.

Table 10 GUI RXBB control description

Parameter	Description
UNGROUPED	
BB loopback to RxLPF	Enables baseband loopback to high band LPF or low band LPF. Enables loopback when selected. Default value is disabled.
PGA input connected to	Controls PGA input path. There are a total five different inputs to the PGA: 1. LPFL_RBB 2. LPFH_RBB 3. Bypass LPF 4. Tx baseband loopback connected to PGA 5. TXRF peak detector connected to PGA Concurrently only one path can be selected as PGA input. Default path is LPFL output connected to PGA.
PGA gain	PGA gain control. Control range from -12 dB to +19 dB. Default value is -1 dB.
PGA Feedback capacitor	PGA feedback capacitor value control. Control range from 0 to 511. Default value is 2.
PGA output connected to	Control PGA output switch internally directly to ADC or indirectly via the Analog output pads. Default value of PGA output is selected to ADC input.
Power down controls	
LPFH block	Power down of the LPFH block. Default value block is powered down.
LPFL block	Power down of the LPFL block. Default value block is powered on.
PGA block	Power down of the PGA block. Default value block is powered on

Enable RBB module	Powers down all RBB blocks when not selected. If selected enables power down of separate RBB blocks. Default values set to enable.
Direct control	Enable direct control of PDs and ENs. Enabled when selected.
RXLPF RC time constant	
Resistance	Controls the absolute value of the resistance of the RC time constant in LPF. Control range from 0 to 31. The higher value selected the wider LPF BW. Default values set to 16.
LPFH capacitance value (rxMode from 37 MHz to 108 MHz)	Controls the capacitance value of the RC time constant of high band LPF. Control range from 0 to 255. The lower value selected the wider LPF BW. Default values set to 0.
LPFL capacitance value (rxMode from 1.4 MHz to 20 MHz)	Controls the capacitance value of the RC time constant of low band LPF. Control range from 0 to 255. The lower value selected the wider LPF BW. Default values set to 0. Intended to be controlled together with the TIA to maintain Chebyshev response.
Rx Filters	
Filters	Selects which active filter chain (Low or High) will be tuned
Low BW (MHz)	Input for the wanted bandwidth of the Low active filter chain
High BW (MHz)	Input for the wanted bandwidth of the High active filter chain
TUNE	Tunes the selected active filter chain bandwidth to the required value (set by “Low BW (MHz)” or “High BW (MHz)”)
Operational amplifier	
LPFH stability passive compensation	Controls the stability passive compensation of the LPFH operational amplifier. Control range from 0 to 7. Default values set to 0.
LPFL stability passive compensation	Controls the stability passive compensation of the LPFL operational amplifier. Control range from 0 to 5. Default values set to 5.
Input stage reference bias current (RBB_LPF)	Controls the reference bias current of the input stage of the operational amplifier used in LPF blocks (Low or High). Must increase up to 24 when a strong close blocker is detected to maintain the linearity performance. Control range from 0 to 31. Default values set to 12.
Output stage reference bias current (RBB_LPF)	Controls the reference bias current of the output stage of the operational amplifier used in LPF blocks (Low or High). Must increase up to 24 when a strong close blocker is detected to maintain the linearity performance. Control range from 0 to 31. Default values set to 12.
Output stage reference bias current (PGA)	Controls the output stage reference bias current of the operational amplifier used in the PGA circuit. Must increase up to 12 when a strong close blocker is detected or when operating at the high band frequencies to maintain the linearity performance. Control range from 0 to 31. Default values set to 6.
Input stage reference bias current (PGA)	Controls the input stage reference bias current of the operational amplifier used in the PGA circuit. Must increase up to 12 when a strong close blocker is detected or when operating at the high band frequencies to maintain the linearity performance. Control range from 0 to 31. Default values set to 6.
PGA stability passive compensation	Controls the stability passive compensation of the PGA operational amplifier. Control range from 0 to 31. Default values set to 24.

7.8 TRF

The TRF page contains the Tx front end amplifier gain controls, Tx outputs paths selection controls and all transmit block power down controls.

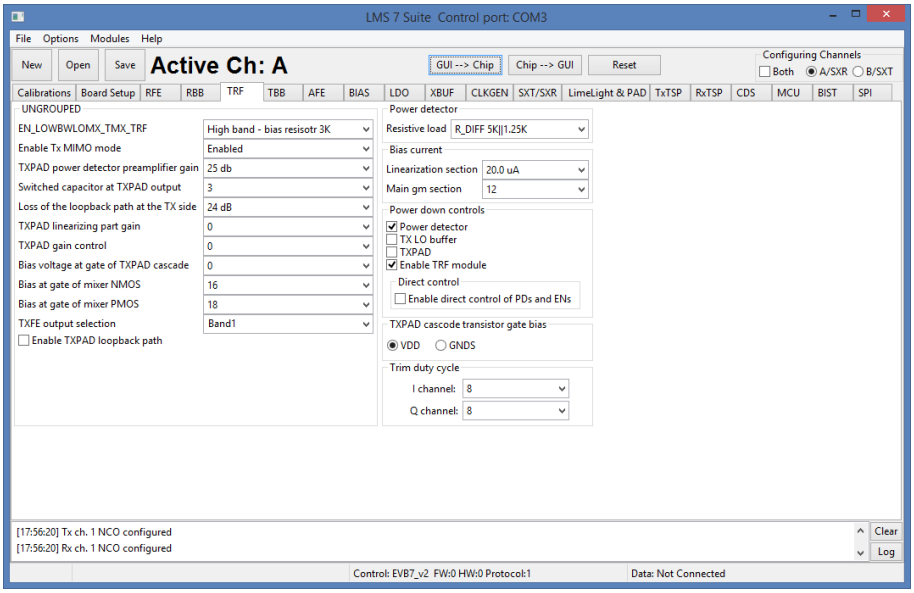

Figure 32 GUI TRF page

A picture of the tab is shown in *Figure 32*. A description of each function available in this tab is shown below in *Table 11*.

Table 11 GUI TRF control description

Parameter	Description
UNGROUPED	
EN_LOWBWLOMX_TMX_TRF	Controls the high pass pole frequency of the mixer switches. Selection between low band and high band. Default is high band selection.
Enable Tx MIMO mode	Enables MIMO mode. Default is set to SISO mode.
TXPAD power detector preamplifier gain	Controls TXPAD power detector gain. Default gain is set to 25 dB.
Switched capacitor at TXPAD output	Controls TXPAD output capacitor used for fine tuning. Control range from 0 to 7. Default is set to 3.
Loss of the loopback path at the TX side	Controls Tx loopback path gain. Default gain is set to -24 dB.
TXPAD linearizing part gain	Controls TXPAD linearization gain. Control range from 0 to 31. Default is set to 0.
TXPAD gain control	Controls the gain of TXPAD. Control range from 0 to 31. Default is set to 0 (Max gain).
Bias voltage at gate of TXPAD cascade	Controls the bias voltage at the gate of TXPAD cascade. Control range from 0 to 31. Default is set to 0.
Bias at gate of mixer NMOS	Controls the bias at the gate of the mixer NMOS switch. Control range from 0 to 31. Default is set to 28.

Bias at gate of mixer PMOS	Controls the bias at the gate of the mixer PMOS switch. Control range from 0 to 31. Default is set to 16.
TXFE output selection	Enables TXFE, Band 1 or Band 2 output. Band 1 enabled by default.
Enable TXPAD loopback path	Enables the TXPAD loopback path. Disabled by default.
Power detector	
Resistive load	Controls power detector dynamic range by selecting resistive load. Default is set to 5K||1.25K.
Bias current	
Linearization section	Control the bias current of the linearization section of the TXPAD. Control range from 0 to 31. Default is set to 12.
Main gm section	Control the bias current of the TXPAD. Control range from 0 to 31. Default is set to 12.
Power down controls	
Power detector	Enables power detector when deselected. By default power detector is powered down.
TX LO buffers	Enables TX LO buffer. By default TX LO is enabled.
TXPAD	Enables TXPAD block. By default TXPAD is enabled
Enable TRF modules	Power down all TFE blocks when deselected. By default TRF blocks enabled.
Direct Control	Enable direct control of PDs and ENs. Enabled if selected.
TXPAD cascade transistor gate bias	
VDD	TXPAD cascade transistor gate bias is referred to VDD – connect to VDD to operate.
GNDS	TXPAD cascade transistor gate bias is referred to GND.
Trim duty cycle	
I channel	Trims the duty cycle in I channel. Default value set to 8.
Q channel	Trims the duty cycle in Q channel. Default value set to 8.

7.9 TBB

The TBB page controls TX IF gain settings, low-LPF and high-LPF filter bandwidths and various loopback options.

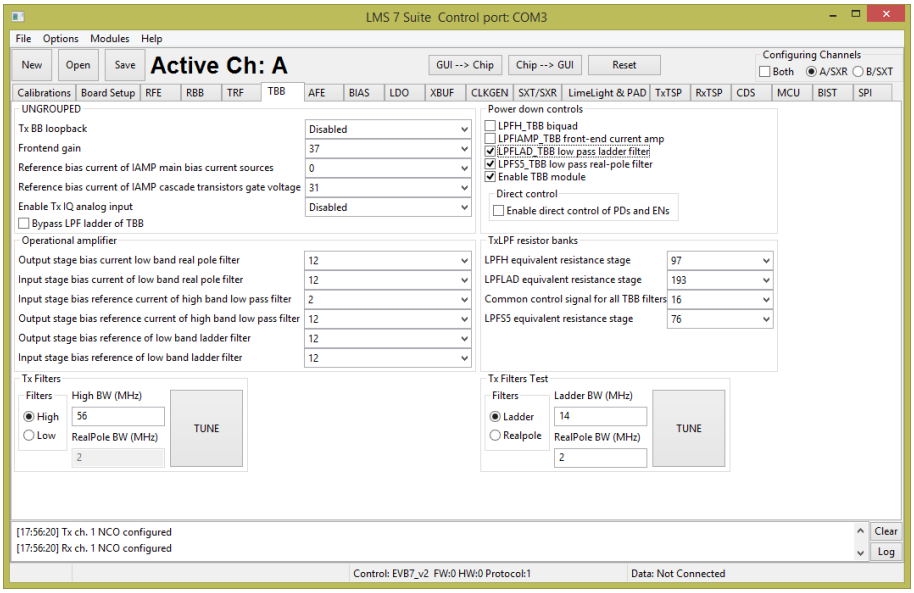

Figure 33 GUI TBB page

A picture of the tab is shown in *Figure 33*. A description of each function available in this tab is shown below in *Table 12*.

Table 12 GUI TBB control description

Parameter	Description
UNGROUPED	
Tx BB Loopback	Controls the Tx BB loopback path. By default loopback is disconnected.
Frontend gain	Tx baseband stage gain control. Control range from 0 to 63. Default is set to 24.
Reference bias current of IAMP main bias current source	This controls the reference bias current of the IAMP main bias current sources. Control range from 0 to 31. Default is set to 12.
Reference bias current of IAMP cascode transistors gate voltage	This controls the reference bias current of the IAMP's cascode transistors gate voltages that set the IAMP's input voltage level. Control range from 0 to 31. Default is set to 12.
Enable Tx IQ analog input	Controls Tx analog inputs path. By default disabled.
Bypass LPF ladder of TBB	Controls TBB LPF ladder bypass mode.
Operational amplifier	
Output stage bias current low band real pole filter	This controls the operational amplifier's output stage bias current. Control range from 0 to 31. Default is set to 12.

Input stage bias current low band real pole filter	This controls the operational amplifier's input stage bias current. Control range from 0 to 31. Default is set to 12
Input stage bias reference current of high band low pass filter	This controls the operational amplifiers input stage bias reference current of the high band filter. Control range from 0 to 31. Default is set to 2.
Output stage bias reference current of high band low pass filter	This controls the operational amplifiers output stage bias reference current of the high band filter. Control range from 0 to 31. Default is set to 12.
Output stage bias reference for low band ladder filter	This controls the operational amplifiers' output stages bias reference current of the low band filter. Control range from 0 to 31. Default is set to 12.
Input stage bias reference for low band ladder filter	This controls the operational amplifiers' input stages bias reference current of the low band filter. Control range from 0 to 31. Default is set to 12.
Power down controls	
LPFHTBB biquad	Enables LPFH filter when deselected. By default filter is powered down.
LPFIAMP front-end current amp	Enables LPF current amplifier when deselected. By default current amplifier is enabled.
LPFLADTBB low pass ladder filter	Enables LPF ladder when deselected. By default current amplifier is enabled.
LPFS5TBB low pass real-pole filter	Enables LPF real-pole filter when deselected. By default real-pole filter is enabled.
Enable direct control of PDs and ENs	Enables direct control of PDs and ENs for TBB. Enabled when selected.
TxLPF Resistor banks	
LPFH equivalent resistance stage	Control LPFH bandwidth. Control range from 0 to 255. The higher number the higher bandwidth. Default setting is 0.
LPFLAD equivalent resistance stage	Control LPFL bandwidth. Control range from 0 to 255. The higher number the higher bandwidth. Default setting is 193.
Common control signal for all	A common control signal for all the capacitor banks of TBB filters. Control range from 0 to 31. Default register value set to 8.
LPFS5 equivalent resistance stage	This controls the value of the equivalent resistance of the resistor banks of the real pole filter stage. Control range from 0 to 255. Default register value set to 76.
Tx Filters	
Filters	Selects which active filter chain (Low or High) will be tuned
High BW (MHz)	Input for the wanted bandwidth of the High active filter chain
Low BW (MHz)	Input for the wanted bandwidth of the Low active filter chain ladder stage (4th order low-pass filter). NOTE: Low active filter chain consists of two independently controlled filter stages (ladder and real pole) that are connected in series, hence the total frequency response is the sum of both filter stages frequency responses.
RealPole BW (MHz)	Input for the wanted bandwidth of the Low active filter chain real pole stage (1st order low-pass filter). NOTE: Low active filter chain consists of two independently controlled filter stages (ladder and real pole) that are connected in series, hence the total frequency response is the sum of both filter stages frequency responses.
TUNE	Tunes the selected active filter chain (set by “Filters” tab option) bandwidth to the required value (set by “High BW (MHz)” or “Low BW (MHz)” and “RealPole BW (MHz)”)
Tx Filters Test	
Filters	Selects which low active filter chain stage (ladder or real pole) will be tuned.
Ladder BW (MHz)	Input for the wanted bandwidth of the Low active filter chain ladder stage (4th order low-pass filter)

RealPole BW (MHz)	Input for the wanted bandwidth of the Low active filter chain real pole stage (1st order low-pass filter)
TUNE	Tunes the selected low active filter chain stage bandwidth to the required value (set by "Ladder BW (MHz)" or "RealPole BW (MHz)")

7.10 AFE

The AFE page controls the TX and RX analog front-end interface to the digital section.

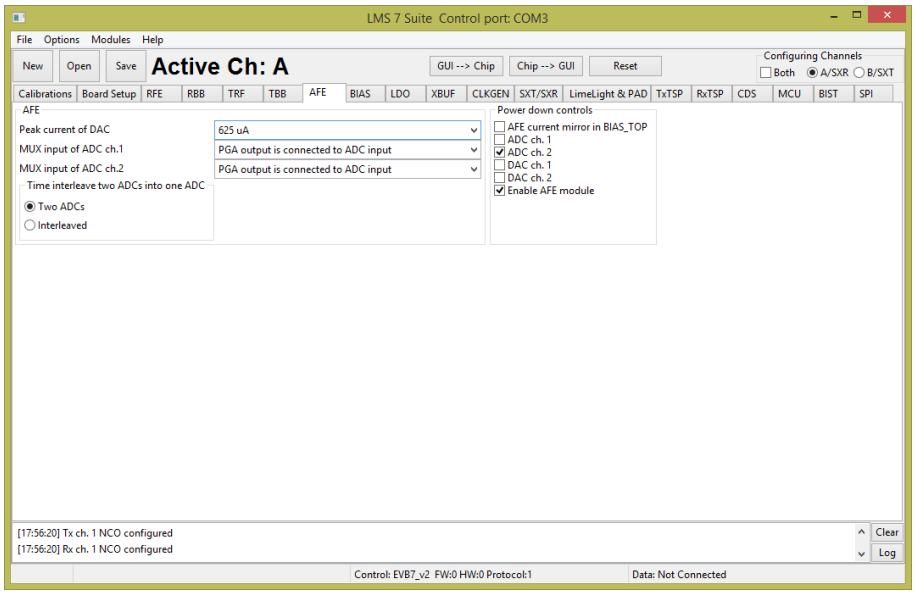

Figure 34 GUI AFE tab

A picture of the tab is shown in
Figure 34. A description of each function available in this tab is shown below in *Table 13*.

Table 13 GUI AFE control description

Parameter	Description
AFE	
Peak current of DAC	Controls the peak current of the DAC output current. By default DAC peak current set to 325 uA.
MUX input of ADC ch 1.	Controls the MUX at the input of the ADC channel 1. By default MUX set to PGA output.
MUX input of ADC ch 2.	Controls the MUX at the input of the ADC channel 2. By default MUX set to PGA output.
Time interleave two analogue signals into one ADC	Default register set to Two ADC's
Power down controls	
AFE current mirror in BIASTOP	Enabled AFE current mirror in BIAS_TOP when deselected. Default current mirror is enabled.
ADC ch. 1	Enable control of ADC of channel 1. Enabled when not selected. Enabled by default.
ADC ch. 2	Enable control of ADC of channel 2. Enabled when not selected. Enabled by default.
DAC ch. 1	Enable control of DAC of channel 1. Enabled when not selected. Enabled by default.
DAC ch. 2	Enable control of DAC of channel 2. Enabled when not selected. Enabled by default.
Enable AFE module	Enabled AFE blocks when selected. By default AFE is enabled.

7.11 BIAS

The BIAS page controls the LMS7002M bias settings.

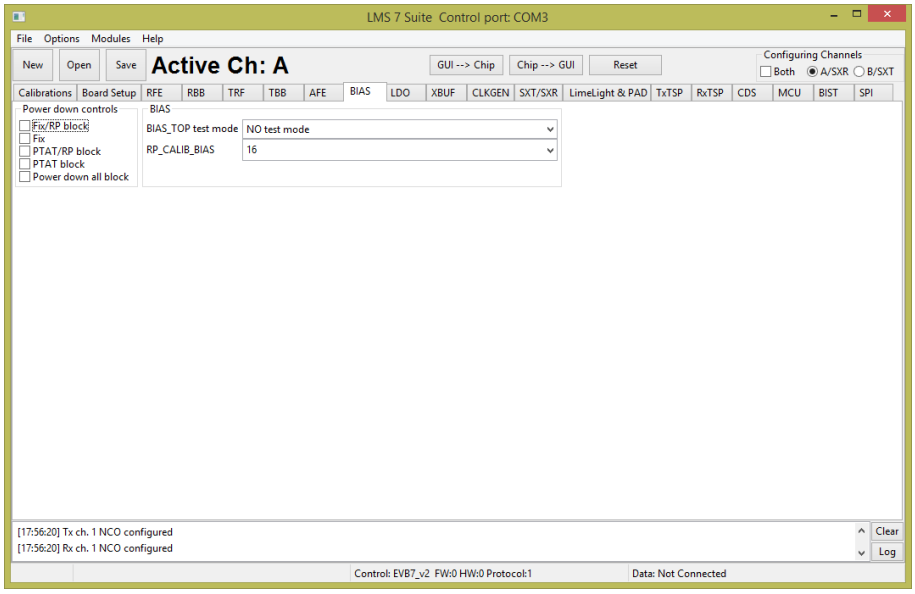

Figure 35 GUI BIAS tab

A picture of the tab is shown in *Figure 35*. A description of each function available in this tab is shown below in *Table 14*.

Table 14 GUI BIAS control description

Parameter	Description
Power down controls	
Fix /RP block	Enable signal for Fix/RP block when not selected. Default register setting is set to enabled.
Fix	Enable signal for Fix block when not selected. Default register setting is set to enabled.
PTAT/RP block	Enable signal for PTAT/RP block when not selected. Default register setting is set to enabled.
PTAT	Enable signal for PTAT block when not selected. Default register setting is set to enabled.
Power down all block	Enables BIAS block when selected. By default BIAS block is enabled.
BIAS	
BIASTOP test mode	Controls the test mode of the BIAS_TOP. No test mode selected by default.
RP_CALIB_bias	Control bias current calibration code. Control range from 0 to 31. Default setting is 0. This is used to set the voltage across current reference resistor R12 to 600 mV – typically code 7. The “calibrate” button automatically sets this.

7.12 LDO

This tab controls the internal LDO modules. These LDO's are used when the LMS7002M chip analog blocks supplied by single 1.8V supply. Pictures of the tab is shown in *Figure 36* and *Figure 37*.

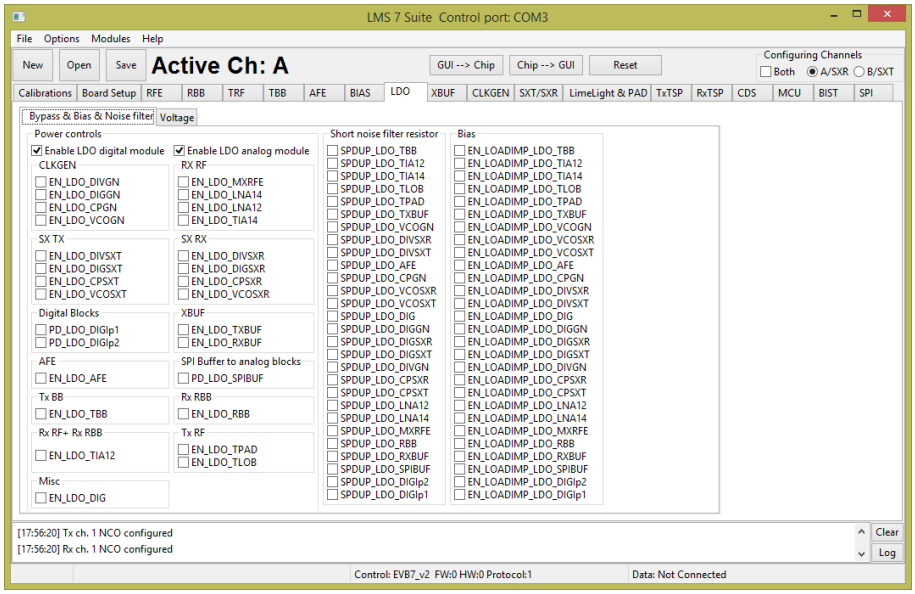

Figure 36 GUI LDO Power downs & Bias & Noise filter tab

Each 1.25 V and 1.4 V supply pins have internal regulators controlled via SPI interface. The LDO "Bypass & Bias & Noise filter" tab (figure above) divided in separate sections:

- Power control
- Short noise filter resistor
- Bias

In **Power control** section is the SPI controls are in groups related to their function. These controls enable the LDO for the particular block.

Short noise filter resistor bypasses noise filtering resistor. By default enabled.

Bias section enables the load dependent bias to optimize the load regulation for each LDO. This option reduces the LDO response, but increase total current consumption. Recommend to set to constant bias (not selected).

In the 'Voltage' tab the voltage level of the each internal LDO can be adjusted (figure below).

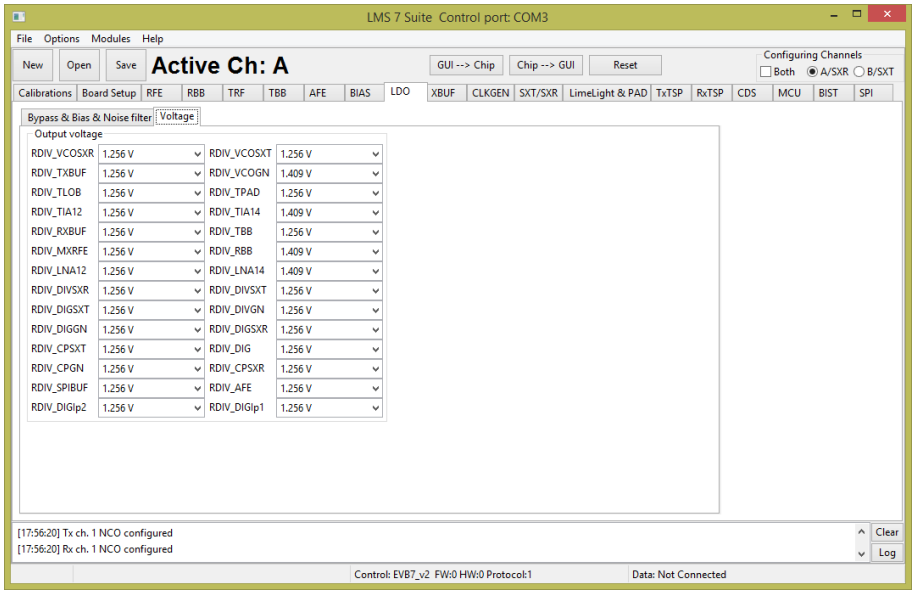

Figure 37 GUI LDO Voltages tab

7.13 XBUF

XBUF page controls the TX and RX PLL clock pin input configurations to provide a reference frequency for SXT and SXR respectively. The CLKGEN PLL uses the SXR Clock.

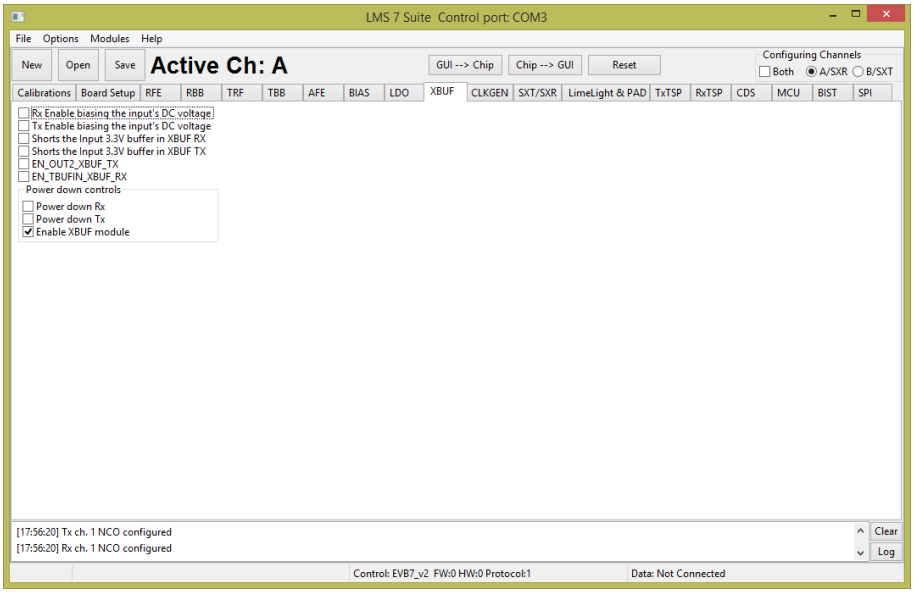

Figure 38 GUI XBUF tab

A picture of the tab is shown in *Figure 38*. A description of each function available in this tab is in *Table* 15.

Table 15 GUI XBUF control description

Parameter	Description
UNGRPUPED	
Rx Enable biasing the input's DC voltage	Receiver clock input self-biasing digital control. By default disabled. For use with AC coupled input.
Tx Enable biasing the input's DC voltage	Transmitter clock input self-biasing digital control. By default disabled. For use with AC coupled input.
Shorts the input 3.3V buffer in XBUF RX	Shorts the Input of 3.3V buffer in XBUF. By default disabled
Shorts the input 3.3V buffer in XBUF TX	Shorts the Input of 3.3V buffer in XBUF. By default disabled
EN_OUT2_XBUF_TX	Enables the 2nd output of TX XBUF. By default buffer is disabled. This control is intended to internally rout TX PLL CLK to SXT and SXR by an internal path.
EN_TBUFIN_XBUF_RX	Disables the input from the external XO. By default buffer is disabled. This control is intended to internally rout TX PLL CLK to SXT and SXR by an internal path.
Power down controls	
Power down Rx	Power down control of the Rx XBUF. Not powered down by default.
Power down Tx	Power down control of the Tx XBUF. Not powered down by default.
Enable XBUF module	Power down complete XBUF block. Enabled by default.

7.14 CLKGEN

The block diagram of the CGEN module (internal clock generator) is shown. The table in this chapter describes the control registers of the CGEN module.

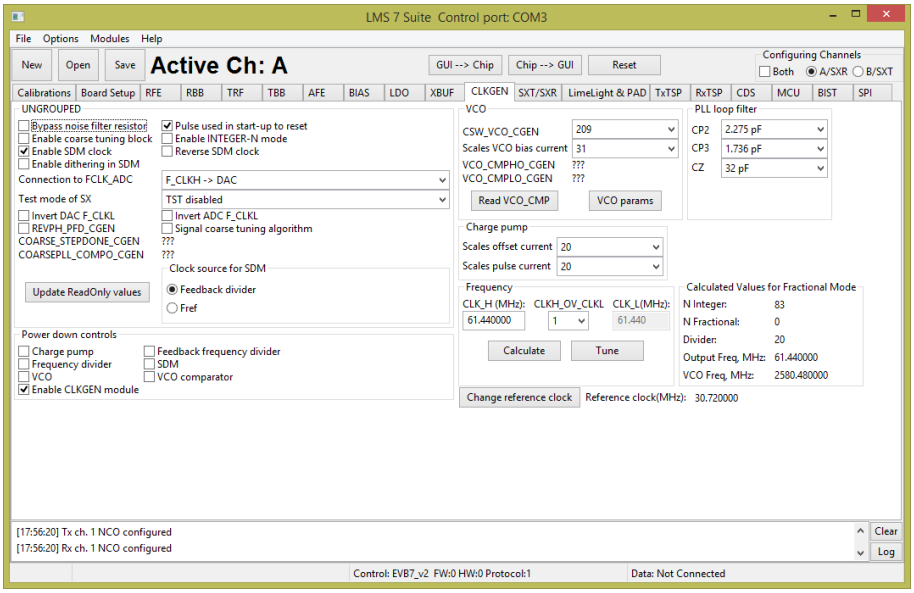

Figure 39 GUI CLKGEN tab

The internal LMS7002N CLKGEN generates clock for ADC's, DAC's and TSP modules. To program the CLKGEN for wanted frequency follow the step below:

1. Type the wanted frequency in CLK_H (MHz) window (default frequency is 61.44 MHz)
2. Press 'Calculate' followed by 'Tune'

After this procedure the digital block core will be supplied by wanted frequency. All other register are preset so no need to change.

A picture of the tab is shown in *Figure 39*. A description of each function available in this tab is shown below in *Table 16*.

Table 16 GUI CLKGEN control description

Parameter	Description
UNGROUPED	
Bypass noise filter resistor	Bypasses the noise filter resistor for fast settling time. Disabled by default.
Enable coarse tuning block	Enable signal for coarse tuning block. Disabled by default.
Enable SDM clock	Enables SDM clock. Used in INT-N mode or for noise testing. Enabled by default.
Enable dithering in SDM	Enabled dithering. Disabled by default.
Connection to FCLK_ADC	Selects if F_CLKH or F_CLKL is connected to FCLK_ADC. By default FCLK_ADC connected to F_CLKH and FCLK_DAC to F_CLKL.

Test mode of SX	Controls the test mode of the SX. Available test modes: 0: TST disabled. By default test mode disabled. 1: tstdo[0]=CLKH1 & tstdo[1]=CLKH2 2: tstdo[0]=CLK_SDM & tstdo[1]=DIV_CLK 2: tstao=vco_vtune through a 50Kohm resistor 3: tstdo[0]=REFCLK & tstdo[1]=DIV_CLK 3: tstao=vco_vtune through a 10Kohm resistor 5: tstdo[0]=PFD UP & tstdo[1]=PFD DN
Invert DAC F_CLK	Inverts the clock F_CLKL for TX TSP. By default is not inverted.
REVPH_PFD_CGEN	Inverts the pulses of PFD. It can be used to reverse the polarity of the PLL loop. By default pulse is not inverted.
Pulse used in start-up to reset	Enables pulse to reset the CLKGEN. By default set to normal operation.
Enable INTEGER-N mode	Enables INTEGER-N mode of the synthesizer. By default disabled.
Reverse SDM clock	Invert the SDM clock. By default not inverted.
Invert ADC F_CLK	Inverts the clock F_CLKL for RX TSP. By default is not inverted.
Signal coarse tuning algorithm	Enables CLKGEN coarse tuning algorithm
Clock source for SDM	Selects the clock source for the SDM (external REF clock or feedback divider output)
Update ReadOnly values	Updates ReadOnly values
Power down controls	
Charge pump	Power down control for charge pump of the CGEN block. Enabled (deselected) by default.
Frequency divider	Power down control for forward frequency divider of the CGEN block. Enabled (deselected) by default.
VCO	Power down control for VCO of the CGEN block. Enabled (deselected) by default.
Enables CLKGEN module	Power down control of the CGEN block. Enabled (selected) by default.
Feedback frequency divider	Power down control for feedback divider of the CGEN block. Enabled (deselected) by default.
SDM	Power down control for SDM of the CGEN block. Enabled (deselected) by default.
VCO comparator	Power down control for VCO comparators of the CGEN block. Enabled (deselected) by default.
VCO	
CSW_VCO_CGEN	Coarse control of VCO frequency, 0 for lowest frequency and 255 for highest, by 1 step. By default set to 128.
Scales VCO bias current	Scales the VCO bias current from 0 to 2.5 xInom. Control range from 0 to 31. Default value 16.
PLL loop filter	
CP2	Controls the value of CP2 (cap from CP output to GND) in the PLL loop filter. Control range from 0 to 5688 fF. Default value 2275.2 fF.
CP3	Controls the value of CP3 (cap from CP output to GND) in the PLL loop filter. Control range from 0 to 3720fF. Default value 1736.00 fF.
CZ	Controls the value of CP3 in the PLL loop filter. Control range from 0 to 43800fF. Default value 321200.00 fF.
Charge pump	
Scales offset current	Scales the offset current of the charge pump, from 0 to 63. This current is used in Fran-N mode to create an offset in the CP response and avoid the non-linear section. Default value is set to 20.
Scales pulse current	Scales the pulse current of the charge pump, from 0 to 63. Default value is set to 20.

7.15 SXT/SXR

This tab controls the SXT and SXR modules. The table in this chapter describes the control registers of SXT and SXR modules.

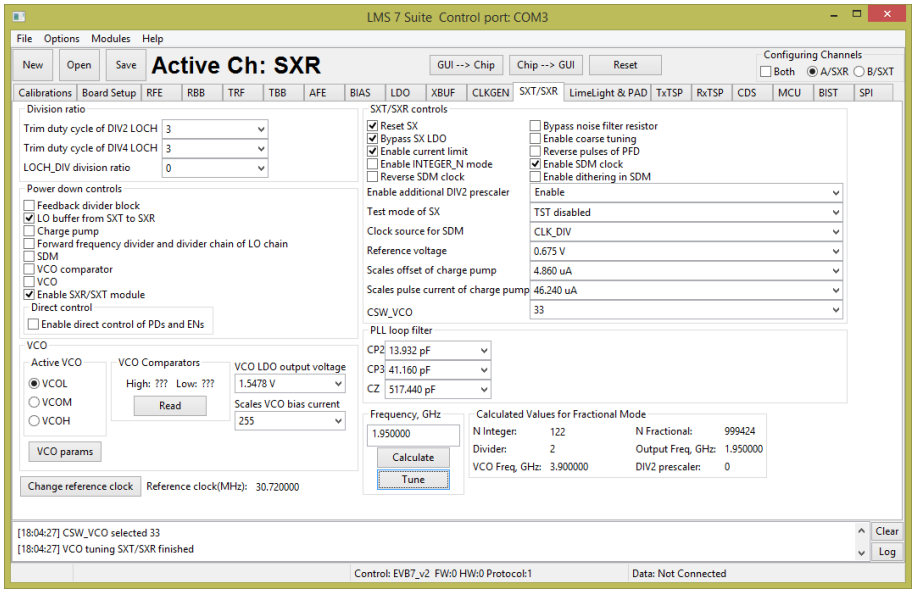

Figure 40 GUI SXT/SXR tab

Most of the SXT/SXR registers are preset to for normal (FDD) operation. To configure Tx/Rx LO to wanted frequency, do the following:

1. Select the **A/SXR** (receiver PLL) or **B/SXT** (transmitter PLL) in configuration channels window accordingly which PLL frequency you want to control
2. Enable **VCO** (deselect)
3. Type the wanted frequency in **Frequency, GHz** box. In this case 1950 MHz.
4. Press **Calculate** followed by **Tune**

A picture of the tab is shown in *Figure 40*. A description of each function available in this tab is shown below in *Table 17*.

Table 17 GUI SXT/SXR control description

Parameter	Description
Division ration	
Trim duty cycle of DIV2 LOCH	Trims the duty cycle of DIV2 LOCH. Only works when forward divider is dividing by at least 2 (excluding quadrature block division). If in bypass mode, this does not work. By default set to 3.
Trim duty cycle of DIV4 LOCH	Trims the duty cycle of DIV4 LOCH. Only works when forward divider is dividing by at least 4 (excluding quadrature block division). If in bypass mode, this does not work. By default set to 3.
LOCH_DIV division ration	Controls the division ratio in the LOCH_DIV. By default set to 2.

Power down controls	
Feedback divider block	Enables PLL feedback divider. By default is enabled.
LO buffer from SXT to SXR	Power down control for LO buffer from SXT to SXR. Controlled for SXT only. To be activated only in the TDD mode. By default is disabled.
Charge pump	Power down control for Charge Pump block. By default is enabled.
Froward frequency divider and divider chain of LO chain	Power down control for feedback frequency divider and divider chain of the LO chain. By default is enabled.
SDM	Power down control for SDM block. By default is enabled.
VCO comparator	Power down control for VCO comparator block. By default is enabled.
VCO	Power down control for VCO block. By default is disabled.
Enable SXR/SXT module	Power down control for SXT/SXR block. By default enabled.
Direct control	Enabled control of PD and EN. Enabled if selected.
VCO	
Active VCO	Selects the active VCO. It is set by SX_SWC calibration. By default VCOH selected.
VCO LDO output voltage	Controls VCO LDO output voltage. Control range from 0 to 255. By default set to 185.
Scales VCO bias current	Scales the VCO bias current from 0 to 2.5xInom. Control range from 0 to 255. By default set to 255.
SXT/SXR controls	
Reset SX	Resets SX when enabled. A pulse should be used in the start-up to reset. By default disabled.
Bypass SX LDO	Controls the bypass signal for the SX LDO. By default LDO is bypassed.
Enable current limit	Enables the output current limitation in the VCO regulator. By default enabled.
Enable INTEGR_N mode	Enables INTEGER-N mode of the SX. By default SX is set to Frac-N mode.
Reverse SDM clock	Inverts DSM clock. By default clock is not inverted.
Bypass noise filter resistor	Bypasses the noise filter resistor for fast settling time. By default the speed up is not enabled.
Enable coarse tuning	Enable signal for coarse tuning block.
Reverse pulses of PFD	Inverts the pulses of PFD block. It can be used to reverse the polarity of the PLL loop. By default the clock is not inverted.
Enable SDM clock	Enables SDM clock Enabled by default.
Enable dithering in SDM	Enabled dithering in SDM. Disabled by default.
Enable additional DIV2 prescaler	Enables additional DIV2 prescaler at the input of the programmable divider. The core of programmable divider in the SX feedback divider works up to 5.5 GHz. For FVCO > 5.5 GHz, the prescaler is needed to lower the input frequency. By default prescaler is not enabled.
Test mode of SX	Controls the test mode of the SX. Available test modes: 0: TST disabled. By default test mode disabled. 1: tstdo[0]=REFCLK & tstdo[1]=DIV_CLK & tstdo[2]=CLK_SDM 2: tstao[0] vco_vtune through a 50Kohm resistor 4: tstao[0] vco_vtune through a 10Kohm resistor 5: tstdo[0]=PFD UP & tstdo[1]=PFD DN
Clock source for SDM	Selects the clock source for the SDM (external REF clock or feedback divider output)
Reference voltage	Sets the reference voltage for varactor. By default set to 1.6 V.
Scales offset of charge pump	Scales the offset current of the charge pump block. Control range from 0 to 15 uA. This current is used in Fran-N mode to create an offset in the CP response and avoid the non-linear section. By default set to 2.9 uA.
Scales pulse current of charge pump	Scales the pulse current of the charge pump block. Control range from 0uA to 145.6. By default set to 145.6.

CSW_VCO	Coarse control of VCO frequency, 0 for lowest frequency and 255 for highest. This control is set by SX_SWC calibration. Default value set to 128.
PLL loop filter	
CP2	Control for CP2 value (cap from CP output to GND) of the PLL loop filter. Control range from 0 fF to 34830 fF. Default value 13932 fF.
CP3	Control for CP3 value (cap from CP output to GND) of the PLL loop filter. Control range from 0 fF to 88200 fF. Default value 41160 fF.
CZ	Control for CZ value of the PLL loop filter. Control range from 0 fF to 705.6 fF. Default value 517.44 fF.

7.16 Application Note on Tuning PLLs on LMS7002M

The LMS7002M has three synthesisers: SXT, SXR and CLKGEN. The LMS 7 Suite uses a simple tuning algorithm to control these. The minimum and maximum frequencies of each VCO are defined in the "VCO PARAMS" control for each VCO. This allows linear interpolation of CSW_VCO control when using the "Tune" control. Further frequencies could be added to the "VCO PARAMS" table to allow quadratic or cubic interpolation.

The LMS7002M also provides two comparators to detect if the VCO tuning voltage is within the recommended limits. These comparators are read with the "Read" or "Read CMP" buttons, after the "Tune" process has been carried out. When the PLL is successfully locked, the low comparator should be "1" and the high comparator "0". If the comparators are both "0", or both "1", then the tuning voltage is outside the recommended range.

For best phase noise and best protection against drift the following procedure is recommended. The "Tune" button gives a nominal value for CSW_VCO. The value of CSW_VCO is manually increased until the tuning comparators report the tune voltage is out of range. The last good CSW_VCO value, CSW_VCO_{max} , is noted. Then CSW_VCO is manually decreased until the tuning comparators report that the tune voltage is out of range. The last good CSW_VCO, CSW_VCO_{min}, is also noted. The average of the two extreme CSW_VCO values is the optimum CSW_VCO_{opt} which will give good phase noise and protection against drift.

$$CSW\_VCO_{opt} = \frac{CSW\_VCO_{max} + CSW\_VCO_{min}}{2}$$

7.17 LimeLight & PAD

This tab controls the LMS7002M digital interface configuration. The IO cell controls are described in the chapter tables.

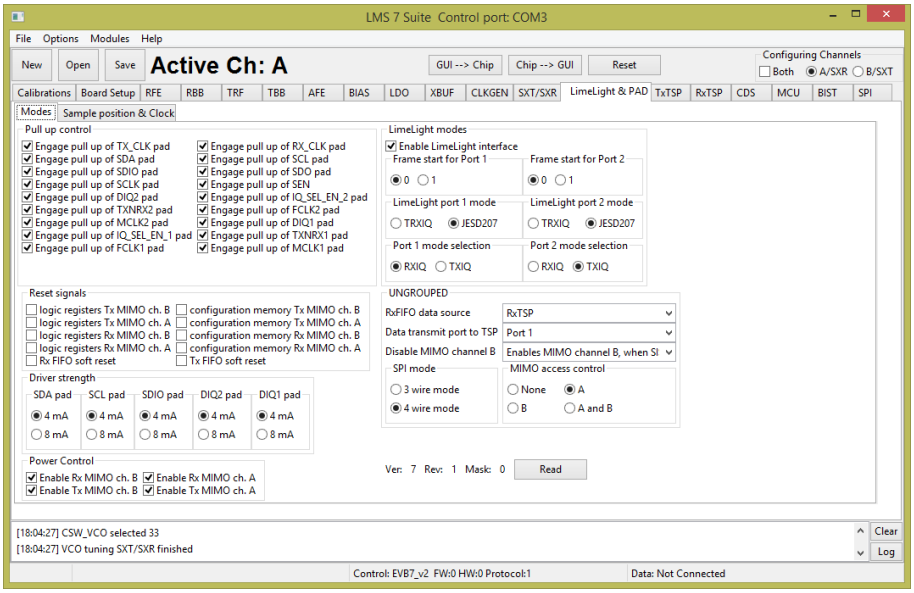

Figure 41 GUI Limelight & PAD Modes tab

The LimeLight tab has two sections:

- Modes
- Sample position & Clock

A picture of the tab is shown in *Figure 41*. A description of each function available in the 'Modes' tab is shown below in *Table 18*.

Table 18 GUI Limelight & PAD Modes control description

Parameter	Description
Pull up control	
Engage pull up of TXCLK pad	Controls Pull up resistor of TX_CLK pad. Pull-up enabled by default.
Engage pull up of SDA pad	Controls Pull up resistor of SDA pad. Pull-up enabled by default.
Engage pull up of SDIO pad	Controls Pull up resistor of SDIO pad. Pull-up enabled by default.
Engage pull up of SCLK pad	Controls Pull up resistor of SCLK pad. Pull-up enabled by default.
Engage pull up of DIQ2 pad	Controls Pull up resistor of DIQ2 pad. Pull-up enabled by default.
Engage pull up of TXNRX2 pad	Controls Pull up resistor of TXNRX2 pad. Pull-up enabled by default.
Engage pull up of MCLK2 pad	Controls Pull up resistor of MCLK2 pad. Pull-up enabled by default.
Engage pull up of IQSELEN1 pad	Controls Pull up resistor of IQSELEN1 pad. Pull-up enabled by default.
Engage pull up of FCLK1 pad	Controls Pull up resistor of FCLK1 pad. Pull-up enabled by default.
Engage pull up of RXCLK pad	Controls Pull up resistor of RXCLK1 pad. Pull-up enabled by default.
Engage pull up of SCL pad	Controls Pull up resistor of SCL pad. Pull-up enabled by default.
Engage pull up of SDO pad	Controls Pull up resistor of SDO pad. Pull-up enabled by default.
Engage pull up of SEN pad	Controls Pull up resistor of SEN pad. Pull-up enabled by default.

Engage pull up of IQSELEN2 pad	Controls Pull up resistor of IQSELEN2 pad. Pull-up enabled by default.
Engage pull up of FCLK2 pad	Controls Pull up resistor of FCLK2 pad. Pull-up enabled by default.
Engage pull up of DIQ1 pad	Controls Pull up resistor of DIQ1 pad. Pull-up enabled by default.
Engage pull up of TXNRX1 pad	Controls Pull up resistor of TXNRX1 pad. Pull-up enabled by default.
Engage pull up of MCLK1 pad	Controls Pull up resistor of MCLK1 pad. Pull-up enabled by default.
Reset Signals	
Logic registers Tx MIMO ch. B	Resets all registers to the default state for Tx MIMO channel B logic. By default RESET inactive.
Logic registers Tx MIMO ch. A	Resets all registers to the default state for Tx MIMO channel A logic. By default RESET inactive.
Logic registers Rx MIMO ch. B	Resets all registers to the default state for Rx MIMO channel B logic. By default RESET inactive.
Logic registers Rx MIMO ch. A	Resets all registers to the default state for Rx MIMO channel A logic. By default RESET inactive.
Rx FIFO soft reset	Soft reset of LimeLight RX FIFO registers. By default RESET inactive.
Configuration memory Tx MIMO ch. B	Resets configuration memory to the default state for Tx MIMO channel B logic. By default RESET inactive.
Configuration memory Tx MIMO ch. A	Resets configuration memory to the default state for Tx MIMO channel A logic. By default RESET inactive.
Configuration memory Rx MIMO ch. B	Resets configuration memory to the default state for Rx MIMO channel B logic. By default RESET inactive.
Configuration memory Rx MIMO ch. A	Resets configuration memory to the default state for Rx MIMO channel A logic. By default RESET inactive.
Tx FIFO soft reset	Soft reset of LimeLight TX FIFO registers. By default RESET inactive.
Driver strength	
SDA pad	Set SDA pad driver strength to 4mA or 8 mA. By default set to 4 mA.
SCL pad	Set SCL pad driver strength to 4mA or 8 mA. By default set to 4 mA.
SDIO pad	Set SDIO pad driver strength to 4mA or 8 mA. By default set to 4 mA.
DIQ2 pad	Set DIQ2 pad driver strength to 4mA or 8 mA. By default set to 4 mA.
DIQ1 pad	Set DIQ1 pad driver strength to 4mA or 8 mA. By default set to 4 mA.
Power Control	
Enable Rx MIMO ch. B	Enables Rx MIMO B channel. Enabled by default.
Enable Tx MIMO ch. B	Enables Tx MIMO B channel. Enabled by default.
Enable Rx MIMO ch. A	Enables Rx MIMO A channel. Enabled by default.
Enable Tx MIMO ch. A	Enables Tx MIMO A channel. Enabled by default.
LimeLight modes	
Enable LimeLight interface	Enables LimeLight interface. By default enabled.
Frame start for Port1	Selects frame start ID for Port 1, can be set to ‘0’ or ‘1’. By default set to ‘0’.
Frame start for Port2	Selects frame start ID for Port 2, can be set to ‘0’ or ‘1’. By default set to ‘0’.
LimeLight port1 mode	Select mode for Port 1: T TRXIQ or JESD207. By default set to JESD207.
LimeLight port2 mode	Select mode for Port 2: T TRXIQ or JESD207. By default set to JESD207.
Port 1 mode selection	IQSEL selection for Port 1: RXIQ or TXIQ. By default set to RXIQ.
Port 2 mode selection	IQSEL selection for Port 2: RXIQ or TXIQ. By default set to TXIQ.
UNGROUPED	
RxFIFO data source	RxFIFO data source selection: RxTSP, TxFIFO, LFSR. By default set to RxTSP.
Data transmit port to TSP	Port selection for data transmit to TSP.
Disable MIMO channel B	MIMO channel B enable control.
SPI mode	SPI mode control.
MIMO access control	MIMO access control.

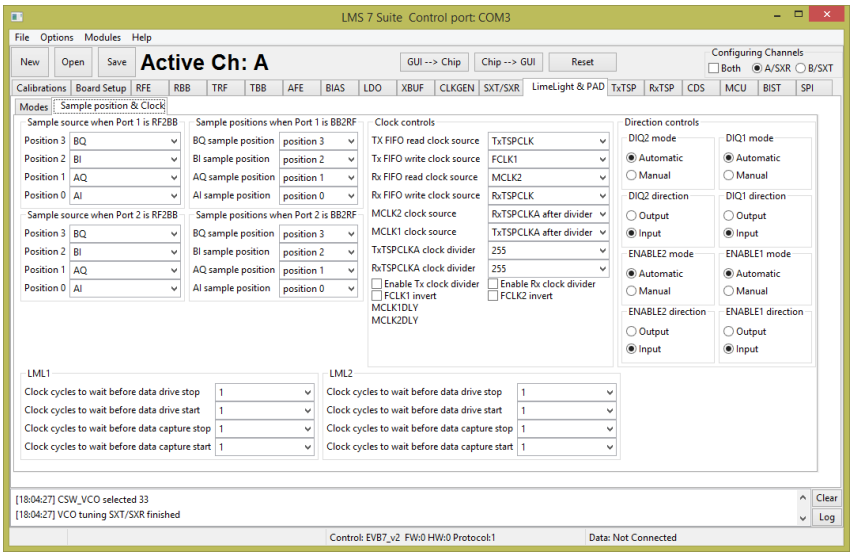

Figure 42 GUI Limelight & PAD Sample position tab

A picture of the tab is shown in *Figure 42*. Description of each function available from the 'Sample position & Clock' page is shown below in *Table 19*.

Table 19 GUI Limelight&PAD Sample position control description

Parameter	Description
Sample source when Port1 is RF2BB	
Position 3	Select sample source of the position 3: BQ, BI, AQ or AI. By default BQ is selected.
Position 2	Select sample source of the position 2: BQ, BI, AQ or AI. By default BI is selected.
Position 1	Select sample source of the position 1: BQ, BI, AQ or AI. By default AQ is selected.
Position 0	Select sample source of the position 0: BQ, BI, AQ or AI. By default AI is selected.
Sample source when Port2 is RF2BB	
Position 3	Select sample source of the position 3: BQ, BI, AQ or AI. By default BQ is selected.
Position 2	Select sample source of the position 2: BQ, BI, AQ or AI. By default BI is selected.
Position 1	Select sample source of the position 1: BQ, BI, AQ or AI. By default AQ is selected.
Position 0	Select sample source of the position 0: BQ, BI, AQ or AI. By default AI is selected.
Sample source when Port1 is BB2RF	
BQ sample position	Select BQ sample position in frame. Position: 3, 2, 1, or 0. By default position set to 3.
BI sample position	Select BI sample position in frame. Position: 3, 2, 1, or 0. By default position set to 2.
AQ sample position	Select AQ sample position in frame. Position: 3, 2, 1, or 0. By default position set to 1.
AI sample position	Select AI sample position in frame. Position: 3, 2, 1, or 0. By default position set to 0.
Sample source when Port2 is BB2RF	
BQ sample position	Select BQ sample position in frame. Position: 3, 2, 1, or 0. By default position set to 3.
BI sample position	Select BI sample position in frame. Position: 3, 2, 1, or 0. By default position set to 2.
AQ sample position	Select AQ sample position in frame. Position: 3, 2, 1, or 0. By default position set to 1.
AI sample position	Select AI sample position in frame. Position: 3, 2, 1, or 0. By default position set to 0.
Clock controls	
TX FIFO read clock source	Select TX FIFO read clock source: TxTSPCLK, FCKL1 or FCKL2. By default TxTSPCLK is selected.
TX FIFO write clock source	Select TX FIFO write clock source: FCKL1, FCKL2 or RxTSPCLK. By default FCKL1 is selected.

RX FIFO read clock source	Select RX FIFO read clock source: MCKL1, MCKL2, FCKL1 or FCKL2. By default MCKL2 is selected.
RX FIFO write clock source	Select RX FIFO write clock source: FCKL1, FCKL2 or RxTSPCLK. By default RxTSPCLK is selected.
MCLK2 clock source	Select MCKL2 clock source from: RxTSPCLKA, TxTSPCLKA, RxTSPCLKA after divider or TxTSPCLKA after divider. By default RxTSPCLK after divider is selected.
MCLK1 clock source	Select MCKL1 clock source from: RxTSPCLKA, TxTSPCLKA, RxTSPCLKA after divider or TxTSPCLKA after divider. By default TxTSPCLK after divider is selected.
TxTSPCLKA clock divider	TxTSP clock divider, used to produce MCLK(1/2) clocks. Control range from 0 to 255. By default set to 255.
RxTSPCLKA clock divider	RxTSP clock divider, used to produce MCLK(1/2) clocks. Control range from 0 to 255. By default set to 255.
Enable Tx clock divider	Enables Tx clock divider. Set to enable by default.
FCLK1 invert	Inverts FCLK1 clock. By default clock is not inverted.
Enable Rx clock divider	Enables Rx clock divider. Set to enable by default.
FCLK2 invert	Inverts FCLK2 clock. By default clock is not inverted.
MCLK1DLY	Select MCLK1 clock delay. By default clock not delayed.
MCLK2DLY	Select MCLK2 clock delay. By default clock not delayed.
Direction controls	
DIQ2 mode	DIQ2 direction control mode. By default set to Automatic.
DIQ1 mode	DIQ1 direction control mode. By default set to Automatic.
DIQ2 direction	DIQ2 direction. By default set to Input.
DIQ1 direction	DIQ1 direction. By default set to Input.
ENABLE2 mode	ENABLE2 direction control mode. By default set to Automatic.
ENABLE1 mode	ENABLE1 direction control mode. By default set to Automatic.
ENABLE2 direction	ENABLE2 direction. By default set to Input.
ENABLE1 direction	ENABLE1 direction. By default set to Input.
LML1	
Clock cycles to wait before data drive stop	Controls the number of clock cycles to wait before data drive stop after burst stop is detected in JESD207 mode on Port 1 and Port 1 is transmitter. By default set to 1.
Clock cycles to wait before data drive start	Controls the number of clock cycles to wait before data drive stop after burst start is detected in JESD207 mode on Port 1 and Port 1 is transmitter. By default set to 1.
Clock cycles to wait before data capture stop	Controls the number of clock cycles to wait before data capture stop after burst stop is detected in JESD207 mode on Port 1 and Port 1 is receiver. By default set to 1.
Clock cycles to wait before data capture start	Controls the number of clock cycles to wait before data capture stop after burst start is detected in JESD207 mode on Port 1 and Port 1 is receiver. By default set to 1.
LML2	
Clock cycles to wait before data drive stop	Controls the number of clock cycles to wait before data drive stop after burst stop is detected in JESD207 mode on Port 1 and Port 1 is transmitter. By default set to 1.
Clock cycles to wait before data drive start	Controls the number of clock cycles to wait before data drive stop after burst start is detected in JESD207 mode on Port 1 and Port 1 is transmitter. By default set to 1.
Clock cycles to wait before data capture stop	Controls the number of clock cycles to wait before data capture stop after burst stop is detected in JESD207 mode on Port 1 and Port 1 is receiver. By default set to 1.
Clock cycles to wait before data capture start	Controls the number of clock cycles to wait before data capture stop after burst start is detected in JESD207 mode on Port 1 and Port 1 is receiver. By default set to 1.
Direction controls	
DIQ2 mode	DIQ2 direction control mode for port 2. Set to Automatic by default.
DIQ1 mode	DIQ1 direction control mode for port 1. Set to Automatic by default.
DIQ2 direction	DIQ2 direction. Set to input by default.
DIQ1 direction	DIQ1 direction. Set to input by default.
ENABLE2 mode	ENABLE2 direction control mode. Set to Automatic by default.
ENABLE1 mode	ENABLE1 direction control mode. Set to Automatic by default.
ENABLE2 direction	ENABLE2 direction. Set to input by default.

ENABLE1 direction	ENABLE1 direction. Set to input by default.

7.18 TxTSP

The TxTSP tab controls the digital blocks of TxTSPA and TxTSPB modules.

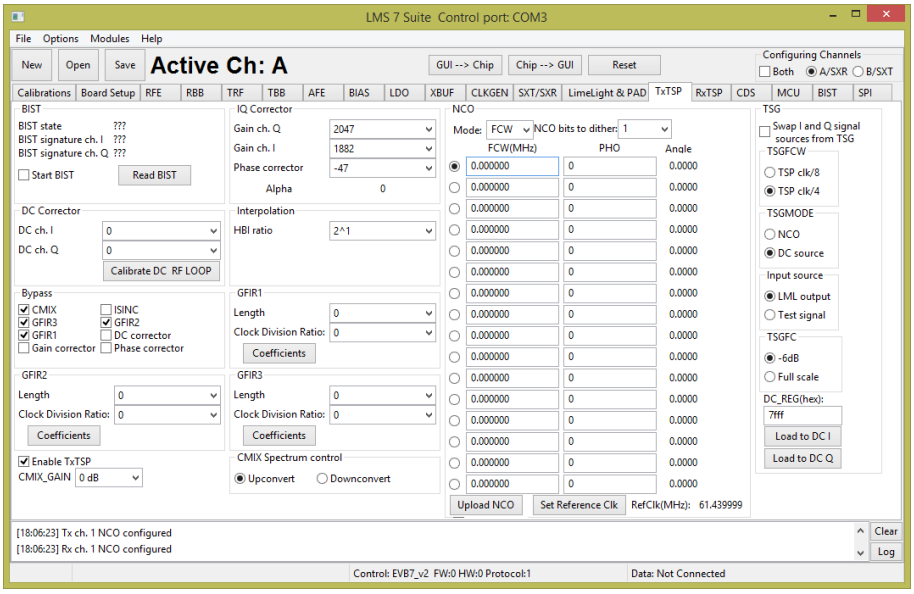

Figure 43 GUI TxTSP tab

A picture of the tab is shown in *Figure 43*. A description of each function available in this tab is shown below in *Table 20*.

Table 20 GUI TxTSP control description

Parameter	Description
Enable TxTSP	Enables TxTSP modules enable. Enabled by default.
CMIX_GAIN	CMIX gain control. Control range from -6 dB to +6 dB. Step size 6 dB. Set to 0 dB by default.
CMIX Spectrum control	Spectrum control of CMIX. By default set to downconvert.
Start BIST	Starts TxTSP built-in self-test. Keep it at 1 one at least three clock cycles.
Bypass	
CMIX	Bypass CMIX module when selected.
GFIR3	Bypass GFIR3 module when selected.
GFIR1	Bypass GFIR1 module when selected.
Gain correction	Bypass Gain correction module when selected.
ISINC	Bypass ISINC module when selected.
GFIR2	Bypass GFIR2 module when selected.
DC Correction	Bypass DC correction module when selected.
Phase corrector	Bypass Phase correction module when selected.
GFIR1	
Length	Set GFIR parameter I. Control range from 0 to 7.
Clock Division Ration	Sets GFIR filter clock division ration. Control range from 0 to 255.
Coefficients	Sets/Load GFIR filters coefficients. By default all set to 0.

GFIR2	
Length	Set GFIR parameter I. Control range from 0 to 7.
Clock Division Ration	Sets GFIR filter clock division ration. Control range from 0 to 255.
Coefficients	Sets/Load GFIR filters coefficients. By default all set to 0.
GFIR3	
Length	Set GFIR parameter I. Control range from 0 to 7.
Clock Division Ration	Sets GFIR filter clock division ration. Control range from 0 to 255.
Coefficients	Sets/Load GFIR filters coefficients. By default all set to 0.
DC Corrector	
DC ch. I	Sets DC corrector value to channel I. Control range from -128 to 128. By default 0.
DC ch. Q	Sets DC corrector value to channel Q. Control range from -128 to 128. By default 0.
IQ Corrector	
Gain ch. Q	Sets Gain corrector value to channel Q. Control range from 0 to 2047. By default 2047.
Gain ch. I	Sets Gain corrector value to channel I. Control range from 0 to 2047. By default 2047.
Phase corrector	Sets Phase corrector value. Control range from 0 to 2047. By default 0.
Interpolation	
HBI ratio	Sets HBI interpolation ratio. Possible control values 2, 4, 8, 16, 32 and bypass. By default bypassed.
TSG	
Swap I and Q signal source from TSG	Swap IQ signals at test signal generator's output. By default not selected.
TSGFCW	Select frequency generated by test NCO. By default TSG frequency set to the TSP clock divided by 8.
TSGMODE	Select test signal generator mode: NCO or DC. By default NCO is selected.
Input Source	Select input source to TSP: LML output or TSG. By default LML output is selected.
TSGC	TSG full scale control: 0 dB or -6 dB. By default set to -6 dB.
Load DC to I	Load TSG DC I register with value from DC_REG (hex) box.
Load ED to Q	Load TSG DC Q register with value from DC_REG (hex) box.
NCO	
Mode	Selects the CW or PHO (Phase offset) mode for NCO.
NCO bits to dither	Selects number of bits for NCO dithering.
FCW(MHz)	Type wanted NCO frequency.
Set Reference Clk	Set reference frequency for NCO. The frequency the same as TSP block.
Upload NCO	Program NCO

7.19 RxTSP

The RxTSP tab controls the digital blocks of RxTSPA and RxTSPB modules. A picture of the tab is shown in *Figure 44*. A description of each function available in this tab is shown below in *Table* 21.

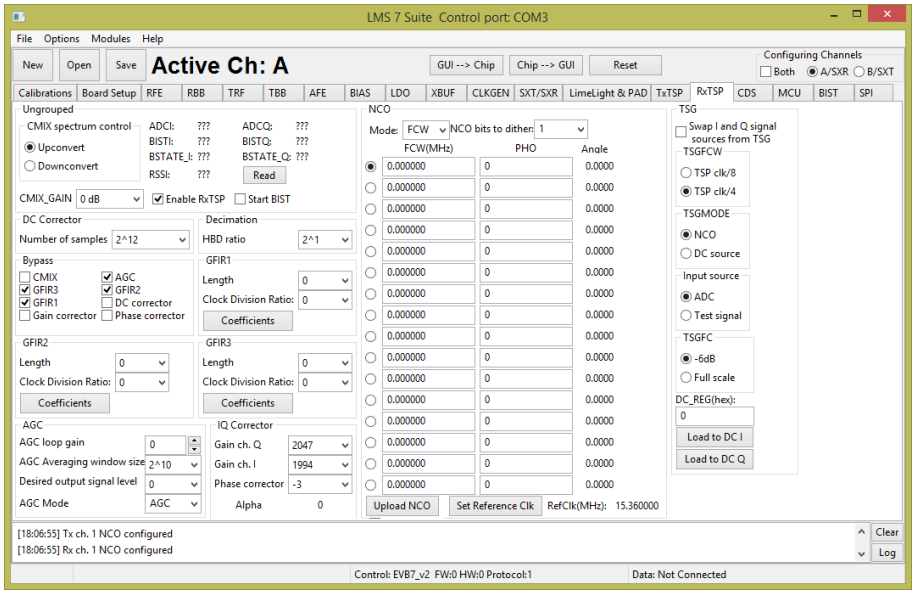

Figure 44 GUI RxTSP tab

Table 21 GUI RxTSP control description

Parameter	Description
Enable RxTSP	Enables TxRSP modules enable. Enabled by default.
CMIX_GAIN	CMIX gain control. Control range from -6 dB to +6 dB. Step size 6 dB. Set to 0 dB by default.
CMIX Spectrum control	Spectrum control of CMIX. By default set to downconvert.
Start BIST	Starts RxTSP built-in self-test. Keep it at 1 one for at least three clock cycles
Bypass	
CMIX	Bypass CMIX module when selected.
GFIR3	Bypass GFIR3 module when selected.
GFIR1	Bypass GFIR1 module when selected.
Gain correction	Bypass Gain correction module when selected.
AGC	Bypass AGC module when selected.
GFIR2	Bypass GFIR2 module when selected.
DC Correction	Bypass DC corrector module when selected.
Phase correction	Bypass Phase corrector module when selected.
GFIR1	
Length	Set GFIR parameter I. Control range from 0 to 7.
Clock Division Ration	Sets GFIR filter clock division ration. Control range from 0 to 255.
Coefficients	Sets/Load GFIR filters coefficients. By default all set to 0.
GFIR2	
Length	Set GFIR parameter I. Control range from 0 to 7.

Clock Division Ration	Sets GFIR filter clock division ration. Control range from 0 to 255.
Coefficients	Sets/Load GFIR filters coefficients. By default all set to 0.
GFIR3	
Length	Set GFIR parameter I. Control range from 0 to 7.
Clock Division Ration	Sets GFIR filter clock division ration. Control range from 0 to 255.
Coefficients	Sets/Load GFIR filters coefficients. By default all set to 0.
DC Corrector	
Numbers of samples	Select the number of samples to average for Automatic DC corrector.
IQ Corrector	
Gain ch. Q	Sets Gain corrector value to channel Q. Control range from 0 to 2047. By default 2047.
Gain ch. I	Sets Gain corrector value to channel I. Control range from 0 to 2047. By default 2047.
Phase corrector	Sets Phase corrector value. Control range from 0 to 2047. By default 0.
Decimation	
HBD ratio	Sets HBD interpolation ratio. Possible control values 2, 4, 8, 16, 32 and bypass. By default bypassed.
TSG	
Swap I and Q signal source from TSG	Swap IQ signals at test signal generator's output. By default not selected.
TSGFCW	Select frequency generated by test NCO. By default TSG frequency set to the TSP clock divided by 8.
TSGMODE	Select test signal generator mode: NCO or DC. By default NCO is selected.
Input Source	Select input source to TSP: ADC input or TSG. By default LML output is selected.
TSGC	TSG full scale control: 0 dB or -6 dB. By default set to -6 dB.
Load DC to I	Load TSG DC I register with value from DC_REG (hex) box.
Load ED to Q	Load TSG DC Q register with value from DC_REG (hex) box.
NCO	
Mode	Selects the CW or PHO (Phase offset) mode for NCO.
NCO bits to dither	Selects number of bits for NCO dithering.
FCW(MHz)	Type wanted NCO frequency.
PHO	Type wanted PHO frequency.
Set Reference Clk	Set reference frequency for NCO. The frequency is the same as the TSP block.
Upload NCO	Program NCO
AGC	
AGC Mode	Selects the AGC mode: Bypass, AGC, RSSI mode.
AGC loop gain	Selects AGC loop gain.
AGC Average window size	AGC averaging window size is $2^{(AGC\_AVG + 7)}$.
Desired output level	Selects desired output signal level

7.20 CDS

The Clock Distribution System (CDS) controls are described in this this chapter.

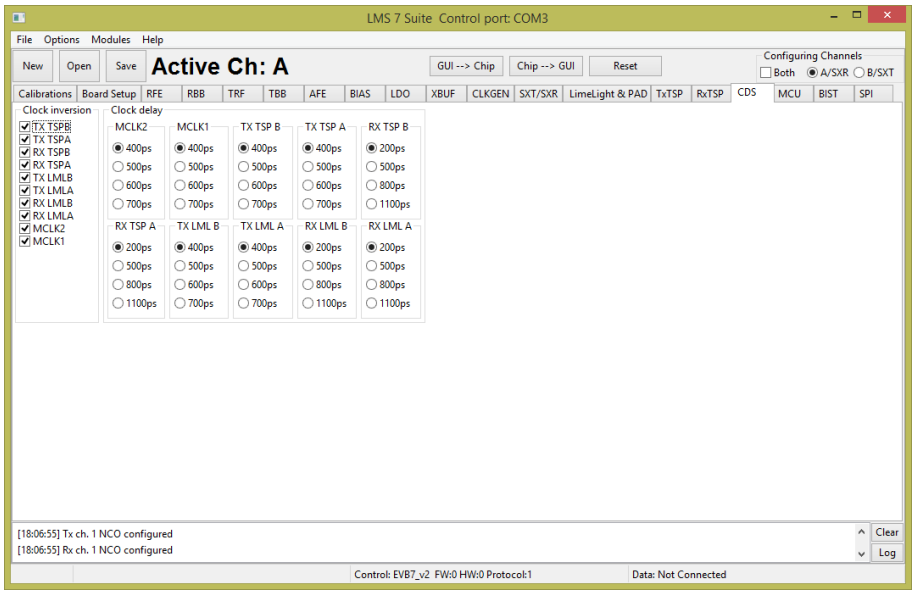

Figure 45 GUI CDS tab

A picture of the tab is shown in *Figure 45*. A description of each function available in this tab is shown below in *Table 22*.

Table 22 GUI CDS control description

Parameter	Description
Clock inversion	
TX TSPB	TX TSP B channel clock inversion controls. By default clock is not inverted.
TX TSPA	TX TSP A channel clock inversion controls. By default clock is not inverted.
RX TSPB	RX TSP B channel clock inversion controls. By default clock is not inverted.
RX TSPA	RX TSP A channel clock inversion controls. By default clock is not inverted.
TX LMLB	TX LML interface B channel clock inversion control. By default clock is not inverted.
TX LMLA	TX LML interface A channel clock inversion control. By default clock is not inverted.
RX LMLB	RX LML interface B channel clock inversion control. By default clock is not inverted.
RX LMLA	RX LML interface A channel clock inversion control. By default clock is not inverted.
MCKL2	MCLK2 clock inversion control. By default clock is not inverted.
MCKL1	MCLK1 clock inversion control. By default clock is not inverted.
Clock delay	
MCLK2	MCLK2 clock delays. Clock can be delayed by 400 ps, 500 ps, 600 ps and 700 ps. By default clock delayed 400 ps.
MCLK1	MCLK1 clock delays. Clock can be delayed by 400 ps, 500 ps, 600 ps and 700 ps. By default clock delayed 400 ps.
TX TSP B	TX TSP B clock delays. Clock can be delayed by 400 ps, 500 ps, 600 ps and 700 ps. By default clock delayed 400 ps.
TX TSP A	TX TSP A clock delays. Clock can be delayed by 400 ps, 500 ps, 600 ps and 700 ps. By default clock delayed 400 ps.

RX TSP B	RX TSP B clock delay. Clock can be delayed by 200 ps, 500 ps, 800 ps and 1100 ps. By default clock delayed 200 ps.
RX TSP A	RX TSP A clock delay. Clock can be delayed by 200 ps, 500 ps, 800 ps and 1100 ps. By default clock delayed 200 ps.
TX LML B	TX LML B clock delay. Clock can be delayed by 400 ps, 500 ps, 600 ps and 700 ps. By default clock delayed 400 ps.
TX LML A	TX LML A clock delay. Clock can be delayed by 400 ps, 500 ps, 600 ps and 700 ps. By default clock delayed 400 ps.
RX LML B	RX LML B clock delay. Clock can be delayed by 200 ps, 500 ps, 800 ps and 1100 ps. By default clock delayed 200 ps.
RX LML A	RX LML A clock delay. Clock can be delayed by 200 ps, 500 ps, 800 ps and 1100 ps. By default clock delayed 200 ps.

7.21 BIST

The Build-In Self-Test (BIST) modules for SXT, SXR and CGEN controls are described in this chapter.

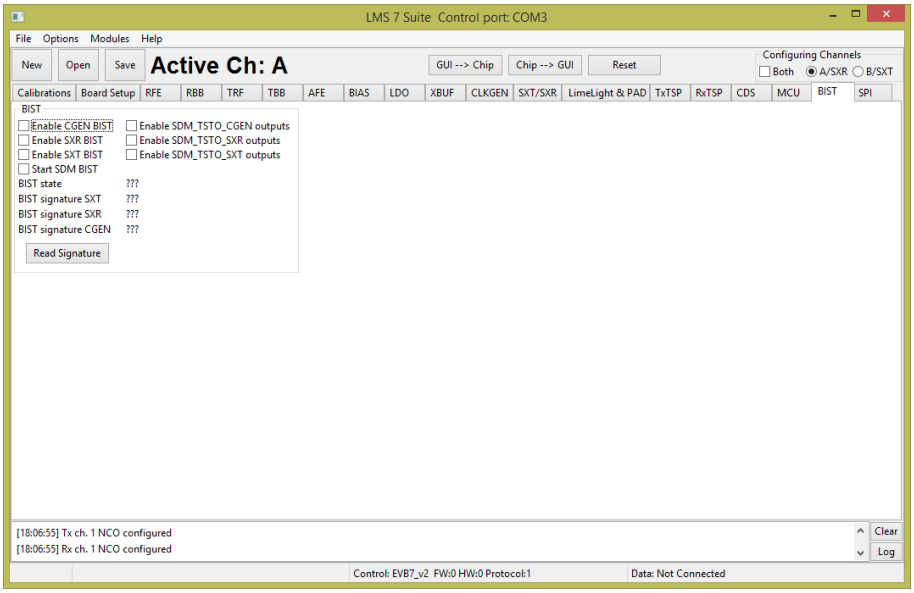

Figure 46 GUI BIST tab

The BIST modules are used for the test proposes only. There is one test vector generator which supplies the test vectors for CGEN, SXT and SXR modules. After pressing the 'Read BIST' button the test results (test vector signature) will be displayed for the selected block.

A picture of the tab is shown in *Figure 46*. A description of each function available in this tab is shown below in *Table 23*.

Table 23 GUI BIST control description

Parameter	Description
BIST	
Enable CGEN BIST	Enables CGEN BIST. Disabled by default.
Enable SXR BIST	Enables SXR BIST
Enable SXT BIST	Enables SXT BIST
Start SDM BIST	Starts SDM BIST
Enable SMD_TSTO_CGEN outputs	Enables SMD_TSTO_CGEN outputs
Enable SMD_TSTO_SXR outputs	Enables SMD_TSTO_SXR outputs
Enable SMD_TSTO_SXT outputs	Enables SMD_TSTO_SXT outputs

7.22 SPI

This is used for test proposes only. Using this tab, every SPI register can be programmed using the register map description. Every SPI register of the LMS7002M can be read back. A picture of the tab is shown in *Figure 47*. A description of each function available in this tab is shown below in *Table 24*.

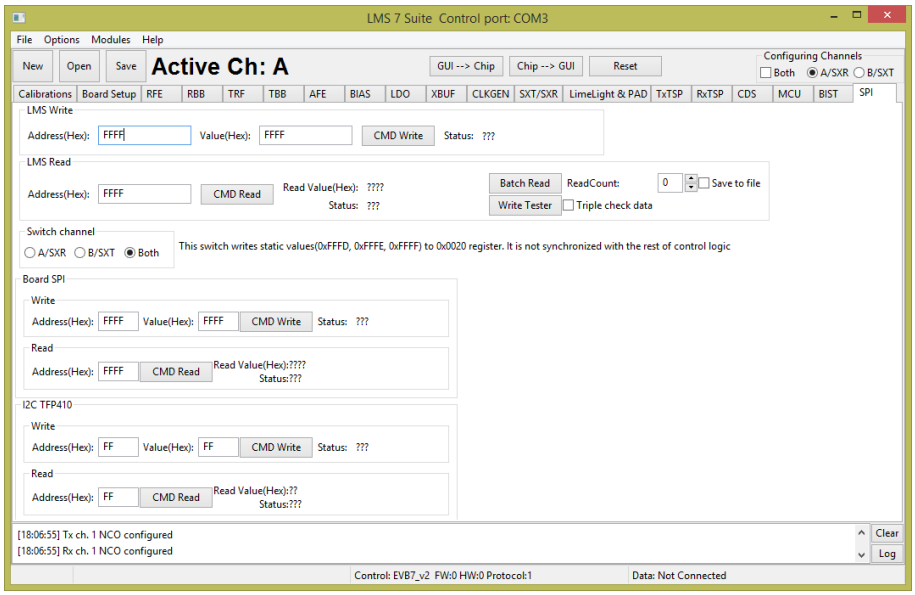

Figure 47 GUI SPI tab

Table 24 GUI SPI control description

Parameter	Description
LMS Write	
Address (Hex)	Register address in HEX format.
Value (Hex)	Register value in HEX format.
Status	Previously executed command status.
LMS Read	
Address (Hex)	Register address in HEX format.
Read Values (Hex)	Register value in HEX format.
Status	Previously executed command status.
Batch Read	Executes multiple reads from selected register. The read number selected by ReadCount.
ReadCount	Set read back function count number.
Write Tester	Writes and read to selected register 100 times**.**
Triple check data	When selected repeats function three times.
Save to file	If selected save function results to txt file to selected location.
Switch channel	Selects read/write channel.
Board SPI Write	
Address (Hex)	Register address in HEX format.
Value (Hex)	Register value in HEX format.
Status	Previously executed command status.
Board SPI Read	
Address (Hex)	Register address in HEX format.

Read Values (Hex)	Register value in HEX format.
Status	Previously executed command status.
I2C TFP410 Write	
Address (Hex)	Register address in HEX format.
Value (Hex)	Register value in HEX format.
Status	Previously executed command status.
I2C TFP410 Read	
Address (Hex)	Register address in HEX format.
Read Values (Hex)	Register value in HEX format.
Status	Previously executed command status.

8

Appendix A: Test Equipment Setup

8.1 Introduction

This section lists the recommended test equipment to use with the UNITE7002. It also provides detailed setup procedures for the Agilent MXG when used with UNITE7002. Note the set up procedure is only required when using the analogue TX inputs of the LMS7002M. This procedure is not required when the LMS7002M chip is driven digitally by a baseband processor.

8.2 Recommended Test Equipment

The following test equipment is recommended for the testing of UNITE7002. It is possible to use other test equipment, but the alternatives may not provide all the necessary features.

- N5182A MXG
  - Differential Arbitrary Waveform Generator Option 1EL
- N9020A MXA DC - 6 GHz
  - NF personality
  - Phase Noise personality
  - WCDMA personality
  - LTE personality
- Agilent Power Supply 5V
- Agilent 384C Noise Source
  - 15 dB ENR

8.3 Agilent MXG Setup

The front panel of the MXG is shown in *Figure 48*.

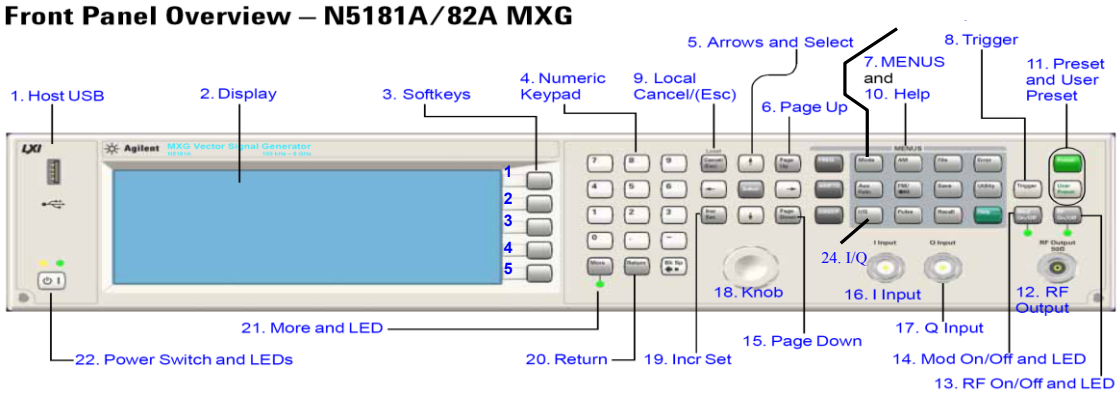

Figure 48 Agilent N5181A/82A MXG Front Panel

8.3.1. Setting Common Mode Voltage

To apply 0.3 V common mode offset voltage to the IQ outputs:

1. Press ‘IQ’ button (24)
2. Press ‘IQ offsets (on/off)’ softkey (3. softkey 4)
3. Press ‘external output adjustments’ softkey (3. softkey 4)
4. Press ‘Common Mode I/Q offset’ softkey (3. softkey 2)
5. type 0.3 on number pad (4), press ‘V’ softkey (3. softkey 1)
6. 0.3 V should appear on the display next to the ‘Common Mode I/Q offset’ softkey
7. Press return
    i. Check text next to ‘I/Q Adjustments’ softkey (3. softkey 1) highlights ‘off/on’
    ii. If not press ‘I/Q Adjustments’ softkey (3. softkey 1), highlighted section should alternate between on and off when pressed.
    iii. press return
    iv. Check text next to ‘I/Q’ softkey (3. softkey 1) highlights ‘off/on’
    v. If not press ‘I/Q’ softkey (3. softkey 1), highlighted section should alternate between on and off when pressed.

There should now be a 0.3 V common mode voltage on the differential IQ connections on the signal generator. This can be verified by measuring the DC level of each of the 4 differential I/Q lines with a multimeter.

Note: Very small DC offset levels in the transmit IQ path can result in LO breakthrough levels changing in the transmit chain. To eliminate or minimize this effect the following practices should be followed:

- The IQ cables should be of equal length
- Once I/Q gain and phase calibration is completed, connections should not be modified
- Cables and connections should not be moved once the I/Q gain and phase calibration is completed

8.3.2. Enabling the Arbitrary Waveform Generator

The arbitrary waveform generator will run test vectors which are downloaded to it. These can be generated either with Agilent's "Signal Studio" program or can be generated independently via "Matlab" or C.

Lime has a number of test vector files which are used for test and calibration of the LMS7002M as follows:

- DC.wfm – Differential DC tone for TX CW testing (clock 52 MHz)
- onetone1.wfm - single tone at 1 MHz offset for sideband suppression calibration/test (clock 52 MHz)
- twotone.wfm - two tone signal for linearity testing for MXG and LMS7002M use MXG IQ scaling factor of 30% (clock 52 MHz)
- wcdma31.wfm - TM2 WCDMA signal - use MXG IQ scaling factor of 30% (clock=15.36 MHz)
- EDGE3.wfm - GSM EDGE modulated test signal - (clock=13 MHz)

To download files to the signal generator follow the process described in section *8.3.3*.

To apply the correct file

1. Press 'Mode' button (23)
2. Press 'Dual Arb' softkey (3. softkey 1)
3. Press 'Select waveform' softkey (3. softkey 2)
4. Use up/down arrows (5) or spin knob (18) to select the wanted waveform from list.
5. Press 'Select waveform' softkey (3. softkey 1)
6. The name of the selected waveform should now be present in the display window
7. The soft key list should have moved up one level back to 'Arb'
8. Now change the Arb clock frequency
9. Press 'Arb setup' softkey (3. softkey 3)
10. Press 'Arb sample clock' softkey (3. softkey 1)
11. Type in the required frequency on the number pad eg for 13 MHz type '13' and press 'MHz' softkey (3. softkey 2)
12. The sample clock frequency should now be displayed on the screen.
13. Now scale the waveform data if necessary
14. Go to the 'Arb' softkey menu
    a) Either press the 'return' button from the 'Arb setup' menu or
    b) Press the 'Mode' button then 'Dual Arb softkey (3. softkey 1)

15. Press the 'More' button (21)
16. Press the 'Waveform Utilities' softkey (3. softkey 2)
17. Use the up/down arrows (5) or spin wheel to highlight the wanted waveform from the list.
18. Press the 'scale waveform data' softkey (3. softkey 2)
19. Type in the required scaling factor e.g.25%, type '25' on number pad and press '%' softkey (3. softkey 1).
    Note – even if the text next to 'scaling' softkey already states 25% (for example) this does not mean it has been applied to the waveform, still follow the process.
20. Press the 'Apply to waveform' softkey (3. softkey 4)
21. The progress bar will show on screen, soft menu will return to level up (Arb utilities).
22. Now return to the main 'Arb' Menu
    a) Press the 'return' button twice or
    b) Press the 'Mode' button then 'Dual Arb softkey (3. softkey 1)
23. Check that Arb in enabled
    a) 'Arb on/off' softkey (3. softkey 1) the text should have on highlighted 'Off / On'
    b) If not, press the 'Arb on/off' softkey (3. softkey 1) to toggle between on and off.
24. The modulation can be also be toggled on and off by the 'Mod on/off' button (just above the RF o/p connector). This must also be on – the green LED must be illuminated.
    a) Press the 'Mod on/off' button to toggle the modulation on and off.
    Note – The Mod on/off button turns the modulation on to the RF output and IQ output simultaneously. The RF does not need to be on for the IQ outputs to work

8.3.3. Downloading *.wfm Files to the Signal Generator

The following process should allow you to download files to the Agilent signal generator. The same process works for MXG and ESG.

This can be done via a network, however these instructions assume a direct connection between a PC running Windows 7 and the signal generator.

- Connect a cable between the PC network port and the signal generator LAN port.
- Check that the LEDs are illuminated on both ends to indicate that the HW is connected.
- Find the IP address of the Signal generator
  - Press the 'Utility' button
  - Press the 'I/O config' softkey (3. softkey 1)
  - Press the 'LAN setup' softkey (3. softkey 2)
  - The IP address should now be displayed on the screen
  - e.g.
    IP Address : 192.168.2.92
    Subnet Mask : 255.255.255.0
- Open a Command Prompt window on your PC
  - Start
  - In 'Search programs and files' window, type 'cmd'
  - The Command prompt window will pop-up
  - Alternatively, it is located at C:\Windows\System32\

- Linux users can use a terminal session with the same commands.

- To check the connection to the signal generator attempt to 'ping' it
  - Type 'ping 192.168.2.92' (or use your sig gen IP address)

    A successful ping result should be returned as shown in *Figure 49*.

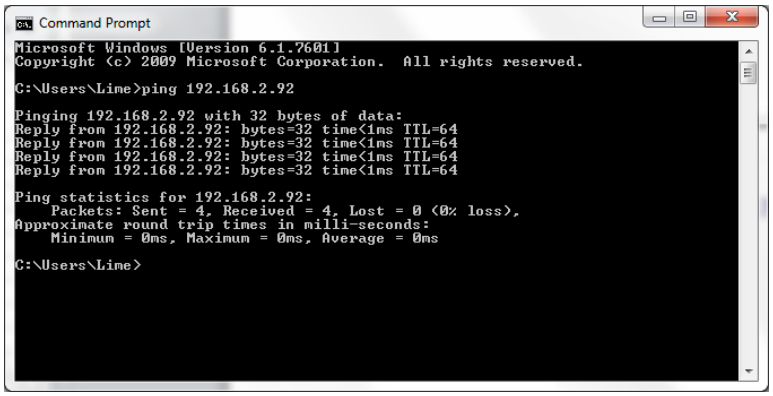

Figure 49 CMD window showing successful ping

To send wfm files to the signal generator the following procedure should be followed.

- Ensure that the wfm files are in a known directory e.g. 'C:\Lime\Waveform'
- In the 'Command Prompt' window set the directory to the one where the wfm files are located using the "CD" command
- Use FTP to send files to the signal generator
- Type 'ftp 192.168.2.92' as shown in *Figure 50*

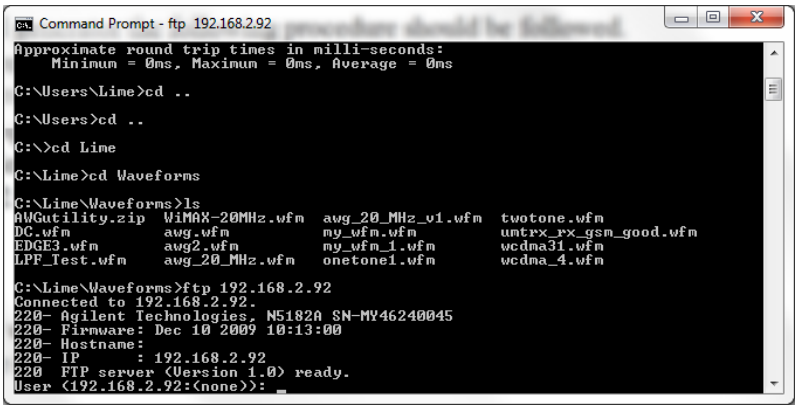

Figure 50 CMD window with ftp connection

- If you are correctly connected, then the above should be returned
- Press 'return' twice (for user name and password – none needed)
- Type 'cd bbg1'
- Type 'cd waveform'
- Type 'bin'

- Type ‘put wcdma31.wfm’
- The applied command copies files to the sig gen – repeat ‘put’ command for all files needed as shown in *Figure 51*

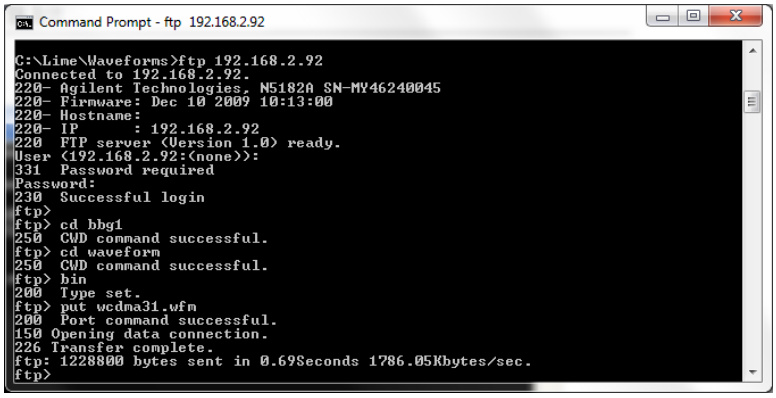

Figure 51 CMD window ftp file transfer

- To exit the ftp program type “bye”
- To close the ‘Command Prompt’ window type exit
- The wfm files should now be visible in the list of ARB files

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