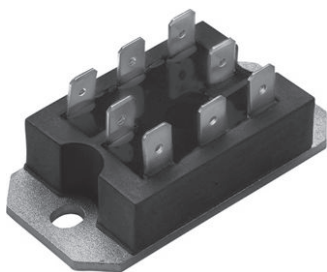



## Power Modules, Passivated Assembled Circuit Elements, 40 A


**PACE-PAK (D-19)**

### FEATURES

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200  $V_{RRM}/V_{DRM}$
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved 
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

### PRIMARY CHARACTERISTICS

$I_O$	40 A
Type	Modules - thyristor, standard
Package	PACE-PAK (D-19)

### DESCRIPTION

The VS-P400 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

### MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_O$	80 °C	40	A
$I_{TSM}$ , $I_{FSM}$	50 Hz 60 Hz	385 400	A
$I^2t$	50 Hz 60 Hz	745 680	A <sup>2</sup> s
$I^2\sqrt{t}$		7450	A <sup>2</sup> √s
$V_{RRM}$	Range	400 to 1200	V
$V_{ISOL}$		2500	V
$T_J$ , $T_{Stg}$		-40 to +125	°C

### ELECTRICAL SPECIFICATIONS

#### VOLTAGE RATINGS

TYPE NUMBER	$V_{RRM}/V_{DRM}$ , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{RRM}$ MAXIMUM AT $T_J$ MAXIMUM mA
VS-P401, VS-P421, VS-P431	400	500	10
VS-P402, VS-P422, VS-P432	600	700	
VS-P403, VS-P423, VS-P433	800	900	
VS-P404, VS-P424, VS-P434	1000	1100	
VS-P405, VS-P425, VS-P435	1200	1300	



ON-STATE CONDUCTION							
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum DC output current at case temperature	I <sub>O</sub>	Full bridge circuits			40	A	
					80	°C	
Maximum peak, one-cycle non-repetitive on-state or forward current	I <sub>TSM</sub> , I <sub>FSM</sub>	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T <sub>J</sub> = T <sub>J</sub> maximum	385	A	
		t = 8.3 ms			400		
		t = 10 ms	100 % V <sub>RRM</sub> reapplied		325		A <sup>2</sup> s
		t = 8.3 ms			340		
Maximum I <sup>2</sup> t for fusing	I <sup>2</sup> t	t = 10 ms	No voltage reapplied		745		
		t = 8.3 ms			680		
		t = 10 ms	100 % V <sub>RRM</sub> reapplied		530		
		t = 8.3 ms			480		
Maximum I <sup>2</sup> √t for fusing	I <sup>2</sup> √t	t = 0.1 ms to 10 ms, no voltage reapplied I <sup>2</sup> t for time tx = I <sup>2</sup> √t · √tx			7450	A <sup>2</sup> √s	
Low level value of threshold voltage	V <sub>T(TO)1</sub>	(16.7 % x π x I <sub>T(AV)</sub> ) < I < π x I <sub>T(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum			0.83	V	
High level value of threshold voltage	V <sub>T(TO)2</sub>	(I > π x I <sub>T(AV)</sub> ), T <sub>J</sub> = T <sub>J</sub> maximum			1.03		
Low level value of on-state slope resistance	r <sub>t1</sub>	(16.7 % x π x I <sub>T(AV)</sub> ) < I < π x I <sub>T(AV)</sub> , T <sub>J</sub> = T <sub>J</sub> maximum			9.61	mΩ	
High level value of on-state slope resistance	r <sub>t2</sub>	(I > π x I <sub>T(AV)</sub> ), T <sub>J</sub> = T <sub>J</sub> maximum			7.01		
Maximum on-state voltage drop	V <sub>TM</sub>	I <sub>TM</sub> = π x I <sub>T(AV)</sub>		T <sub>J</sub> = 25 °C	1.4	V	
Maximum forward voltage drop	V <sub>FM</sub>	I <sub>FM</sub> = π x I <sub>F(AV)</sub>		T <sub>J</sub> = 25 °C	1.4	V	
Maximum non-repetitive rate of rise of turned-on current	di/dt	T <sub>J</sub> = 125 °C from 0.67 V <sub>DRM</sub> I <sub>TM</sub> = π x I <sub>T(AV)</sub> , I <sub>g</sub> = 500 mA, t <sub>r</sub> < 0.5 μs, t <sub>p</sub> > 6 μs			200	A/μs	
Maximum holding current	I <sub>H</sub>	T <sub>J</sub> = 25 °C anode supply = 6 V, resistive load			130	mA	
Maximum latching current	I <sub>L</sub>				250		

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T <sub>J</sub> = 125 °C, exponential to 0.67 V <sub>DRM</sub> gate open	200	V/μs
Maximum peak reverse and off-state leakage current at V <sub>RRM</sub> , V <sub>DRM</sub>	I <sub>RRM</sub> , I <sub>DRM</sub>	T <sub>J</sub> = 125 °C, gate open circuit	10	mA
Maximum peak reverse leakage current	I <sub>RRM</sub>	T <sub>J</sub> = 25 °C	100	μA
RMS isolation voltage	V <sub>ISOL</sub>	50 Hz, circuit to base, all terminals shorted, T <sub>J</sub> = 25 °C, t = 1 s	2500	V

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum peak gate power	P <sub>GM</sub>			8	W	
Maximum average gate power	P <sub>G(AV)</sub>			2		
Maximum peak gate current	I <sub>GM</sub>			2	A	
Maximum peak negative gate voltage	-V <sub>GM</sub>			10	V	
Maximum gate voltage required to trigger	V <sub>GT</sub>	T <sub>J</sub> = - 40 °C	Anode supply = 6 V resistive load	3	V	
		T <sub>J</sub> = 25 °C		2		
		T <sub>J</sub> = 125 °C		1		
Maximum gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = - 40 °C		90	mA	
		T <sub>J</sub> = 25 °C		60		
		T <sub>J</sub> = 125 °C		35		
Maximum gate voltage that will not trigger	V <sub>GD</sub>	T <sub>J</sub> = 125 °C, rated V <sub>DRM</sub> applied		0.2	V	
Maximum gate current that will not trigger	I <sub>GD</sub>			2	mA	

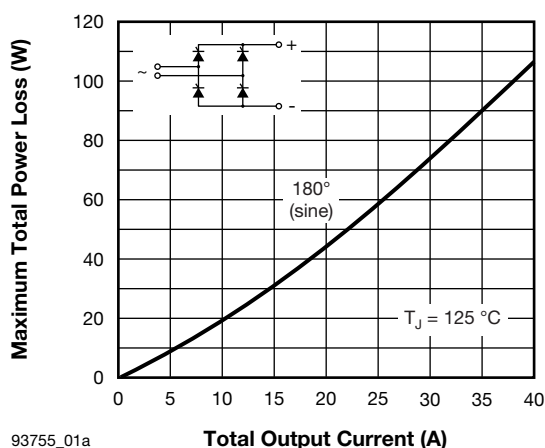


## THERMAL AND MECHANICAL SPECIFICATIONS

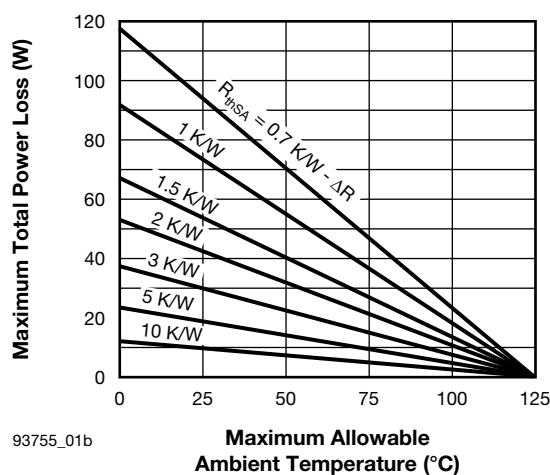
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating and storage temperature range	$T_J, T_{Stg}$		-40 to +125	°C
Maximum thermal resistance, junction to case per junction	$R_{thJC}$	DC operation	1.05	K/W
Maximum thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth and greased	0.10	
Mounting torque, base to heatsink <sup>(1)</sup>			4	Nm
Approximate weight			58	g
			2.0	oz.
Case style			PACE-PAK (D-19)	

### Note

<sup>(1)</sup> A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound

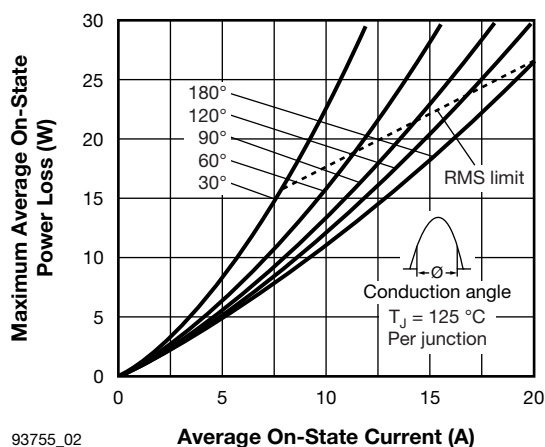


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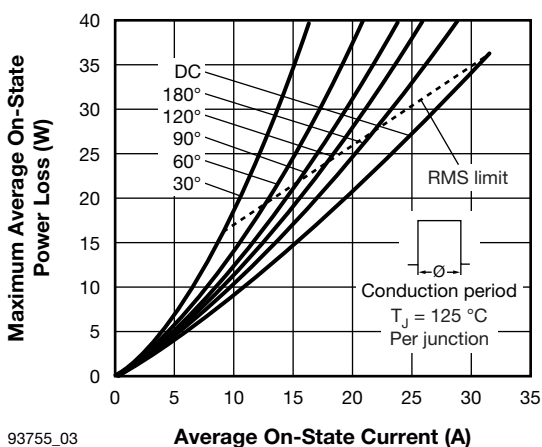
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Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)



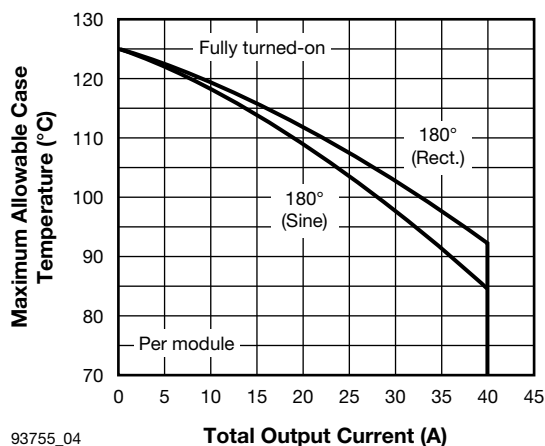
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Fig. 2 - On-State Power Loss Characteristics



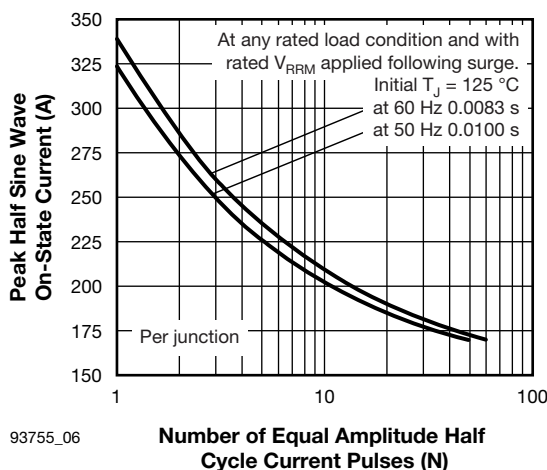
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Fig. 3 - On-State Power Loss Characteristics



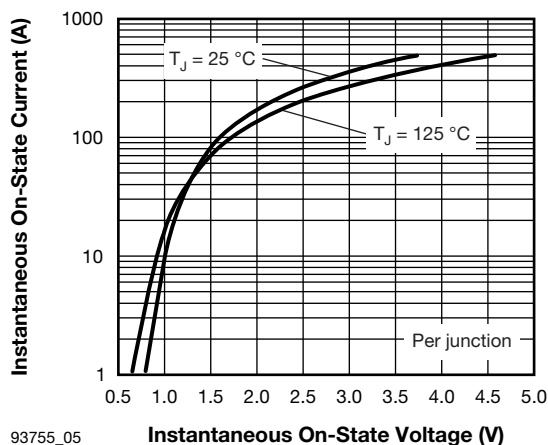
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Fig. 4 - Current Ratings Characteristics



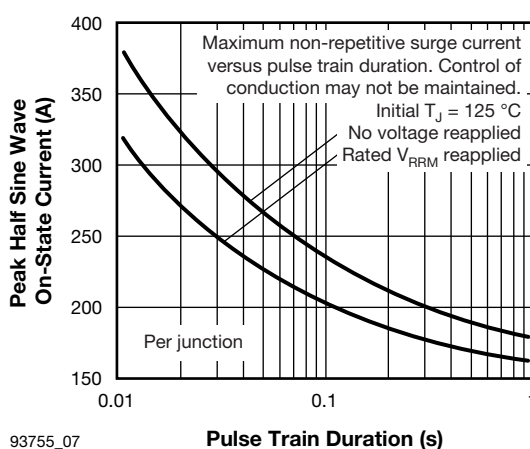
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Fig. 6 - Maximum Non-Repetitive Surge Current



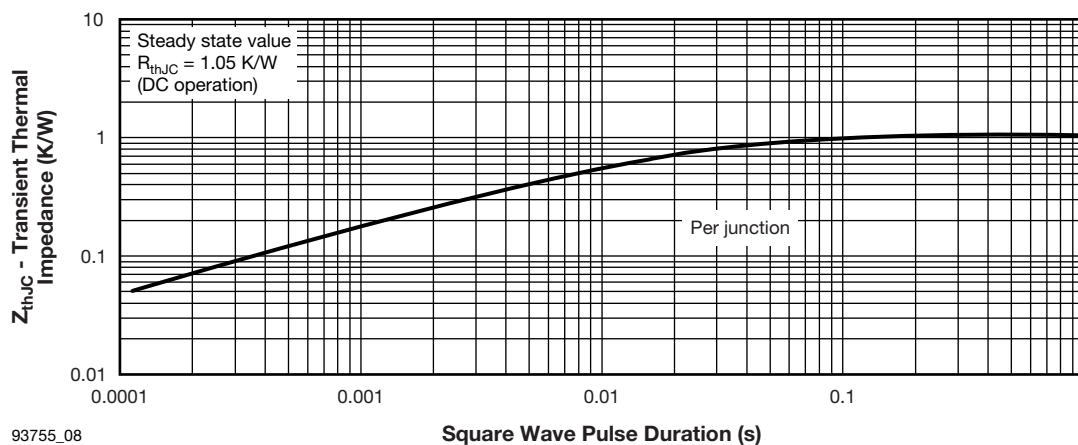
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Fig. 5 - On-State Voltage Drop Characteristics



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Fig. 7 - Maximum Non-Repetitive Surge Current



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Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

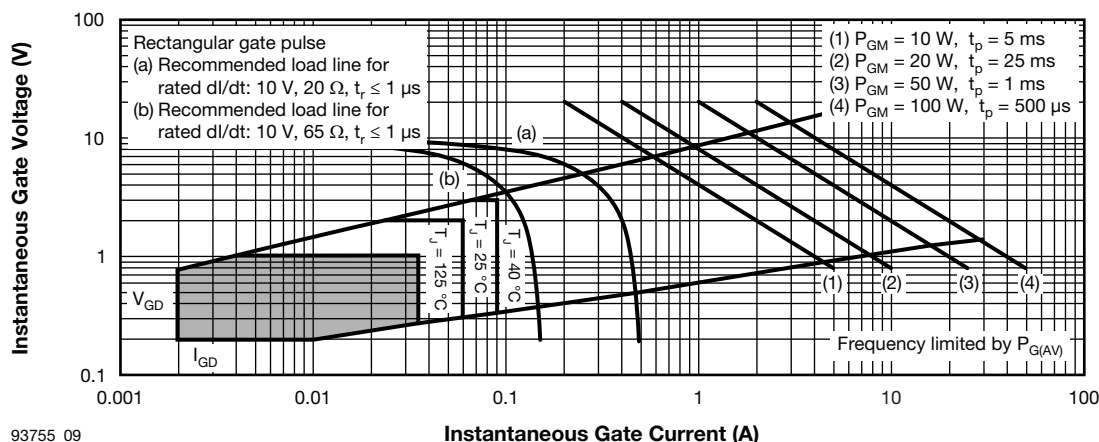
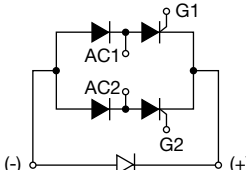
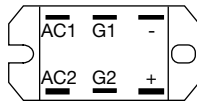
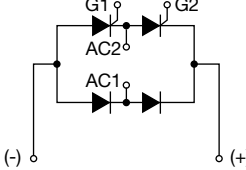

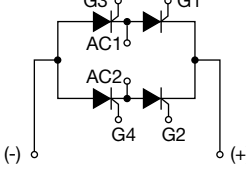



Fig. 9 - Gate Characteristics

## ORDERING INFORMATION TABLE

Device code	<b>VS-</b>	<b>P</b>	<b>4</b>	<b>0</b>	<b>2</b>	<b>K</b>	<b>W</b>
	(1)	(2)	(3)	(4)	(5)	(6)	(7)

- 1** - Vishay Semiconductors product
- 2** - Module type
- 3** - Current rating  
1 = 25 A DC (P100 series)  
4 = 40 A DC (P400 series)
- 4** - Circuit configuration  
0 = single phase, hybrid bridge common cathode  
2 = single phase, hybrid bridge doubler connection  
3 = single phase, all SCR bridge
- 5** - Voltage code  
1 = 400 V  
2 = 600 V  
3 = 800 V  
4 = 1000 V  
5 = 1200 V
- 6** - K = optional voltage suppression
- 7** - W = optional freewheeling diode

CIRCUIT CONFIGURATION			
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	SCHEMATIC DIAGRAM	TERMINAL POSITIONS
Single phase, hybrid bridge common cathode	0		
Single phase, hybrid bridge doubler connection	2		
Single phase, all SCR bridge	3		

CODING (1)					
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	BASIC SERIES	WITH VOLTAGE SUPPRESSION	WITH FREEWHEELING DIODE	WITH BOTH VOLTAGE SUPPRESSION AND FREEWHEELING DIODE
Single phase, hybrid bridge common cathode	0	P40.	P40.K	P40.W	P40.KW
Single phase, hybrid bridge doubler connection	2	P42.	P42.K	-	-
Single phase, all SCR bridge	3	P43.	P43.K	-	-

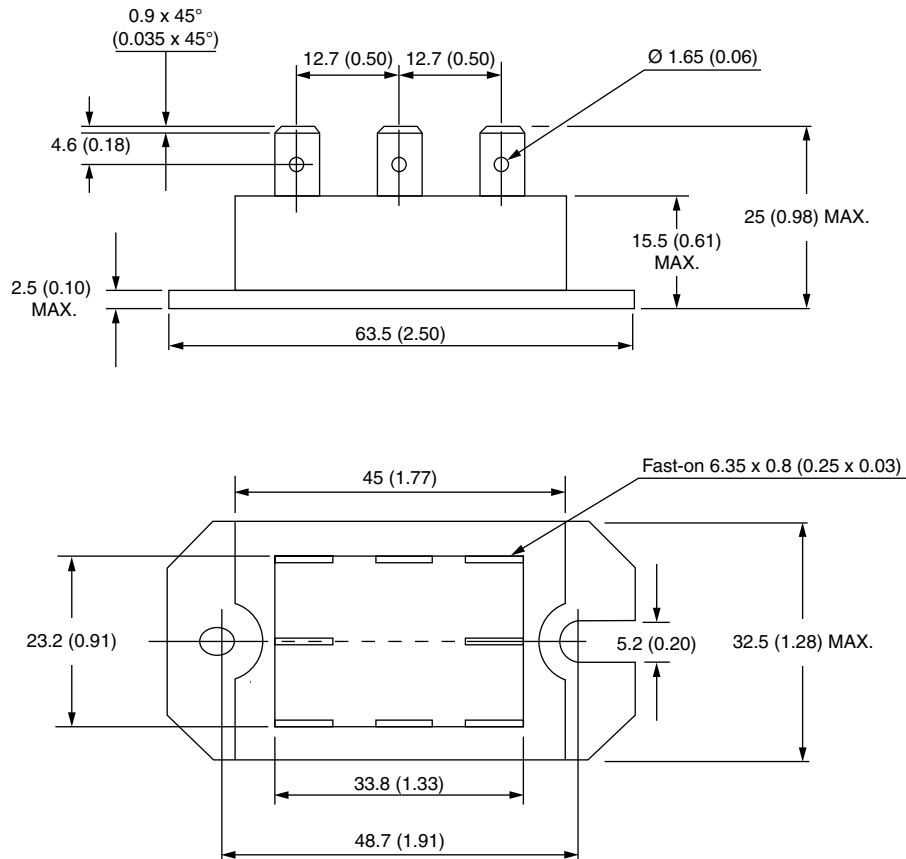
#### Note

(1) To complete code refer to Voltage Ratings table, i.e.: for 600 V P40.W complete code is P402W

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95335">www.vishay.com/doc?95335</a>

## D-19 PACE-PAK

**DIMENSIONS** in millimeters (inches)





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