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ISL9222A

High Input Voltage Charger

FN6704
Rev 0.00
July 28, 2008

The ISL9222A is a cost-effective, fully integrated high input voltage single-cell Li-ion battery charger. The charger uses a CC/CV charge profile required by Li-ion batteries. The charger accepts an input voltage up to 28V but is disabled when the input voltage exceeds the OVP threshold, typically 7.2V, to prevent excessive power dissipation. The 28V rating eliminates the overvoltage protection circuit required in a low input voltage charger.

The charge current is user programmable with an external resistor. When the battery voltage is lower than typically 2.55V, the charger preconditions the battery with typically 20% of the programmed charge current. An internal thermal foldback function protects the charger from any thermal failure.

AN indication pin $\overline{PPR}$ allows simple interface to a microprocessor or LED. When no adapter is attached or when disabled, the charger draws less than 1µA leakage current from the battery.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9222AIRTZ-T	22A	-40 to +85	8 Ld 2x3 TDFN Tape and Reel	L8.2x3A

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

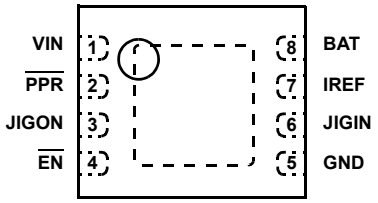
- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- Low Component Count and Cost
- 1% Voltage Accuracy
- Programmable Charge Current
- **Charge Current Thermal Foldback for Thermal Protection**
- Trickle Charge for Fully Discharged Batteries
- **28V Maximum Voltage for the Power Input**
- Power Presence Indication
- Less Than 1µA Leakage Current off the Battery When No Input Power Attached or Charger Disabled
- Ambient Temperature Range: -40°C to +85°C
- **8 Ld 2x3 TDFN Package**
- Auxiliary OR-gate For System Booting Logic
- Pb-Free (RoHS Compliant)

Applications

- Mobile Phones
- Blue-Tooth Devices
- PDAs
- MP3 Players
- Stand-Alone Chargers
- Other Handheld Devices

Pinout

ISL9222A
(8 LD TDFN)
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

VIN . . . . . -0.3V to 30V
JIGIN, IREF, BAT, JIGON, $\overline{EN}$, $\overline{PPR}$ . . . . . -0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Maximum Supply Voltage (VIN Pin) 28V
Operating Supply Voltage (VIN Pin) . . . . . 4.5V to 6.5V
Programmed Charge Current . . . . . 100mA to 900mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TDFN Package (Notes 1, 2)	59	4.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical values are tested at V_{IN} = 5V and the ambient temperature at +25°C. All maximum and minimum values are established under the recommended operating supply voltage range and ambient temperature range, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising POR Threshold	V_{POR}	VBAT = 3.0V, use $\overline{PPR}$ to indicate the comparator output.	3.5	3.9	4.4	V
Falling POR Threshold	V_{POR}		2.8	3.4	3.50	V
VIN-BAT OFFSET VOLTAGE						
Rising Edge	V_{OS}	Monitor output current to indicate the comparator output. (Note 3)	-	90	150	mV
Falling Edge	V_{OS}		10	50	-	mV
OVERVOLTAGE PROTECTION						
Overvoltage Protection Threshold	V_{OVP}	Use $\overline{PPR}$ to indicate the comparator output. (Note 4)	6.9	7.2	7.5	V
OVP Threshold Hysteresis			100	240	400	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	VIN floating	-	-	1.0	µA
VIN Pin Supply Current	I_{VIN}	Charger disabled	-	350	600	µA
VIN Pin Supply Current	I_{VIN}	Charger enabled	-	500	800	µA
VOLTAGE REGULATION						
Output Voltage	V_{CH}	4.3V < V_{IN} < 6.5V, charge current = 20mA	4.158	4.20	4.242	V
PMOS ON-Resistance	$r_{DS(ON)}$	V_{BAT} = 3.8V, charge current = 0.5A	-	0.6	-	Ω
CHARGE CURRENT (Note 5)						
IREF Pin Output Voltage	I_{IREF}	V_{BAT} = 3.8V	1.18	1.22	1.26	V
Constant Charge Current	I_{CHG}	R_{IREF} = 24.3kΩ, V_{BAT} = 2.8V - 4.0V	440	500	550	mA
Trickle Charge Current	I_{TRK}	R_{IREF} = 24.3kΩ, V_{BAT} = 2.4V	70	95	130	mA
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.45	2.55	2.65	V
Preconditioning Voltage Hysteresis	V_{MINHYS}		-	250	-	mV
INTERNAL TEMPERATURE MONITORING						
Charge Current Foldback Threshold	T_{FOLD}		-	115	-	°C

Electrical Specifications Typical values are tested at V_{IN} = 5V and the ambient temperature at +25°C. All maximum and minimum values are established under the recommended operating supply voltage range and ambient temperature range, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUT AND OUTPUTS						
$\overline{EN}$ Pin Logic Input High	VIH		1.3	-	-	V
$\overline{EN}$ Pin Logic Input Low	VIL		-	-	0.5	V
$\overline{EN}$ Pin Internal Pull-Down Resistance			100	200	400	kΩ
$\overline{PPR}$ Sink Current when LOW		Pin Voltage = 1V	10	20	-	mA
$\overline{PPR}$ Leakage Current When HIGH		V_{PPR} = 6.5V	-	-	1	µA
AUXILIARY OR GATE						
Supply Voltage	V_S		2.5	-	5.0	V
JIGON High Level Output Voltage	VOH	$I_{JIGON(SOURCE)}$ = -60µA, 2.5V < VBAT < 5.0V	VBAT - 0.1V	-	-	V
		$I_{JIGON(SOURCE)}$ = -1mA, 3.0V < VBAT < 5.0V	VBAT- 0.45V	-	-	V
JIGON Out Put Low Voltage	VOL	$I_{JIGON(SINK)}$ = 1mA	-	-	0.1	V
JIGIN Pin Logic Input High	VIH	VBAT = 2.5V	2.1	-	-	V
		3.0V < VBAT < 5.0V	0.75 x VBAT	-	-	V
JIGIN Pin Logic Input Low	VIL	VBAT = 2.5V	-	-	0.4	V
		3.0V < VBAT < 5.0V	-	-	0.25x VBAT	V
JIGIN Pin Internal Pull-Down Resistance			100	240	400	kΩ

NOTES:

3. The output is used to test the VOS threshold. The output current will toggle between 0 and the CC current when VOS crosses over the threshold.
4. For junction temperature below +100°C.
5. The charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.

Pin Descriptions

VIN - Power input. The absolute maximum input voltage is 28V. A 1µF or larger value X5R ceramic capacitor is recommended to be placed very close to the input pin for decoupling purpose. Additional capacitance may be required to provide a stable input voltage.

$\overline{PPR}$ - Open-drain power presence indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold and off otherwise. This pin is capable to sink 10mA (minimum) current to drive an LED. The maximum voltage rating for this pin is 7V. This pin is independent on the EN-pin input.

JIGON - Output pin of the auxiliary 2-input OR gate. One of the inputs is internal and is connected to the inverted PPR logic. The other input is from the JIGIN pin driven externally to provide system booting enable signal.

$\overline{EN}$ - Enable input. This is a logic input pin to disable or enable the charger. Drive to HIGH to disable the charger. When this pin is driven to LOW or left floating, the charger is enabled. This pin has an internal 200kΩ pull-down resistor.

GND - System ground.

JIGIN - One of the inputs of the 2-input auxiliary OR gate. There is a 240kΩ pull down resistor at this pin.

IREF - Charge-current program and monitoring pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by Equation 1:

$$I_{REF} = \frac{12089}{R_{IREF}} \quad (mA) \qquad \text{(EQ. 1)}$$

Where R_{IREF} is in kΩ. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, VIREF = 0V.

BAT - Charger output pin. Connect this pin to the battery. A 1µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes. When the EN pin is pulled to logic HIGH, the BAT output is disabled.

EPAD - Exposed pad. Connect as much copper as possible to this pad either on the component layer or other layers through thermal vias to enhance the thermal performance.

Typical Applications

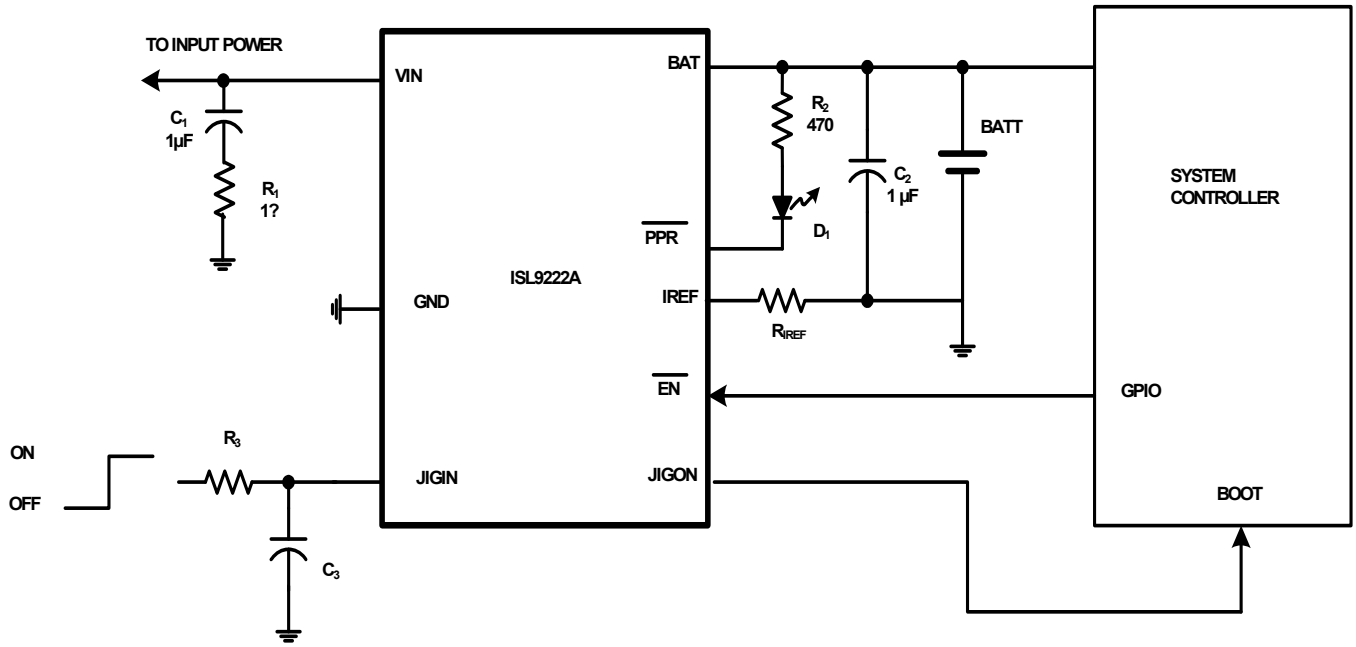


TABLE 1. JIGON STATES

POWER GOOD	JIGIN	VBAT VOLTAGE PRESENT, OR BATTERY ATTACHED	JIGON	PPR
No	L	No	L	Hi-Z
No	L	Yes	L	Hi-Z
No	H	No	L	Hi-Z
No	H	Yes	H	Hi-Z
Yes	L	X	H	Low
Yes	H	X	H	Low

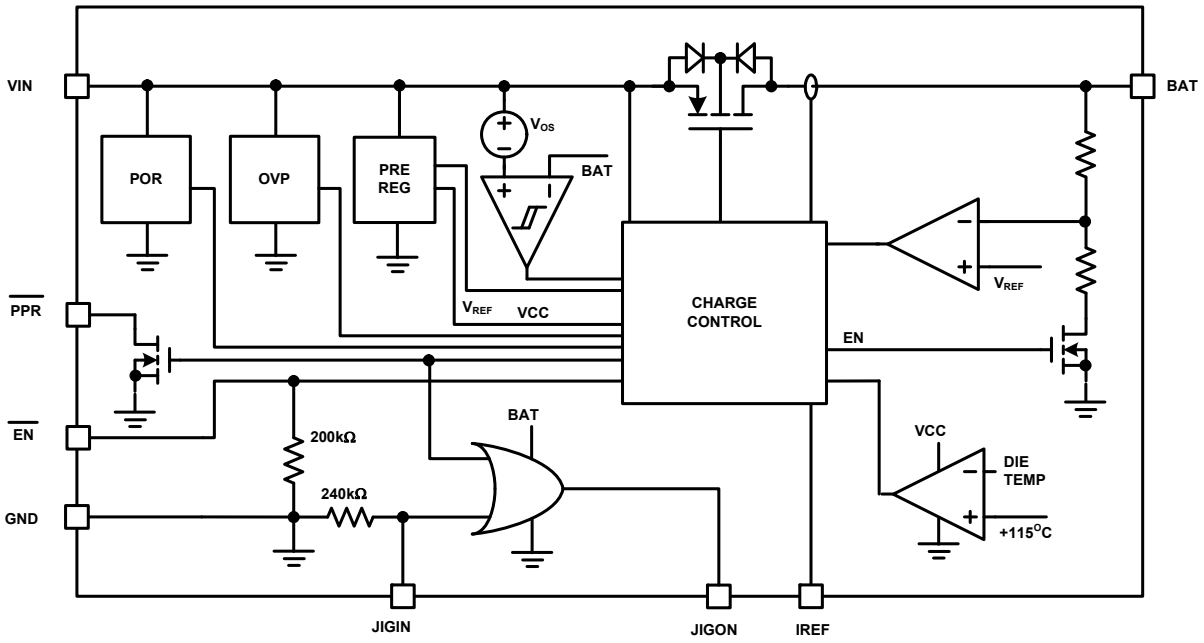


FIGURE 1. BLOCK DIAGRAM

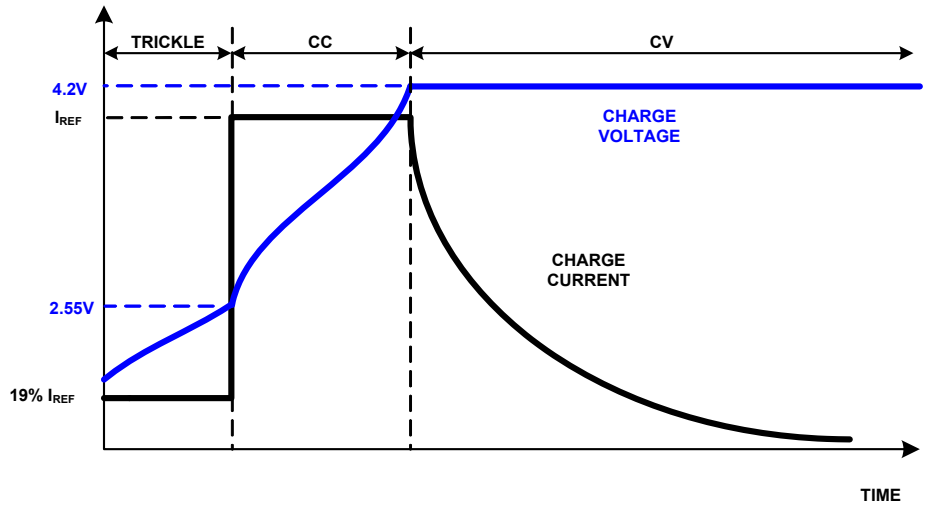


FIGURE 2. TYPICAL CHARGE PROFILE

Description

The ISL9222A charges a Li-ion battery using a CC/CV profile. The constant current I_{REF} is set with the external resistor R_{IREF} (See Typical Applications circuit on page 4) and the constant voltage is fixed at 4.2V. If the battery voltage is below a typical 2.55V trickle-charge threshold, the ISL9222A charges the battery with a trickle current of 19% of I_{REF} until the battery voltage rises above the trickle charge threshold. Fast charge CC mode is maintained at the rate determined by programming I_{REF} until the cell voltage rises to 4.2V. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates the battery voltage at 4.2V to fully charge the battery without the risk of over charge. The charger will continue to output the 4.2V voltage until the

input power is removed or the EN pin is pulled to HI. Figure 2 shows the typical charge waveforms after the power is on.

A thermal foldback function reduces the charge current anytime when the die temperature reaches typically +115°C. This function guarantees safe operation when the printed-circuit board (PCB) is not capable of dissipating the heat generated by the linear charger. The ISL9222A accepts an input voltage up to 28V but disables charging when the input voltage exceeds the OVP threshold, typically 7.2V, to protect against unqualified or faulty AC adapters.

$\overline{\text{PPR}}$ Indication

The $\overline{\text{PPR}}$ pin is an open-drain output to indicate the presence of the ac adapter. Whenever the input voltage is higher than the POR threshold, the $\overline{\text{PPR}}$ pin turns on the internal open-drain MOSFET to indicate a logic LOW signal, independent on the $\overline{\text{EN}}$ pin input. When the internal open-drain FET is turned off, the $\overline{\text{PPR}}$ pin should leak less than 1µA current. When turned on, the $\overline{\text{PPR}}$ pin should be able to sink at least 10mA current under all operating conditions.

The PPR pin can be used to drive an LED or to interface with a microprocessor.

Power-Good Range

The power-good range is defined by the following three conditions:

1. VIN > VPOR
2. VIN - VBAT > VOS
3. VIN < VOVP

where VOS is the offset voltage for the input and output voltage comparator, discussed shortly, and VOVP is the overvoltage protection threshold given in the Electrical Specifications table on page 2. All V_{POR}, V_{OS}, and V_{OVP} have hysteresis, as given in the Electrical Specification table on page 2. The charger will not charge the battery if the input voltage is not in the power-good range.

Input and Output Comparator

The charger will not be enabled unless the input voltage is higher than the battery voltage by an offset voltage VOS. The purpose of this comparator is to ensure that the charger is turned off when the input power is removed from the charger. Without this comparator, it is possible that the charger will fail to power-down when the input is removed and the current can leak through the PFET pass element to continue biasing the POR and the Pre-Regulator blocks shown in the Block Diagram on page 5.

$\overline{\text{EN}}$ Input

$\overline{\text{EN}}$ is an active-low logic input to enable the charger. Drive the $\overline{\text{EN}}$ pin to LOW or leave it floating to enable the charger. This pin has a 200kΩ internal pulldown resistor so when left floating, the input is equivalent to logic LOW. Drive this pin to HIGH to disable the charger. The threshold for HIGH is given in the Electrical Specifications table on page 2.

IREF Pin

The IREF pin has the two functions as described in “Pin Descriptions” on page 3. When setting the fast charge current, the charge current is guaranteed to have 10% accuracy with the charge current set at 500mA. When monitoring the charge current, the accuracy of the IREF pin voltage vs. the actual charge current is the same as the gain from the IREF pin current to the actual charge current. The accuracy is 10% at 500mA and is expected to drop to 30% of the actual current (not the set constant charge current) when the current drops to 50mA.

Operation Without the Battery

The ISL9222A relies on a battery for stability and is not guaranteed to be stable if the battery is not connected. With a battery, the charger will be stable with an output ceramic decoupling capacitor in the range of 1µF to 200µF. The maximum load current is limited by the dropout voltage or the thermal foldback.

Dropout Voltage

The constant current may not be maintained due to the $r_{DS(ON)}$ limit at a low input voltage. The worst case ON-resistance of the pass FET is 1.2Ω at the maximum operating temperature, thus if tested with 0.5A current and 3.8V battery voltage, constant current could not be maintained when the input voltage is below 4.4V.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of +115°C.

Auxiliary OR Gate

The auxiliary OR gate provides a booting enable signal from from 2 possible inputs, the VIN power good signal, which is internal to the IC, or the external JIGIN signal. The supply voltage of the OR gate comes from VBAT. The JIGON states are summarized in Table 1. There is an internal pull-down resistor at the JIGIN pin so that when left floating, the input is a logic low.

Applications Information

Input Capacitor Selection

The input capacitor is required to suppress the power supply transient response during transitions. Mainly, this capacitor is selected to avoid oscillation during the start up when the input supply is passing the POR threshold and the VIN-BAT comparator offset voltage. A 1µF or larger X5R ceramic capacitor is recommended.

Due to the inductance of the power leads of the wall adapter or USB source, the input capacitor type must be properly selected to prevent high voltage transient during a hot-plug

event. A tantalum capacitor is a good choice for its high ESR, providing damping to the voltage transient. Multi-layer ceramic capacitors, however, have a very low ESR and hence when chosen as input capacitors, a 1Ω series resistor must be used (as shown in “Typical Applications” on page 4) to provide adequate damping.

Output Capacitor Selection

The criteria for selecting the output capacitor is to maintain the stability of the charger as well as to bypass any transient load current. The minimum capacitance is a 1µF X5R ceramic capacitor. The actual capacitance connected to the output is dependent on the actual application requirement.

Charge Current Limit

The actual charge current in CC mode is limited by several factors in addition to the set I_{REF}. Figure 3 shows three limits for the charge current in CC mode. The charge current is limited by the ON-resistance of the pass element (power P-channel MOSFET) if the input and the output voltage are too close to each other. The solid curve shows a typical case when the battery voltage is 4.0V and the charge current is set to 700mA. The non-linearity on the R_{ON}-limited region is due to the increased resistance at higher die temperatures. If the battery voltage increases to higher than 4.0V, the entire curve moves towards the right side. As the input voltage increases, the charge current may be reduced due to the thermal foldback function. The limit caused by the thermal limit is dependent on the thermal impedance. As the thermal impedance increases, the thermal-limited curve moves towards left, as shown in Figure 3.

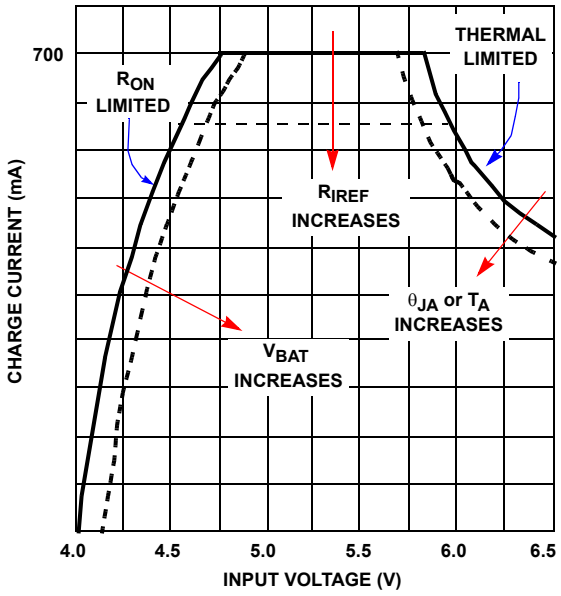


FIGURE 3. CHARGE CURRENT LIMITS IN THE CC MODE

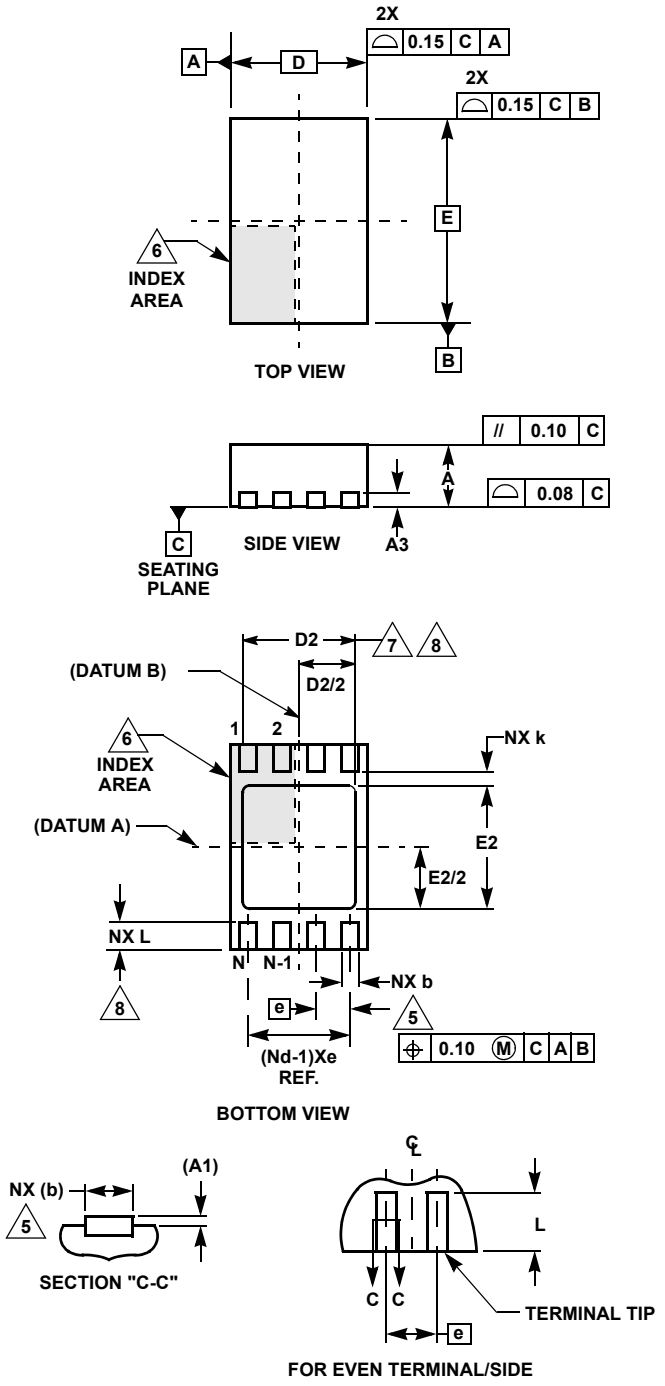
Layout Guidance

The ISL9222A uses a thermally-enhanced TDFN package that has an exposed thermal pad at the bottom side of the package. The layout should connect as much as possible to copper on the exposed pad. Typically, the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance from other thermal vias.

Input Power Sources

The input power source is typically a well-regulated wall cube with 1-meter length wire or a USB port. The input voltage ranges from 4.25V to 6.5V under full-load and unloaded conditions. The ISL9222A can withstand up to 28V on the input without damaging the IC. If the input voltage is higher than typically 7.2V, the charger stops charging.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.2x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.