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June 2014

FDMC86520L

N-Channel Power Trench[®] MOSFET 60 V, 22 A, 7.9 m Ω

Features

- Max $r_{DS(on)} = 7.9 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 13.5 \text{ A}$
- Max $r_{DS(on)}$ = 11.7 m Ω at V_{GS} = 4.5 V, I_D = 11.5 A
- Low Profile 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

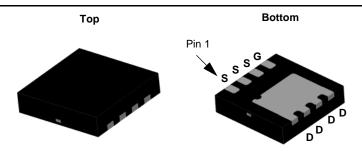


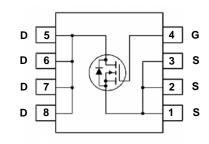
General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers.It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- Primary Switch in isolated DC-DC
- Synchronous Rectifier
- Load Switch





MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parame		Ratings	Units	
V_{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C		22	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	13.5	Α
	-Pulsed			60	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	79	mJ
Б	Power Dissipation	T _C = 25 °C		40	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	iture Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86520L	FDMC86520L	Power 33	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_DSS	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		29		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-7		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 13.5 \text{ A}$		6.5	7.9	
r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 11.5 \text{ A}$		9.1	11.7	mΩ	
		$V_{GS} = 10 \text{ V}, I_D = 13.5 \text{ A}, T_J = 125 ^{\circ}\text{C}$		9	11	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 13.5 A		49		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 20 V V 0 V	3420	4550	pF
Coss	Output Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	638	850	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112	25	40	pF
R _a	Gate Resistance		0.5		Ω

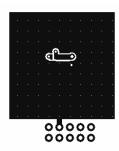
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		15	30	ns
t _r	Rise Time	$V_{DD} = 30 \text{ V}, I_{D} = 13.5 \text{ A},$	5.2	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	32	55	ns
t _f	Fall Time		3.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to 10 V	45	64	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $I_{DD} = 30 \text{ V},$ $I_{D} = 13.5 \text{ A}$	21	30	nC
Q_{gs}	Total Gate Charge	I _D = 13.5 A	9.6		nC
Q_{gd}	Gate to Drain "Miller" Charge		4.9		nC

Drain-Source Diode Characteristics

V _{SD} Source to Drain Diode Forward Voltage	Source to Drain Diode, Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 13.5 \text{ A}$ (Note 2)		0.82	1.3	\/
	$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$ (Note 2)		0.71	1.2	V	
t _{rr}	Reverse Recovery Time	I _F = 13.5 A, di/dt = 100 A/μs		38	62	ns
Q _{rr}	Reverse Recovery Charge			21	34	nC

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



53 °C/W when mounted on a 1 in² pad of 2 oz copper



125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0%.
- 3. Starting T $_J$ = 25 °C; N-ch: L = 0.3 mH, I $_{AS}$ = 23 A, V $_{DD}$ = 54 V, V $_{GS}$ = 10 V.

Typical Characteristics $T_J = 25$ °C unless otherwise noted

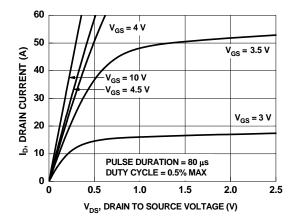


Figure 1. On Region Characteristics

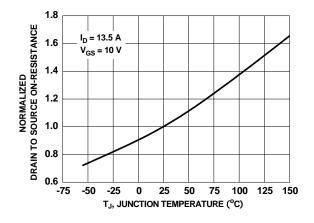


Figure 3. Normalized On Resistance vs. Junction Temperature

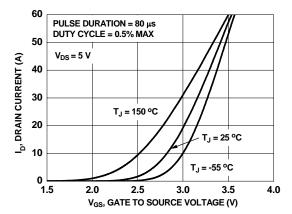


Figure 5. Transfer Characteristics

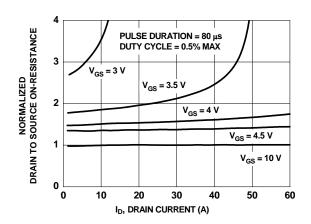


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

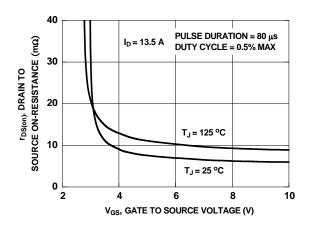


Figure 4. On-Resistance vs. Gate to Source Voltage

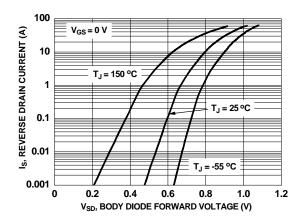


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

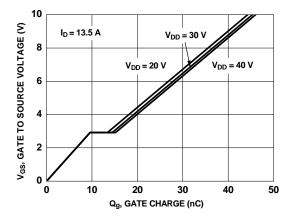


Figure 7. Gate Charge Characteristics

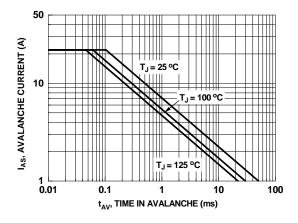


Figure 9. Unclamped Inductive Switching Capability

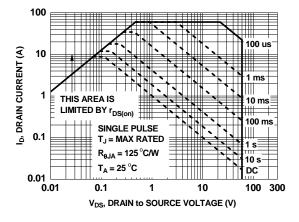


Figure 11. Forward Bias Safe Operating Area

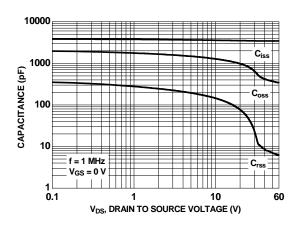


Figure 8. Capacitance vs. Drain to Source Voltage

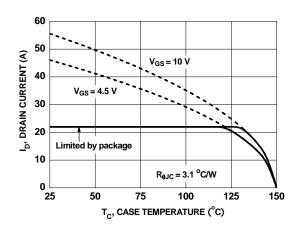


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

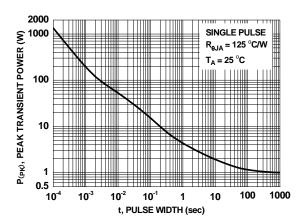


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

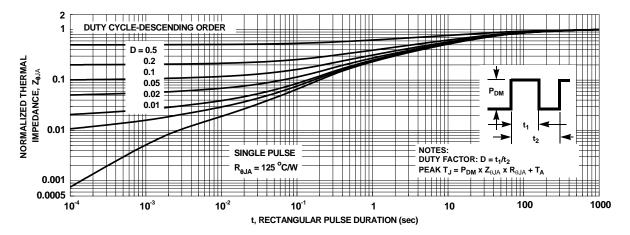
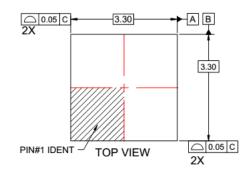
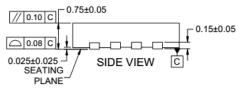
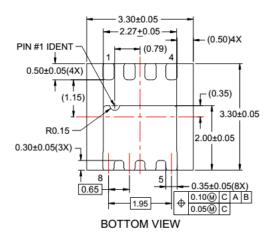


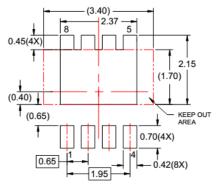
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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