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FAIRCHILD SEMICONDUCTOR®

September 2013

FDMC86102

N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 20 A, 24 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 24 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $r_{DS(on)}$ = 38 mΩ at V_{GS} = 6 V, I_D = 5 A
- Low Profile - 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

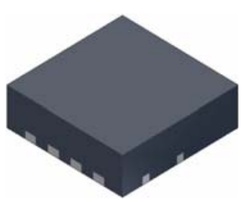
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

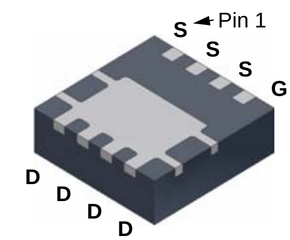
Application

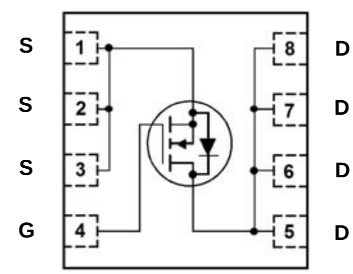
- DC - DC Conversion

Top



Bottom





Power 33

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous T_C = 25 °C	20	A
	-Continuous T_A = 25 °C (Note 1a)	7	
	-Pulsed (Note 4)	60	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	72	mJ
P_D	Power Dissipation T_C = 25 °C	41	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86102	FDMC86102	Power 33	13''	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		69		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A		19.4	24	mΩ
		V_{GS} = 6 V, I_D = 5 A		26.8	38	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125 °C		32.8	41	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 7 A		19		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		725	965	pF
C_{oss}	Output Capacitance			175	235	pF
C_{rss}	Reverse Transfer Capacitance			15	25	pF
R_g	Gate Resistance			0.5		Ω

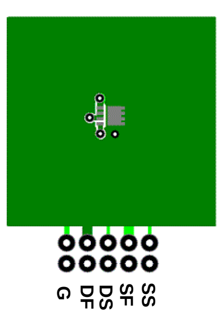
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	17	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
t_f	Fall Time			4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 7 A		13	18	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 50 V, I_D = 7 A		8	11	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 7 A		3.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.6		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)		0.81	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)		0.75	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs		44	70	ns
Q_{rr}	Reverse Recovery Charge			40	65	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Starting T_J = 25 ^oC; N-ch: L = 1 mH, I_{AS} = 12 A, V_{DD} = 90 V, V_{GS} = 10 V.
4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25 °C unless otherwise noted

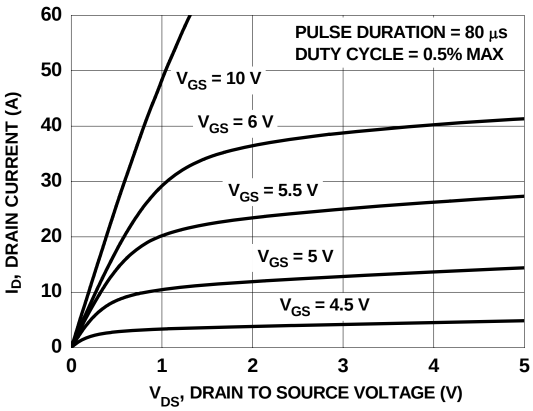


Figure 1. On-Region Characteristics

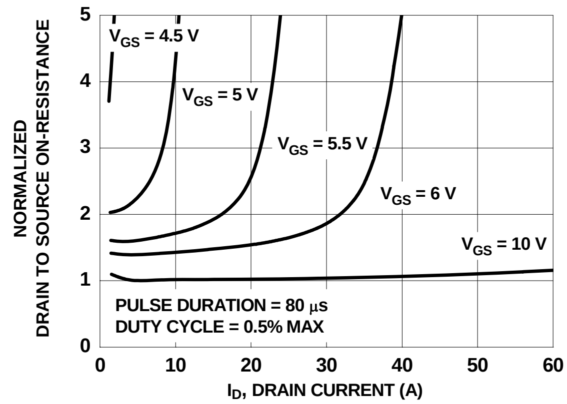


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

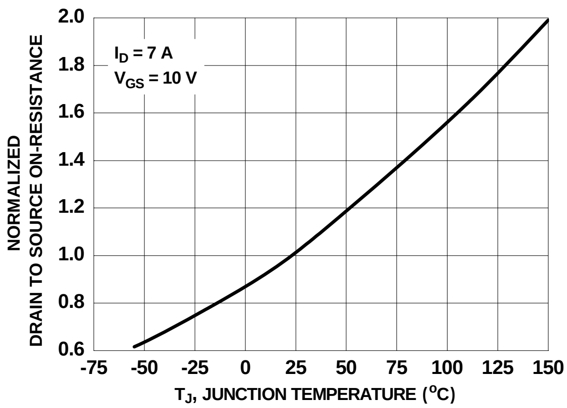


Figure 3. Normalized On-Resistance vs Junction Temperature

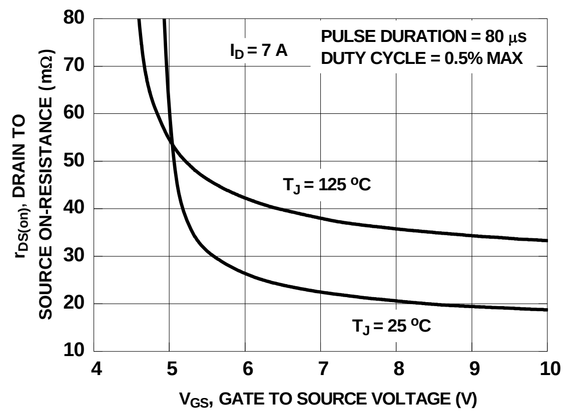


Figure 4. On-Resistance vs Gate to Source Voltage

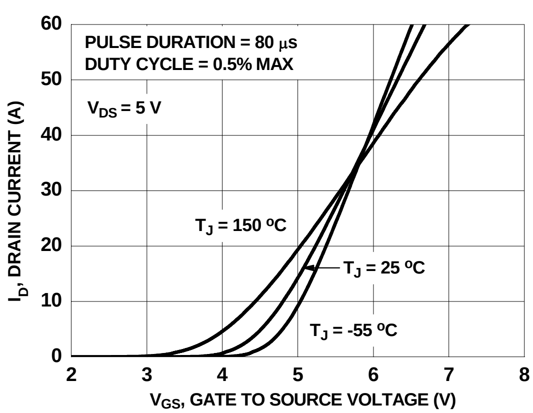


Figure 5. Transfer Characteristics

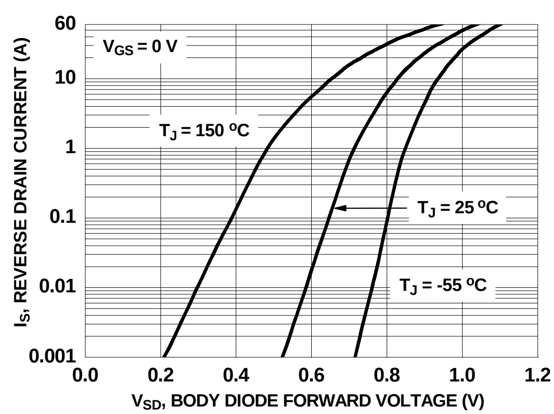


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

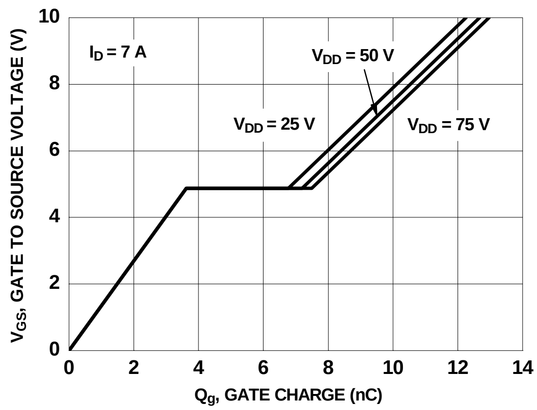


Figure 7. Gate Charge Characteristics

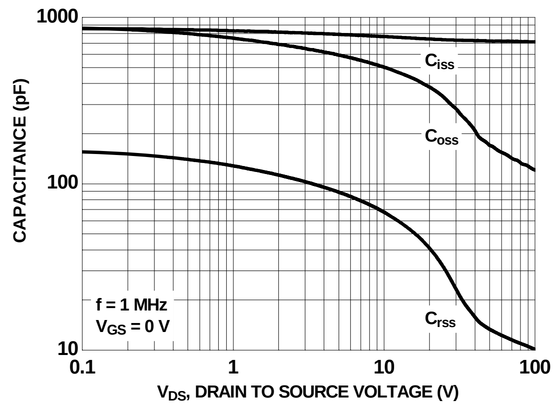


Figure 8. Capacitance vs Drain to Source Voltage

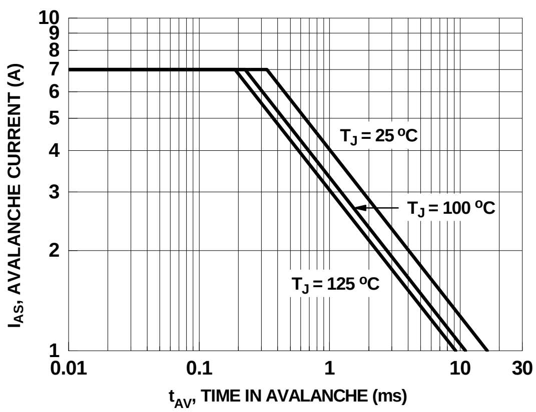


Figure 9. Unclamped Inductive Switching Capability

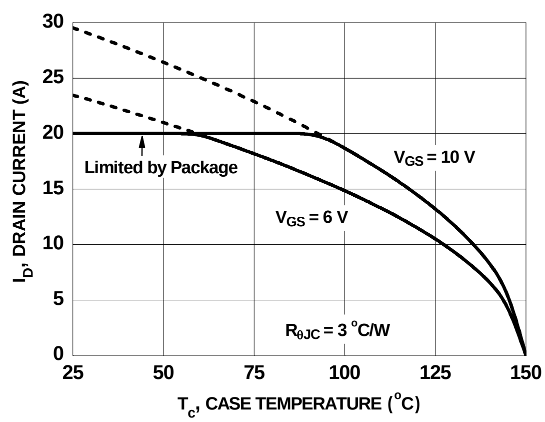


Figure 10. Maximum Continuous Drain Current vs Case Temperature

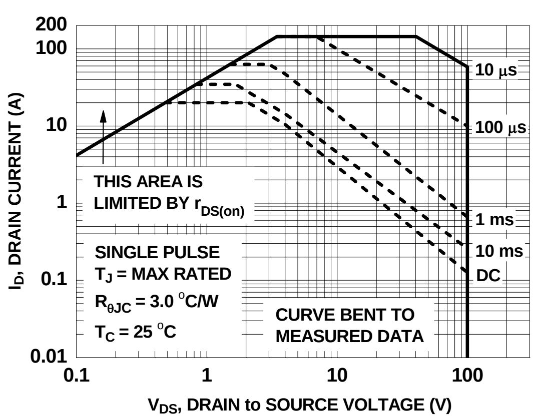


Figure 11. Forward Bias Safe Operating Area

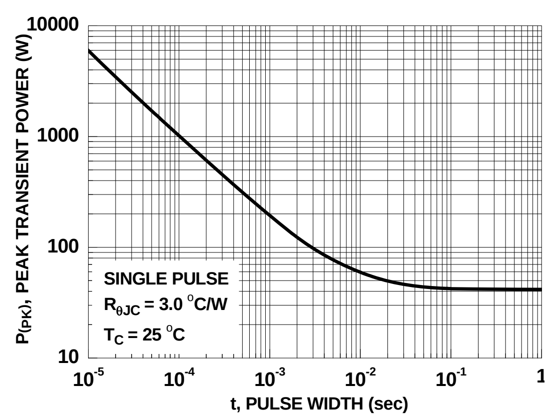


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

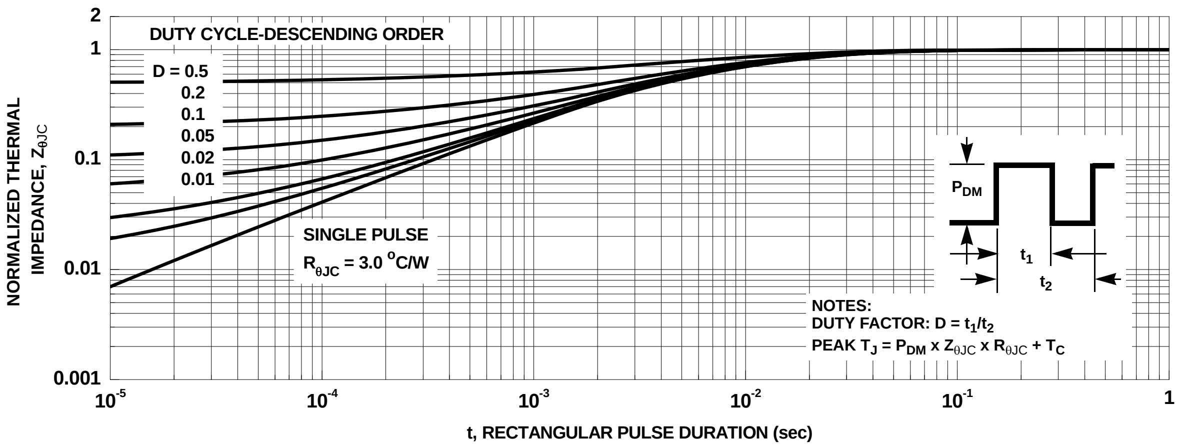
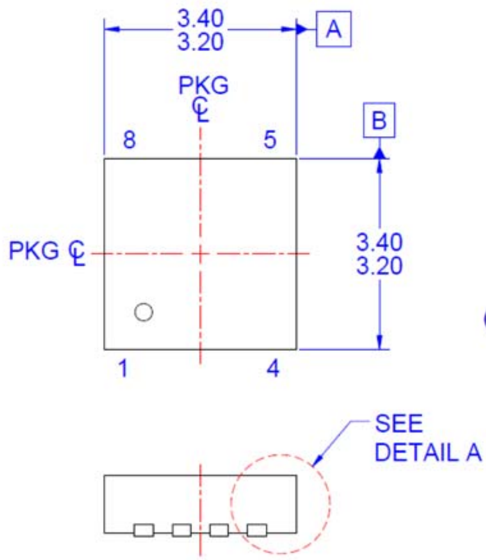
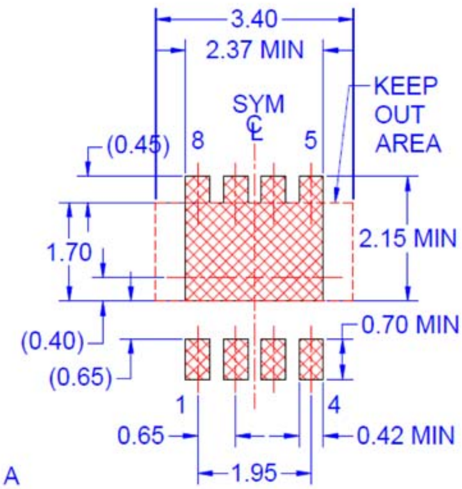


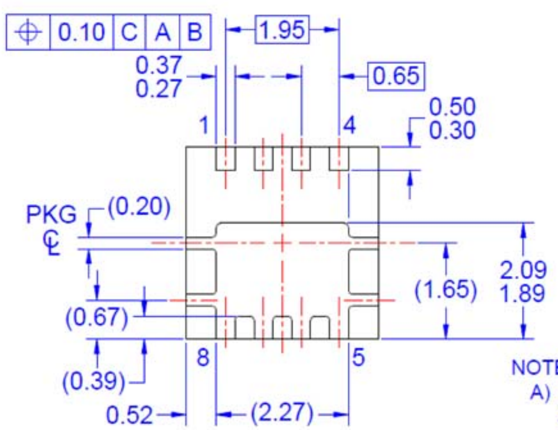
Figure 13. Transient Thermal Response Curve

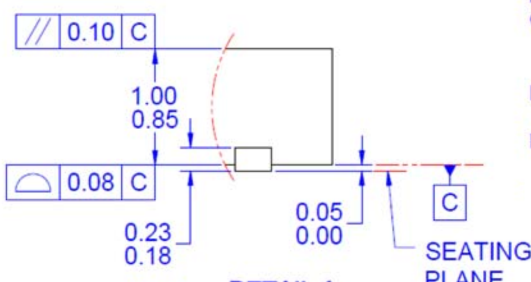
Dimensional Outline and Pad Layout





LAND PATTERN RECOMMENDATION





DETAIL A
SCALE: 2X

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I65

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