MCP453X/455X/463X/465X

7/8-Bit Single/Dual I²C Digital POT with Volatile Memory

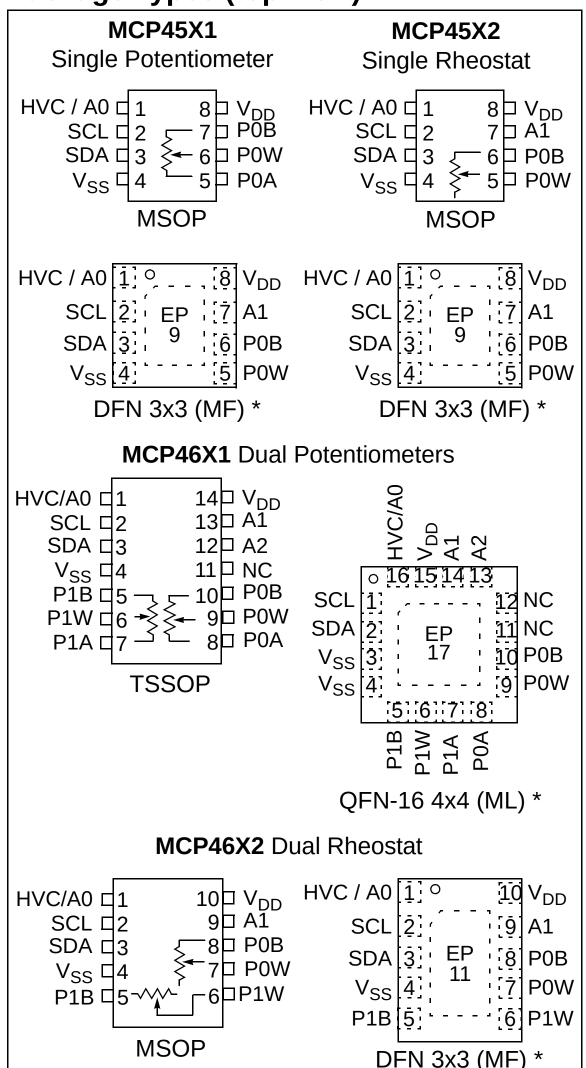
Features

- Single or Dual Resistor Network options
- Potentiometer or Rheostat configuration options
- Resistor Network Resolution
  - 7-bit: 128 Resistors (129 Steps)
  - 8-bit: 256 Resistors (257 Steps)
- R_{AB} Resistances options of:
  - 5 kΩ
  - 10 kΩ
  - 50 kΩ
  - 100 kΩ
- Zero-Scale to Full-Scale Wiper operation
- Low Wiper Resistance: 75Ω (typical)
- Low Tempco:
  - Absolute (Rheostat): 50 ppm typical (0°C to 70°C)
  - Ratiometric (Potentiometer): 15 ppm typical
- I²C Serial interface
  - 100 kHz, 400 kHz and 3.4 MHz support
- Serial protocol allows:
  - High-Speed Read/Write to wiper
  - Increment/Decrement of wiper
- Resistor Network Terminal Disconnect Feature via the Terminal Control (TCON) Register
- Brown-out reset protection (1.5V typical)
- Serial Interface Inactive current (2.5 uA typical)
- High-Voltage Tolerant Digital Inputs: Up to 12.5V
- Wide Operating Voltage:
  - 2.7V to 5.5V - Device Characteristics Specified
  - 1.8V to 5.5V - Device Operation
- Wide Bandwidth (-3dB) Operation:
  - 2 MHz (typical) for 5.0 kΩ device
- Extended temperature range (-40°C to +125°C)

Description

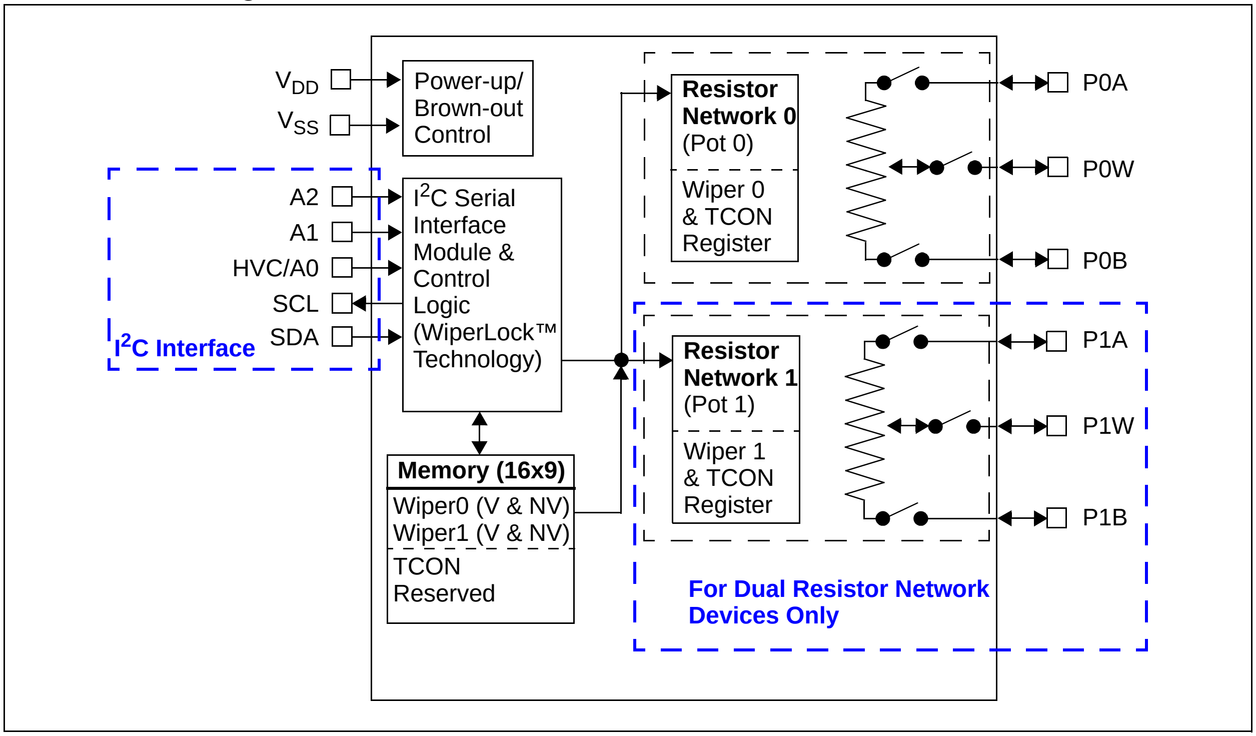
The MCP45XX and MCP46XX devices offer a wide range of product offerings using an I²C interface. This family of devices support 7-bit and 8-bit resistor networks, Volatile memory configurations, and Potentiometer and Rheostat pinouts.

Package Types (top view)



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Device Block Diagram



Device Features

Device	# of POTs	Wiper Configuration	Control Interface	Memory Type	WiperLock Technology	POR Wiper Setting	Resistance (typical) R_{AB} Options (kΩ)	Resistance (typical) Wiper - R_W (Ω)	# of Steps	V_{DD} Operating Range (2)
MCP4531 (3)	1	Potentiometer (1)	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4532 (3)	1	Rheostat	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4541	1	Potentiometer (1)	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4542	1	Rheostat	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4551 (3)	1	Potentiometer (1)	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4552 (3)	1	Rheostat	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4561	1	Potentiometer (1)	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4562	1	Rheostat	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4631 (3)	2	Potentiometer (1)	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4632 (3)	2	Rheostat	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	129	1.8V to 5.5V
MCP4641	2	Potentiometer (1)	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4642	2	Rheostat	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	129	2.7V to 5.5V
MCP4651 (3)	2	Potentiometer (1)	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4652 (3)	2	Rheostat	I^2C	RAM	No	Mid-Scale	5.0, 10.0, 50.0, 100.0	75	257	1.8V to 5.5V
MCP4661	2	Potentiometer (1)	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V
MCP4662	2	Rheostat	I^2C	EE	Yes	NV Wiper	5.0, 10.0, 50.0, 100.0	75	257	2.7V to 5.5V

Note 1: Floating either terminal (A or B) allows the device to be used as a Rheostat (variable resistor).
2: Analog characteristics only tested from 2.7V to 5.5V unless otherwise noted.
3: Please check Microchip web site for device release and availability

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD} with respect to V_{SS} .... -0.6V to +7.0V
Voltage on HVC/A0, A1, A2, SCL, and SDA with respect to V_{SS} .... -0.6V to 12.5V
Voltage on all other pins (PxA, PxW, and PxB) with respect to V_{SS} .... -0.3V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ ON HV pins) ....±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ....±20 mA
Maximum output current sunk by any Output pin ....25 mA
Maximum output current sourced by any Output pin ....25 mA
Maximum current out of V_{SS} pin ....100 mA
Maximum current into V_{DD} pin ....100 mA
Maximum current into PxA, PxW & PxB pins ....±2.5 mA
Storage temperature ....-65°C to +150°C
Ambient temperature with power applied -40°C to +125°C
Total power dissipation (**Note 1**) ....400 mW
Soldering temperature of leads (10 seconds).............+300°C
ESD protection on all pins ....≥ 4 kV (HBM), ... ≥ 300V (MM)
Maximum Junction Temperature (T_J) ....+150°C

Note 1: Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$$

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	Serial Interface only.
HVC pin Voltage Range	V_{HV}	V_{SS}	—	12.5V	V	V_{DD} ≥ 4.5V: The HVC pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}). (**Note 6**)
		V_{SS}	—	V_{DD} + 8.0V	V	V_{DD} < 4.5V
VDD Start Voltage to ensure Wiper Reset	V_{BOR}	—	—	1.65	V	RAM retention voltage (V_{RAM}) < V_{BOR}
VDD Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 9**)			V/ms	
Delay after device exits the reset state (V_{DD} > V_{BOR})	T_{BORD}	—	10	20	µs	
Supply Current **(Note 10)**	I_{DD}	—	—	600	µA	Serial Interface Active, HVC/A0 = V_{IH} (or V_{IL}) (**Note 11**) Write all 0's to Volatile Wiper 0 V_{DD} = 5.5V, F_{SCL} = 3.4 MHz
		—	—	250	µA	Serial Interface Active, HVC/A0 = V_{IH} (or V_{IL}) (**Note 11**) Write all 0's to Volatile Wiper 0 V_{DD} = 5.5V, F_{SCL} = 100 kHz
		—	2.5	5	µA	Serial Interface Inactive, (Stop condition, SCL = SDA = V_{IH}), Wiper = 0 V_{DD} = 5.5V, HVC/A0 = V_{IH}

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Resistance (± 20%)	R_{AB}	4.0	5	6.0	kΩ	-502 devices **(Note 1)**	
		8.0	10	12.0	kΩ	-103 devices **(Note 1)**	
		40.0	50	60.0	kΩ	-503 devices **(Note 1)**	
		80.0	100	120.0	kΩ	-104 devices **(Note 1)**	
Resolution	N	257			Taps	8-bit	No Missing Codes
		129			Taps	7-bit	No Missing Codes
Step Resistance	R_S	—	R_{AB} / (256)	—	Ω	8-bit	**Note 6**
		—	R_{AB} / (128)	—	Ω	7-bit	**Note 6**
Nominal Resistance Match	$\|R_{AB0} - R_{AB1}\| / R_{AB}$	—	0.2	1.25	%	**MCP46X1** devices only	
	$\|R_{BW0} - R_{BW1}\| / R_{BW}$	—	0.25	1.5	%	**MCP46X2** devices only, Code = Full-Scale	
Wiper Resistance (**Note 3, Note 4**)	R_W	—	75	160	Ω	V_{DD} = 5.5 V, I_W = 2.0 mA, code = 00h	
		—	75	300	Ω	V_{DD} = 2.7 V, I_W = 2.0 mA, code = 00h	
Nominal Resistance Tempco	$\Delta R_{AB}/\Delta T$	—	50	—	ppm/°C	T_A = -20°C to +70°C	
		—	100	—	ppm/°C	T_A = -40°C to +85°C	
		—	150	—	ppm/°C	T_A = -40°C to +125°C	
Ratiometeric Tempco	$\Delta V_{WB}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (80h or 40h)	
Resistor Terminal Input Voltage Range (Terminals A, B and W)	V_A, V_W, V_B	Vss	—	V_{DD}	V	**Note 5, Note 6**	

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

AC/DC CHARACTERISTICS (CONTINUED)

<table>
<tr><td colspan="2">DC Characteristics</td><td colspan="6">Standard Operating Conditions (unless otherwise specified)
Operating Temperature –40°C ≤ T_A ≤ +125°C (extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.</td></tr>
<tr><th>Parameters</th><th>Sym</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th><th colspan="2">Conditions</th></tr>
<tr><td rowspan="7">Maximum current through Terminal (A, W or B)
Note 6</td><td rowspan="7">I_T</td><td>—</td><td>—</td><td>2.5</td><td>mA</td><td>Terminal A</td><td>I_{AW},
W = Full-Scale (FS)</td></tr>
<tr><td>—</td><td>—</td><td>2.5</td><td>mA</td><td>Terminal B</td><td>I_{BW},
W = Zero Scale (ZS)</td></tr>
<tr><td>—</td><td>—</td><td>2.5</td><td>mA</td><td>Terminal W</td><td>I_{AW} or I_{BW},
W = FS or ZS</td></tr>
<tr><td>—</td><td>—</td><td>1.38</td><td>mA</td><td rowspan="4">Terminal A and Terminal B</td><td>I_{AB}, V_B = 0V,
V_A = 5.5V,
$R_{AB(MIN)}$ = 4000</td></tr>
<tr><td>—</td><td>—</td><td>0.688</td><td>mA</td><td>I_{AB}, V_B = 0V,
V_A = 5.5V,
$R_{AB(MIN)}$ = 8000</td></tr>
<tr><td>—</td><td>—</td><td>0.138</td><td>mA</td><td>I_{AB}, V_B = 0V,
V_A = 5.5V,
$R_{AB(MIN)}$ = 40000</td></tr>
<tr><td>—</td><td>—</td><td>0.069</td><td>mA</td><td>I_{AB}, V_B = 0V,
V_A = 5.5V,
$R_{AB(MIN)}$ = 80000</td></tr>
<tr><td rowspan="3">Leakage current into A, W or B</td><td rowspan="3">I_{WL}</td><td>—</td><td>100</td><td>—</td><td>nA</td><td colspan="2">MCP4XX1 PxA = PxW = PxB = V_{SS}</td></tr>
<tr><td>—</td><td>100</td><td>—</td><td>nA</td><td colspan="2">MCP4XX2 PxB = PxW = V_{SS}</td></tr>
<tr><td>—</td><td>100</td><td>—</td><td>nA</td><td colspan="2">Terminals Disconnected
(R1HW = R0HW = 0)</td></tr>
</table>

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Full-Scale Error (**MCP4XX1** only) (8-bit code = 100h, 7-bit code = 80h)	V_{WFSE}	-6.0	-0.1	—	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-4.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-3.5	-0.1	—	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-2.0	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.8	-0.1	—	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		-0.5	-0.1	—	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Zero-Scale Error (**MCP4XX1** only) (8-bit code = 00h, 7-bit code = 00h)	V_{WZSE}	—	+0.1	+6.0	LSb	5 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+3.5	LSb	10 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+2.0	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.8	LSb	50 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb	100 kΩ	8-bit	3.0V ≤ V_{DD} ≤ 5.5V
		—	+0.1	+0.5	LSb		7-bit	3.0V ≤ V_{DD} ≤ 5.5V
Potentiometer Integral Non-linearity	INL	-1	±0.5	+1	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP4XX1** devices only **(Note 2)**	
		-0.5	±0.25	+0.5	LSb	7-bit		
Potentiometer Differential Non-linearity	DNL	-0.5	±0.25	+0.5	LSb	8-bit	3.0V ≤ V_{DD} ≤ 5.5V **MCP4XX1** devices only **(Note 2)**	
		-0.25	±0.125	+0.25	LSb	7-bit		

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Bandwidth -3 dB (See Figure 2-65, load = 30 pF)	BW	—	2	—	MHz	5 kΩ	8-bit	Code = 80h
		—	2	—	MHz		7-bit	Code = 40h
		—	1	—	MHz	10 kΩ	8-bit	Code = 80h
		—	1	—	MHz		7-bit	Code = 40h
		—	200	—	kHz	50 kΩ	8-bit	Code = 80h
		—	200	—	kHz		7-bit	Code = 40h
		—	100	—	kHz	100 kΩ	8-bit	Code = 80h
		—	100	—	kHz		7-bit	Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP4XX1** only.
4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.
8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network
11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Rheostat Integral Non-linearity **MCP45X1** (**Note 4, Note 8**) **MCP4XX2** devices only **(Note 4)**	R-INL	-1.5	±0.5	+1.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-8.25	+4.5	+8.25	LSb			3.0V, I_W = 480 µA (**Note 7**)
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 900 µA
		-6.0	+4.5	+6.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		-1.5	±0.5	+1.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-5.5	+2.5	+5.5	LSb			3.0V, I_W = 240 µA (**Note 7**)
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 450 µA
		-4.0	+2.5	+4.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		-1.5	±0.5	+1.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-2.0	+1	+2.0	LSb			3.0V, I_W = 48 µA (**Note 7**)
		-1.125	±0.5	+1.125	LSb		7-bit	5.5V, I_W = 90 µA
		-1.5	+1	+1.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		-1.0	±0.5	+1.0	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-1.5	+0.25	+1.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		-0.8	±0.5	+0.8	LSb		7-bit	5.5V, I_W = 45 µA
		-1.125	+0.25	+1.125	LSb			3.0V, I_W = 24 µA (**Note 7**)

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B’s polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions		
Rheostat Differential Non-linearity **MCP45X1** (**Note 4, Note 8**) **MCP4XX2** devices only **(Note 4)**	R-DNL	-0.5	±0.25	+0.5	LSb	5 kΩ	8-bit	5.5V, I_W = 900 µA
		-1.0	+0.5	+1.0	LSb			3.0V, I_W = 480 µA (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 900 µA
		-0.75	+0.5	+0.75	LSb			3.0V, I_W = 480 µA (**Note 7**)
		-0.5	±0.25	+0.5	LSb	10 kΩ	8-bit	5.5V, I_W = 450 µA
		-1.0	+0.25	+1.0	LSb			3.0V, I_W = 240 µA (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 450 µA
		-0.75	+0.5	+0.75	LSb			3.0V, I_W = 240 µA (**Note 7**)
		-0.5	±0.25	+0.5	LSb	50 kΩ	8-bit	5.5V, I_W = 90 µA
		-0.5	±0.25	+0.5	LSb			3.0V, I_W = 48 µA (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 90 µA
		-0.375	±0.25	+0.375	LSb			3.0V, I_W = 48 µA (**Note 7**)
		-0.5	±0.25	+0.5	LSb	100 kΩ	8-bit	5.5V, I_W = 45 µA
		-0.5	±0.25	+0.5	LSb			3.0V, I_W = 24 µA (**Note 7**)
		-0.375	±0.25	+0.375	LSb		7-bit	5.5V, I_W = 45 µA
		-0.375	±0.25	+0.375	LSb			3.0V, I_W = 24 µA (**Note 7**)
Capacitance (P_A)	C_{AW}	—	75	—	pF	f =1 MHz, Code = Full-Scale		
Capacitance (P_w)	C_W	—	120	—	pF	f =1 MHz, Code = Full-Scale		
Capacitance (P_B)	C_{BW}	—	75	—	pF	f =1 MHz, Code = Full-Scale		

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

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AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $-40°C \le T_A \le +125°C$ (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**		
Digital Inputs/Outputs (SDA, SCK, HVC/A0, A1, A2, $\overline{WP}$)								
Schmitt Trigger High Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	All Inputs except SDA and SCL	$2.7V \le V_{DD} \le 5.5V$ (Allows 2.7V Digital V_{DD} with 5V Analog V_{DD})	
		0.5 V_{DD}	—	—	V		$1.8V \le V_{DD} \le 2.7V$	
		0.7 V_{DD}	—	V_{MAX}	V	SDA and SCL	100 kHz	
		0.7 V_{DD}	—	V_{MAX}	V		400 kHz	
		0.7 V_{DD}	—	V_{MAX}	V		1.7 MHz	
		0.7 V_{DD}	—	V_{MAX}	V		3.4 Mhz	
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	$0.2V_{DD}$	V	All inputs except SDA and SCL		
		-0.5	—	$0.3V_{DD}$	V	SDA and SCL	100 kHz	
		-0.5	—	$0.3V_{DD}$	V		400 kHz	
		-0.5	—	$0.3V_{DD}$	V		1.7 MHz	
		-0.5	—	$0.3V_{DD}$	V		3.4 Mhz	
Hysteresis of Schmitt Trigger Inputs **(Note 6)**	V_{HYS}	—	$0.1V_{DD}$	—	V	All inputs except SDA and SCL		
		N.A.	—	—	V	SDA and SCL	100 kHz	$V_{DD} < 2.0V$
		N.A.	—	—	V			$V_{DD} \ge 2.0V$
		0.1 V_{DD}	—	—	V		400 kHz	$V_{DD} < 2.0V$
		0.05 V_{DD}	—	—	V			$V_{DD} \ge 2.0V$
		0.1 V_{DD}	—	—	V		1.7 MHz	
		0.1 V_{DD}	—	—	V		3.4 Mhz	
High Voltage Limit	V_{MAX}	—	—	12.5 **(6)**	V	Pin can tolerate V_{MAX} or less.		

Note 1: Resistance is defined as the resistance between terminal A to terminal B.
2: INL and DNL are measured at V_W with $V_A = V_{DD}$ and $V_B = V_{SS}$.
3: **MCP4XX1** only.
4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.
5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.
6: This specification by design.
7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.
8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.
9: POR/BOR is not rate dependent.
10: Supply current is independent of current through the resistor network
11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

AC/DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ devices. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Low Voltage (SDA)	V_{OL}	V_{SS}	—	$0.2V_{DD}$	V	V_{DD} < 2.0V, I_{OL} = 1 mA
		V_{SS}	—	0.4	V	V_{DD} ≥ 2.0V, I_{OL} = 3 mA
Weak Pull-up / Pull-down Current	I_{PU}	—	—	1.75	mA	Internal V_{DD} pull-up, V_{IHH} pull-down V_{DD} = 5.5V, V_{IHH} = 12.5V
		—	170	—	µA	HVC pin, V_{DD} = 5.5V, V_{HVC} = 3V
HVC Pull-up / Pull-down Resistance	R_{HVC}	—	16	—	kΩ	V_{DD} = 5.5V, V_{HVC} = 3V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 3.4 MHz
RAM (Wiper) Value						
Value Range	N	0h	—	1FFh	hex	8-bit device
		0h	—	1FFh	hex	7-bit device
TCON POR/BOR Value	N_{TCON}	1FFh			hex	All Terminals connected
Power Requirements						
Power Supply Sensitivity (**MCP45X2** and **MCP46X2** only)	PSS	—	0.0015	0.0035	%/%	8-bit: V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 80h
		—	0.0015	0.0035	%/%	7-bit: V_{DD} = 2.7V to 5.5V, V_A = 2.7V, Code = 40h

Note 1: Resistance is defined as the resistance between terminal A to terminal B.

2: INL and DNL are measured at V_W with V_A = V_{DD} and V_B = V_{SS}.

3: **MCP4XX1** only.

4: **MCP4XX2** only, includes V_{WZSE} and V_{WFSE}.

5: Resistor terminals A, W and B's polarity with respect to each other is not restricted.

6: This specification by design.

7: Non-linearity is affected by wiper resistance (R_W), which changes significantly overvoltage and temperature.

8: The **MCP4XX1** is externally connected to match the configurations of the **MCP45X2** and **MCP46X2**, and then tested.

9: POR/BOR is not rate dependent.

10: Supply current is independent of current through the resistor network

11: When HVC/A0 = V_{IHH}, the I_{DD} current is less due to current into the HVC/A0 pin. See I_{PU} specification

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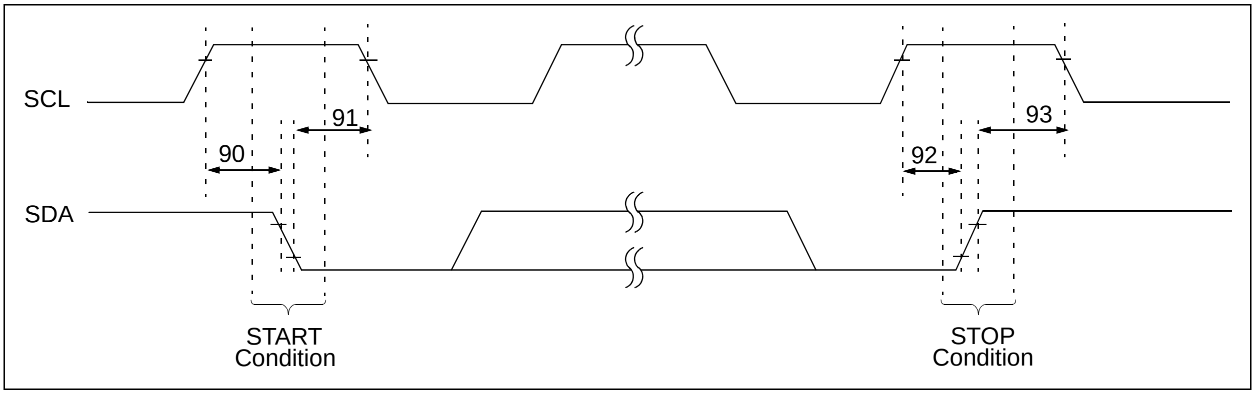

FIGURE 1-1: I^2C Bus Start/Stop Bits Timing Waveforms.

TABLE 1-1: I^2C BUS START/STOP BITS REQUIREMENTS

I^2C AC Characteristics			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage VDD range is described in **AC/DC characteristics**				
Param. No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	Cb	Bus capacitive loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	ns	Only relevant for repeated START condition
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	ns	After this period the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	TSU:STO	STOP condition Setup time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	

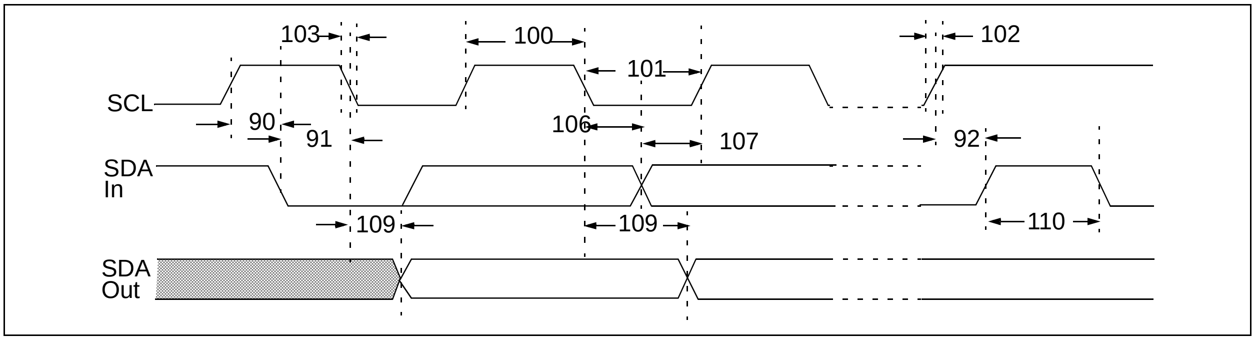

FIGURE 1-2: I^2C Bus Data Timing.

TABLE 1-2: I^2C BUS DATA REQUIREMENTS (SLAVE MODE)

I^2C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **AC/DC characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
100	THIGH	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120		ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	TLOW	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320		ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

3: The MCP46X1/MCP46X2 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use Cb in pF for the calculations.

5: Not Tested

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

7: Ensured by the T_{AA} 3.4 MHz specification test.

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TABLE 1-2: I^2C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I^2C AC Characteristics				Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in **AC/DC characteristics**			
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
102A (5)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B (5)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
103A (5)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B (5)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF (100 pF max for 3.4 MHz mode)
			400 kHz mode	20 + 0.1Cb (4)	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V, **Note 6**
			400 kHz mode	0	—	ns	2.7V-5.5V, **Note 6**
			1.7 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**
			3.4 MHz mode	0	—	ns	4.5V-5.5V, **Note 6**

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

3: The MCP46X1/MCP46X2 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I^2C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use Cb in pF for the calculations.

5: Not Tested

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

7: Ensured by the T_{AA} 3.4 MHz specification test.

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TABLE 1-2: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

I²C AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage V_{DD} range is described in AC/DC characteristics				
Param. No.	**Sym**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**Note 2**
			400 kHz mode	100	—	ns	
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	**Note 1**
			400 kHz mode	—	900	ns	
			1.7 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**, **Note 7**
				—	310	ns	Cb = 400 pF, **Note 1**, **Note 5**
			3.4 MHz mode	—	150	ns	Cb = 100 pF, **Note 1**
110	TBUF	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	Philips Spec states N.A.
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line
T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

3: The MCP46X1/MCP46X2 device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. This specification is not a part of the I²C specification, but must be tested in order to ensure that the output data will meet the setup and hold specifications for the receiving device.

4: Use Cb in pF for the calculations.

5: Not Tested

6: A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

7: Ensured by the T_{AA} 3.4 MHz specification test.

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TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-DFN (3x3)	θ_{JA}	—	60	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	145.5	—	°C/W	
Thermal Resistance, 10L-DFN (3x3)	θ_{JA}	—	57	—	°C/W	
Thermal Resistance, 10L-MSOP	θ_{JA}	—	202	—	°C/W	
Thermal Resistance, 14L-MSOP	θ_{JA}	—	N/A	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 16L-QFN	θ_{JA}	—	47	—	°C/W	

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

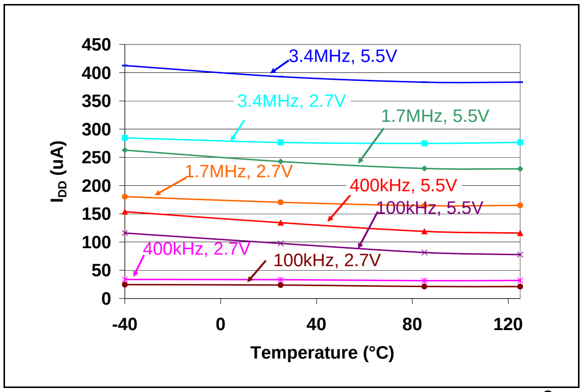

FIGURE 2-1: *Device Current (I_{DD}) vs. I^2C Frequency (f_{SCL}) and Ambient Temperature (V_{DD} = 2.7V and 5.5V).*

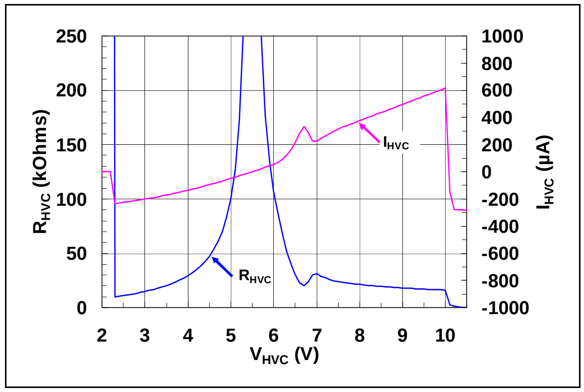

FIGURE 2-4: *HVC Pull-up/Pull-down Resistance (R_{HVC}) and Current (I_{HVC}) vs. HVC Input Voltage (V_{HVC}) (V_{DD} = 5.5V).*

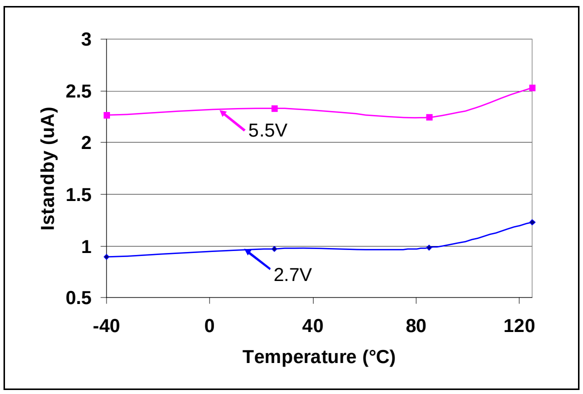

FIGURE 2-2: *Device Current (I_{SHDN}) and V_{DD}. (HVC = V_{DD}) vs. Ambient Temperature.*

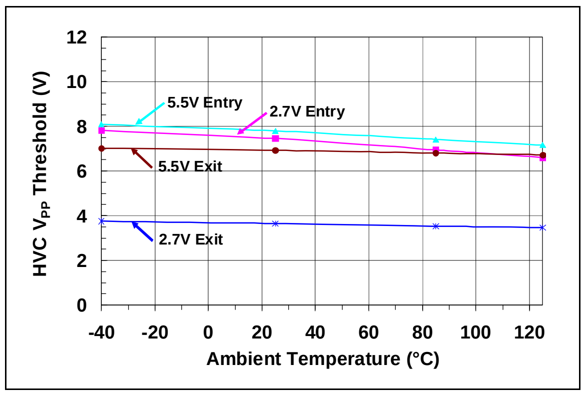

FIGURE 2-5: *HVC High Input Entry/Exit Threshold vs. Ambient Temperature and V_{DD}.*

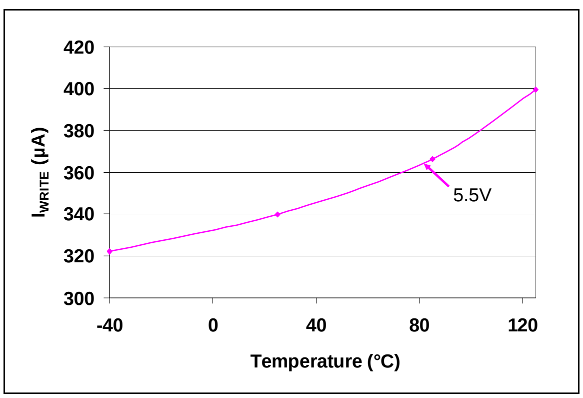

FIGURE 2-3: *Write Current (I_{WRITE}) vs. Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

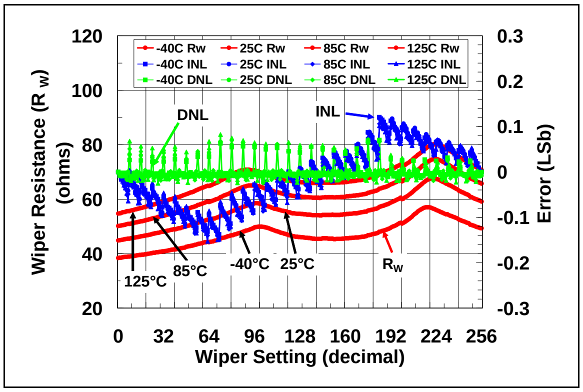


FIGURE 2-6: 5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

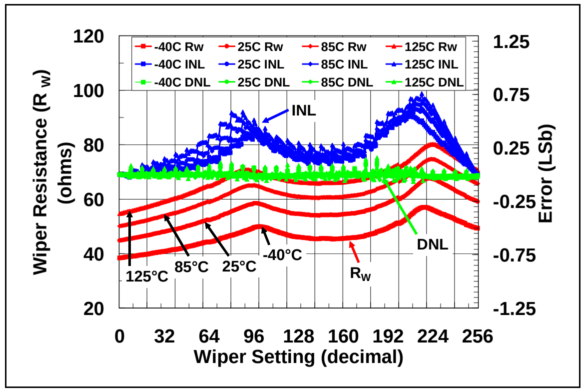


FIGURE 2-9: 5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

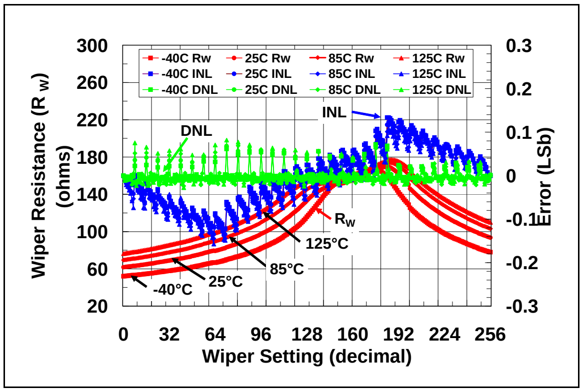


FIGURE 2-7: 5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).

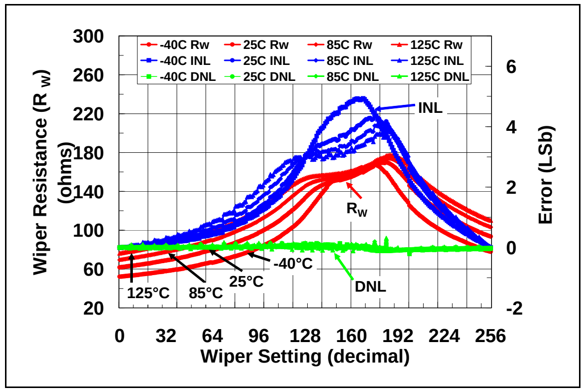
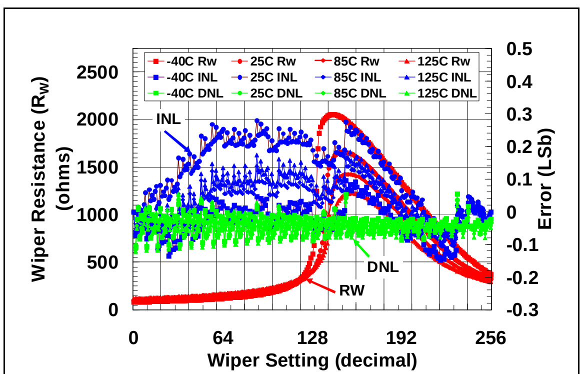
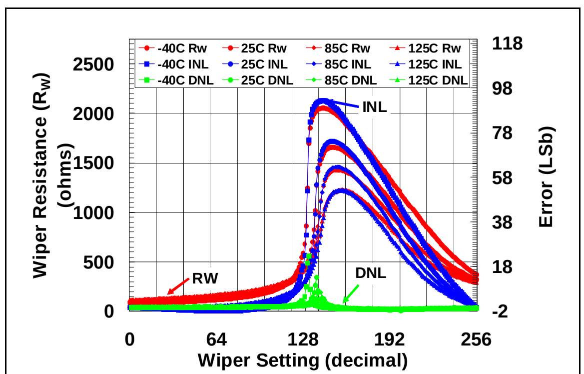


FIGURE 2-10: 5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-8: 5 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-11: 5 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

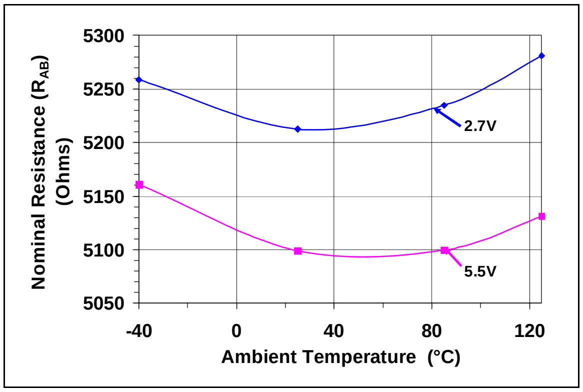

FIGURE 2-12: *5 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

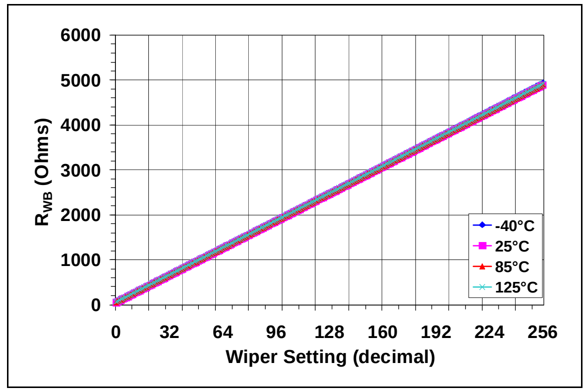

FIGURE 2-13: *5 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

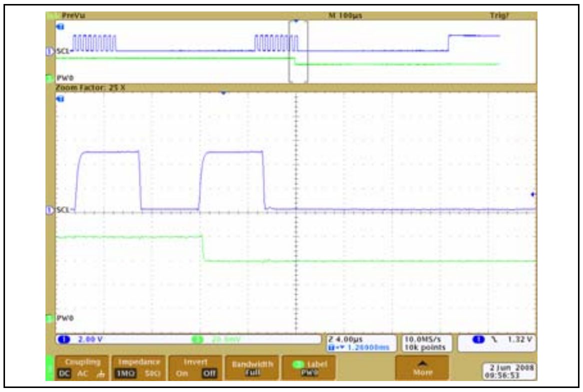

FIGURE 2-14: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

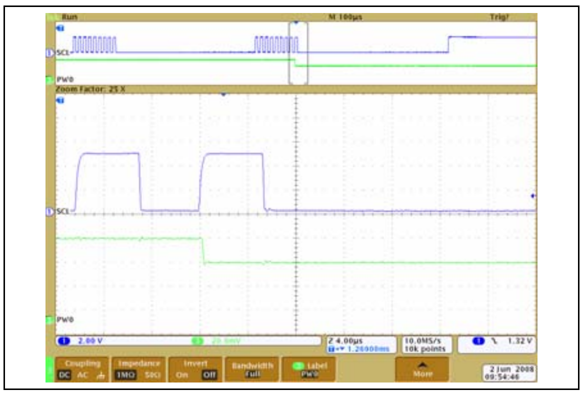

FIGURE 2-15: *5 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

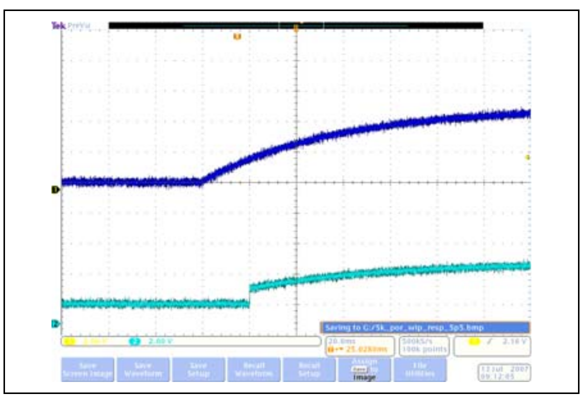

FIGURE 2-16: *5 kΩ – Power-Up Wiper Response Time (20 ms/Div).*

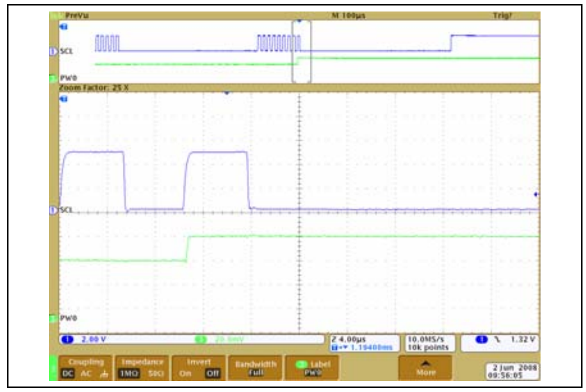

FIGURE 2-17: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

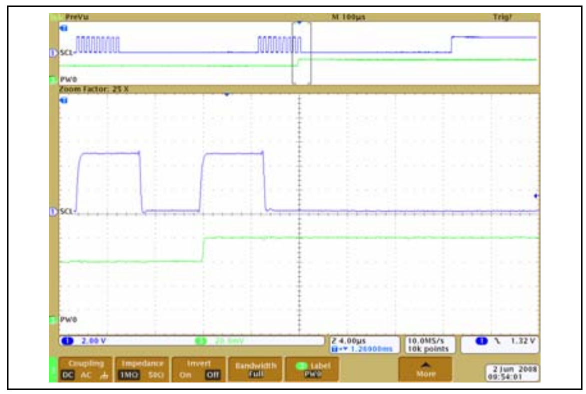

FIGURE 2-18: *5 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

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Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 5V$, $V_{SS} = 0V$.

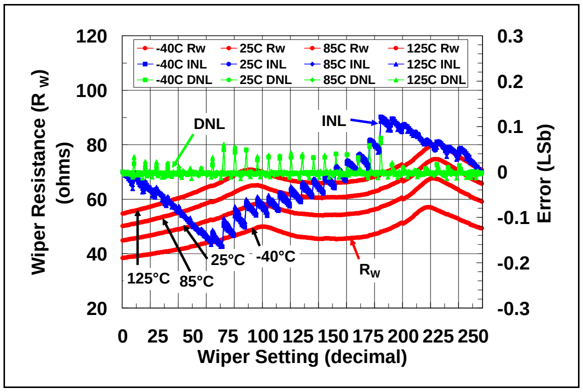


FIGURE 2-19: 10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

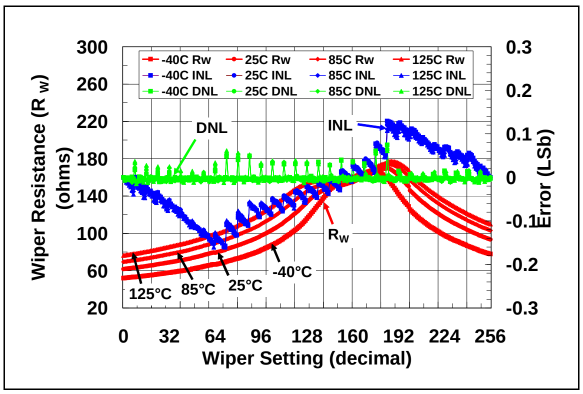
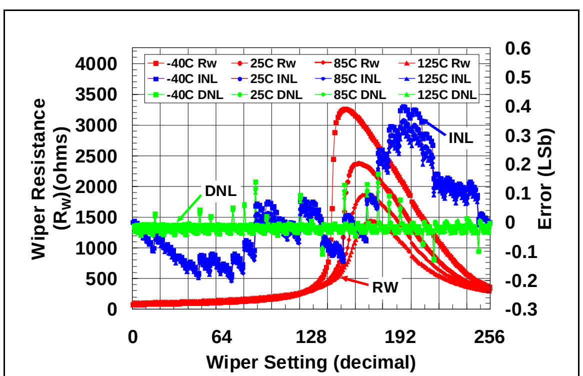


FIGURE 2-20: 10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-21: 10 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).

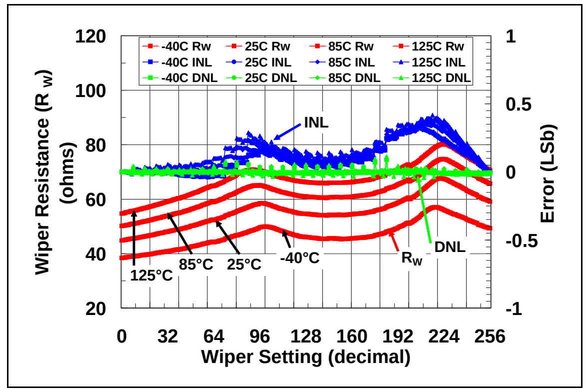


FIGURE 2-22: 10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

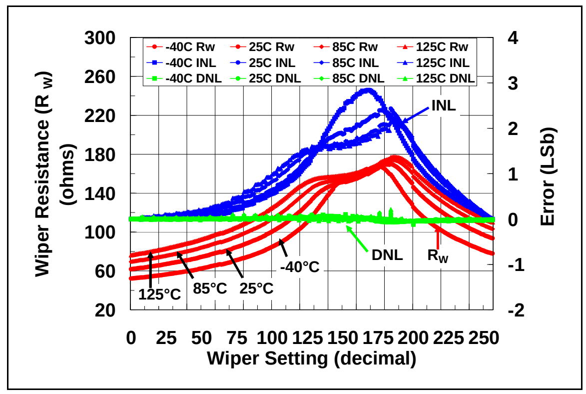
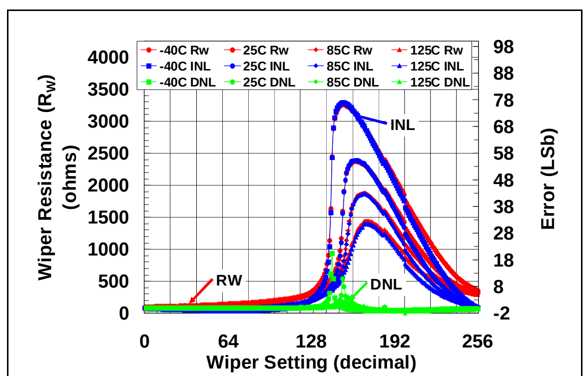


FIGURE 2-23: 10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-24: 10 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

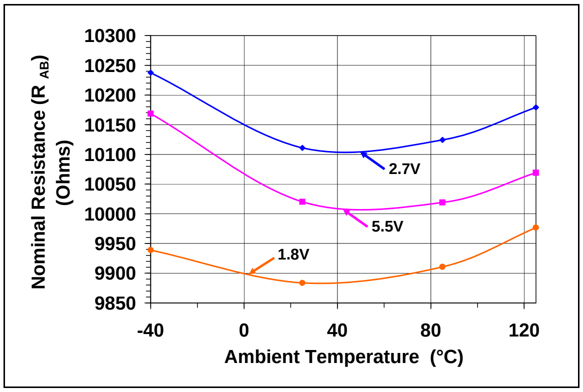


FIGURE 2-25: *10 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

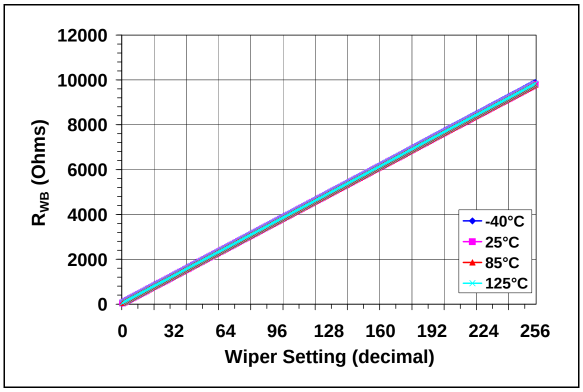


FIGURE 2-26: *10 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

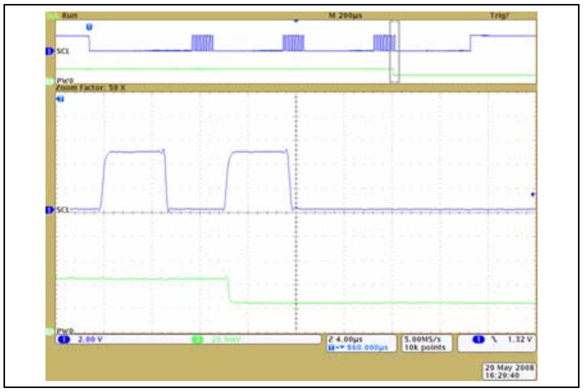

FIGURE 2-27: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

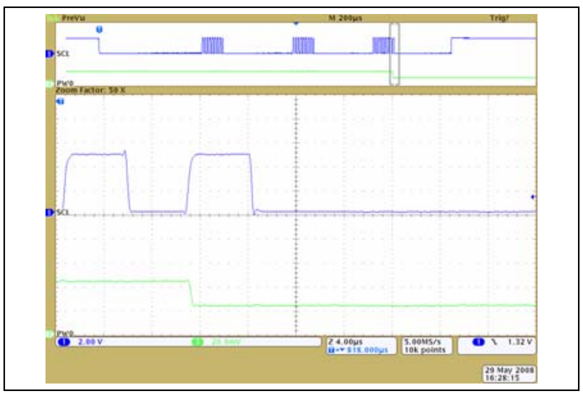

FIGURE 2-28: *10 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

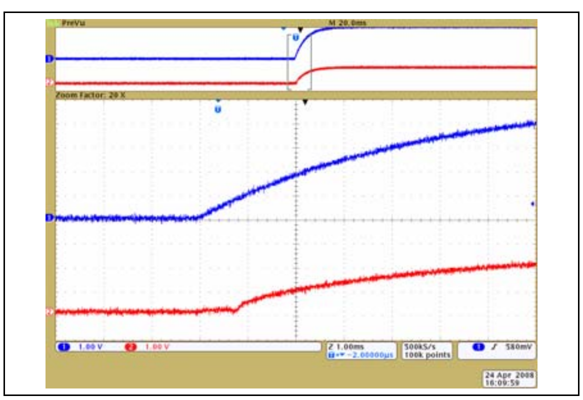

FIGURE 2-29: *10 kΩ – Power-Up Wiper Response Time (1 µs/Div).*

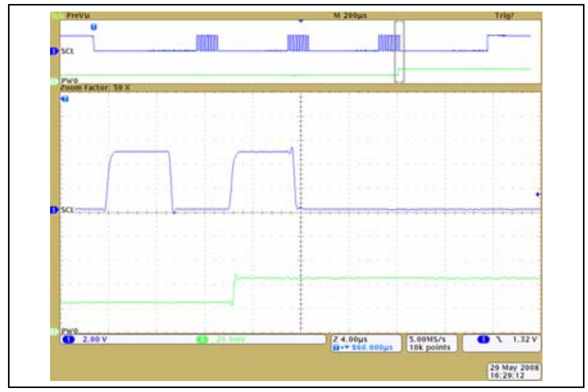

FIGURE 2-30: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

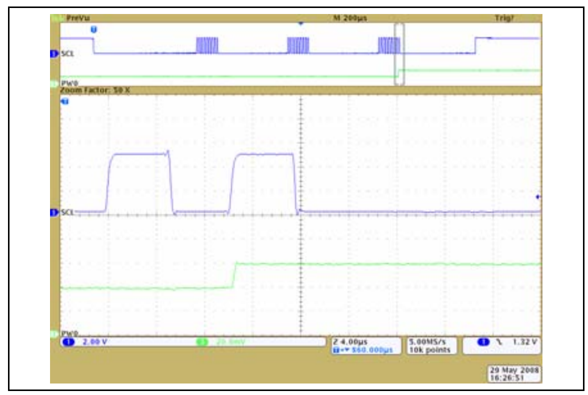

FIGURE 2-31: *10 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

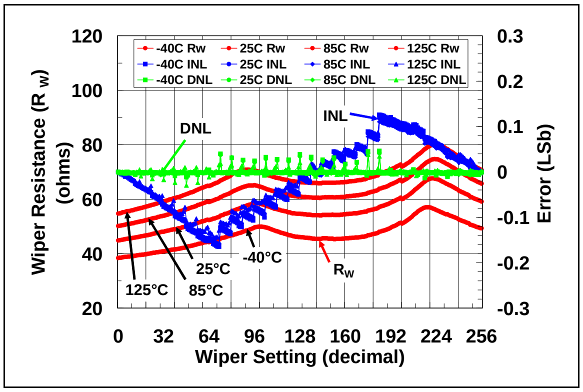


FIGURE 2-32: 50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

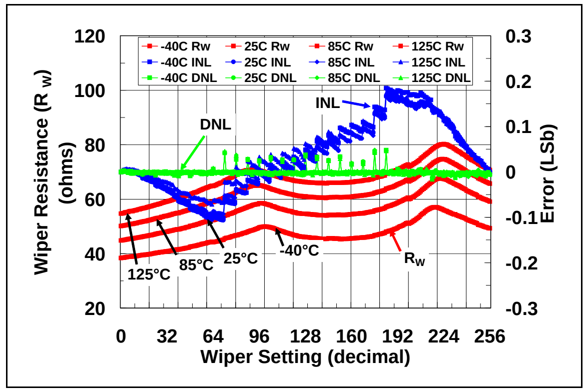


FIGURE 2-35: 50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).

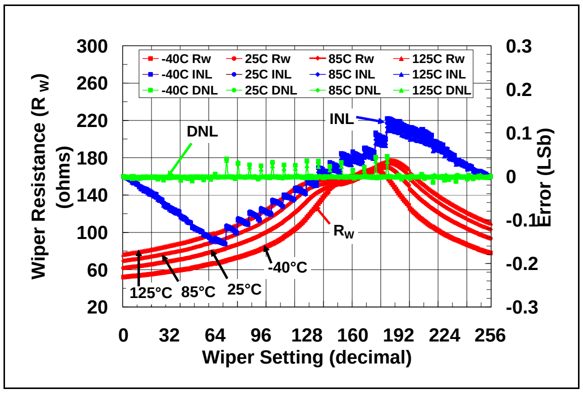


FIGURE 2-33: 50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).

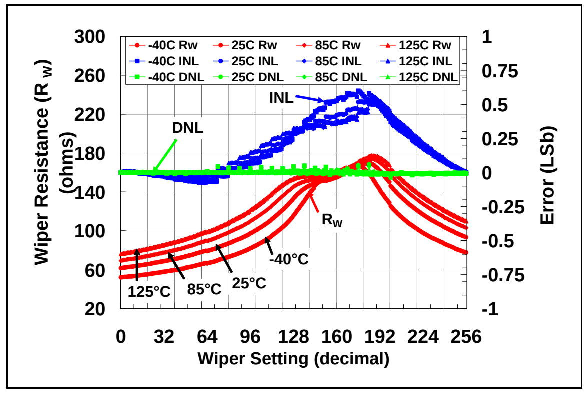
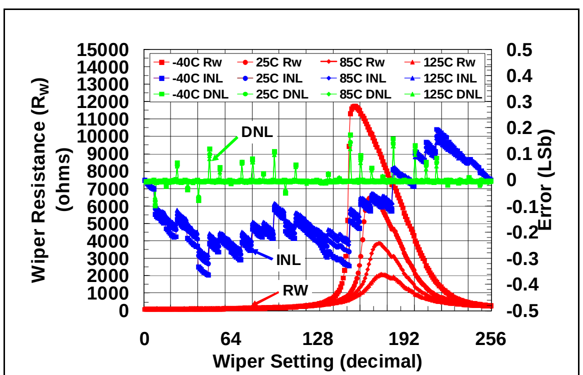
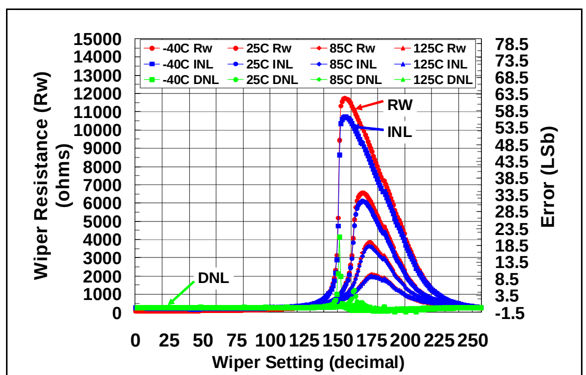


FIGURE 2-36: 50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-34: 50 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).



Note: Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-37: 50 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

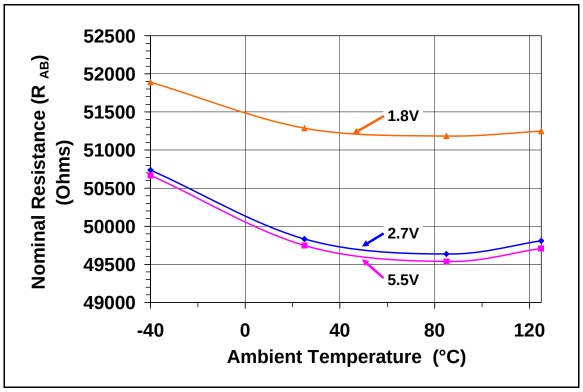

FIGURE 2-38: *50 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

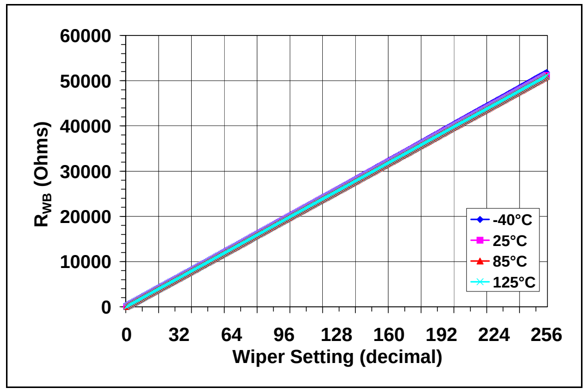

FIGURE 2-39: *50 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

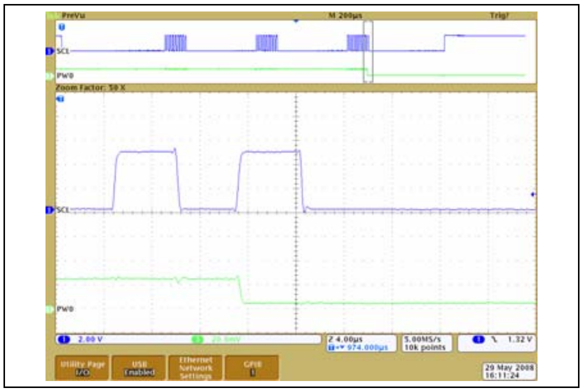

FIGURE 2-40: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

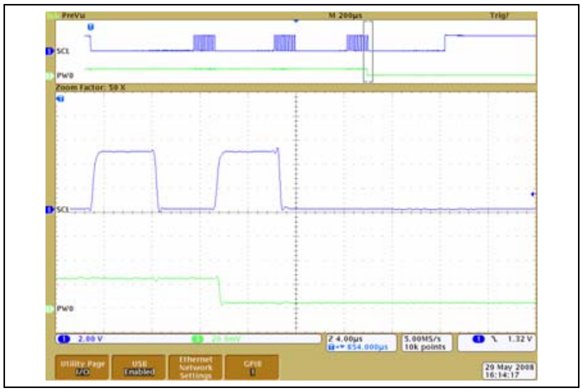

FIGURE 2-41: *50 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

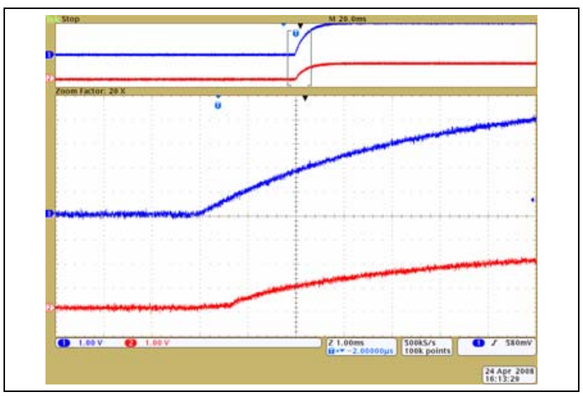

FIGURE 2-42: *50 kΩ – Power-Up Wiper Response Time (1 µs/Div).*

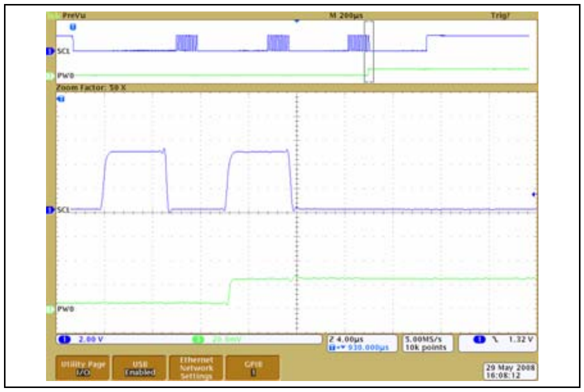

FIGURE 2-43: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

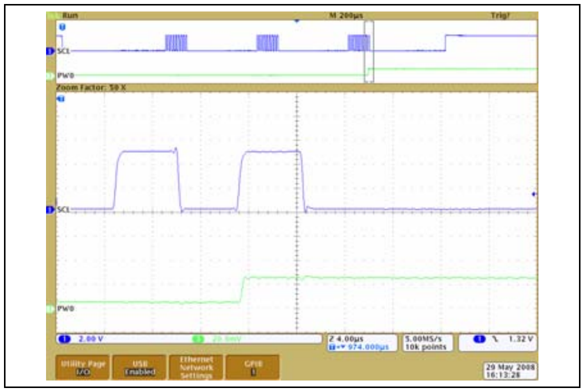

FIGURE 2-44: *50 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

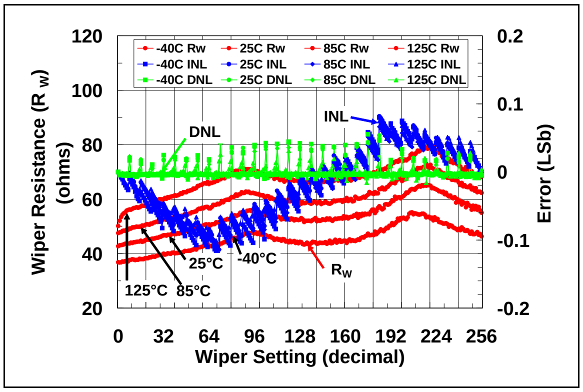


FIGURE 2-45: *100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

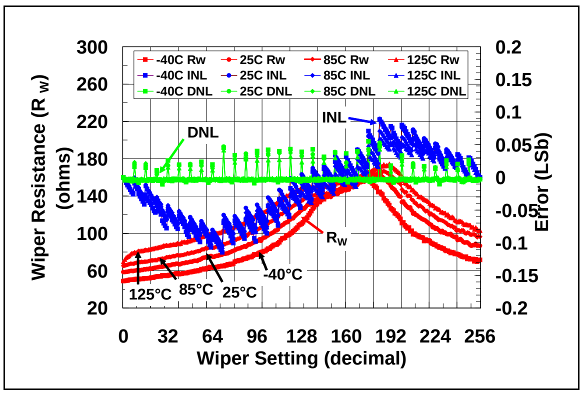
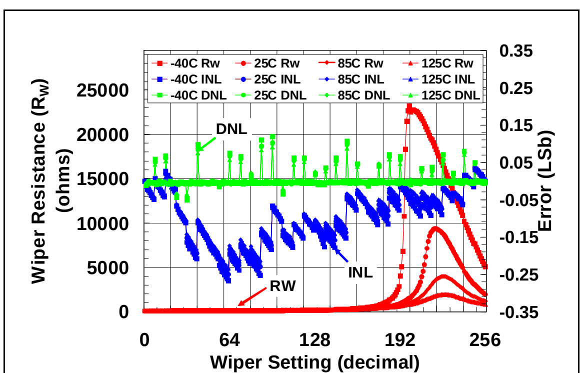


FIGURE 2-46: *100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-47: *100 kΩ Pot Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

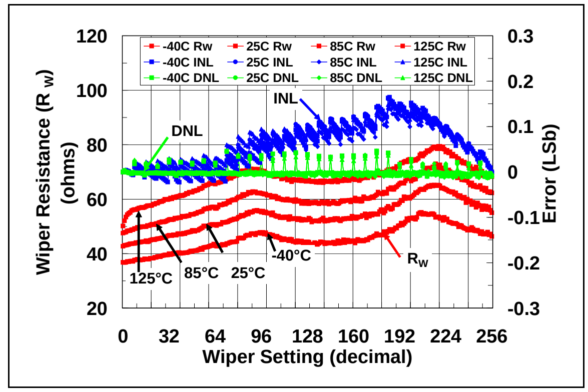


FIGURE 2-48: *100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 5.5V).*

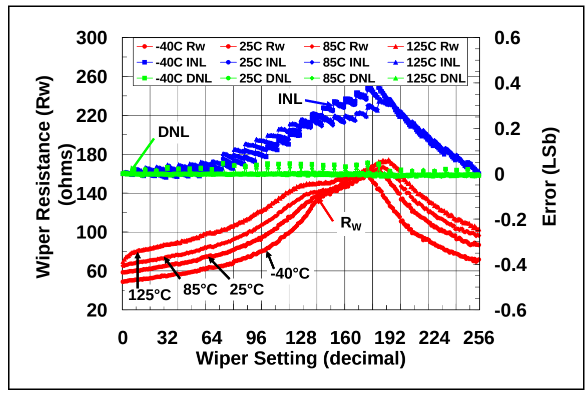
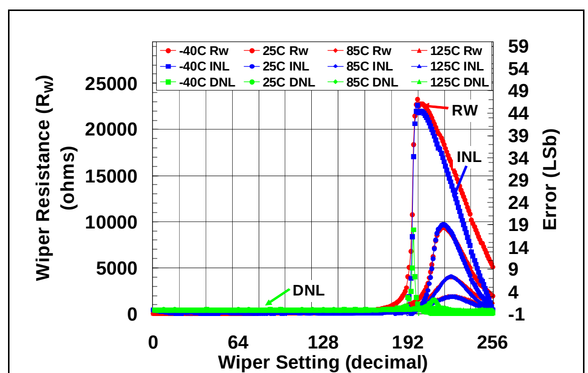


FIGURE 2-49: *100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 3.0V).*



Note:	Refer to AN1080 for additional information on the characteristics of the wiper resistance (R_W) with respect to device voltage and wiper setting value.

FIGURE 2-50: *100 kΩ Rheo Mode – R_W (Ω), INL (LSb), DNL (LSb) vs. Wiper Setting and Ambient Temperature (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

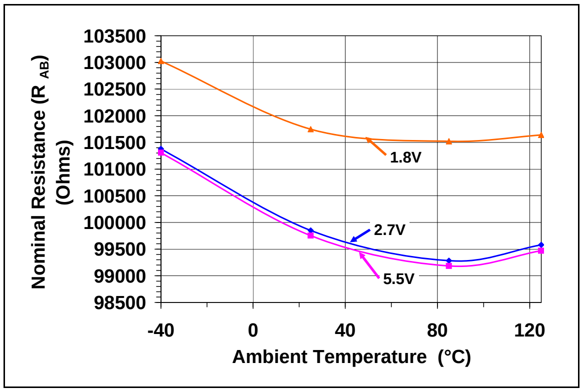


FIGURE 2-51: *100 kΩ – Nominal Resistance (Ω) vs. Ambient Temperature and V_{DD}.*

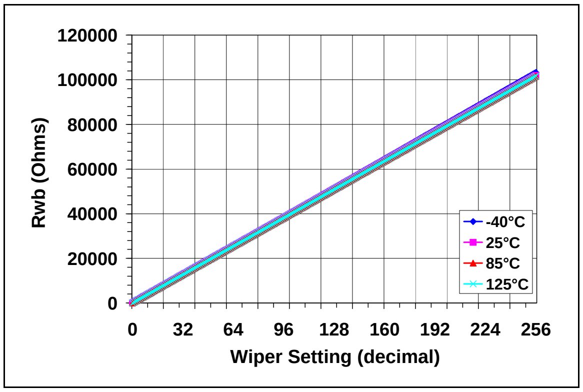


FIGURE 2-52: *100 kΩ – R_{WB} (Ω) vs. Wiper Setting and Ambient Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

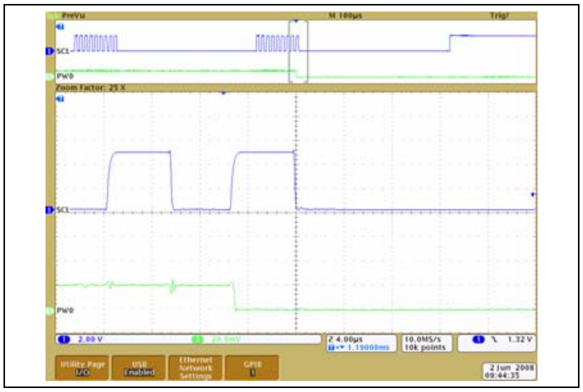

FIGURE 2-53: *100 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 5.5V) (1 µs/Div).*

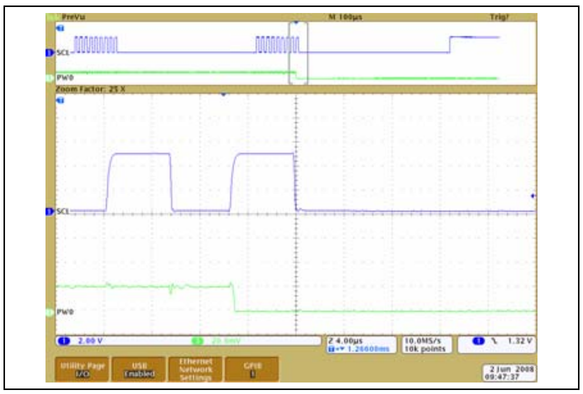

FIGURE 2-54: *100 kΩ – Low-Voltage Decrement Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div).*

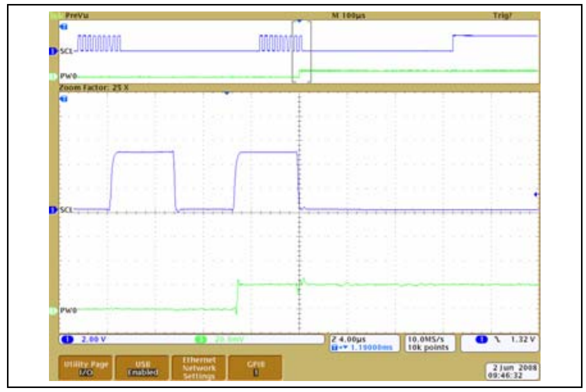

FIGURE 2-55: *100 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} =5.5V) (1 µs/Div).*

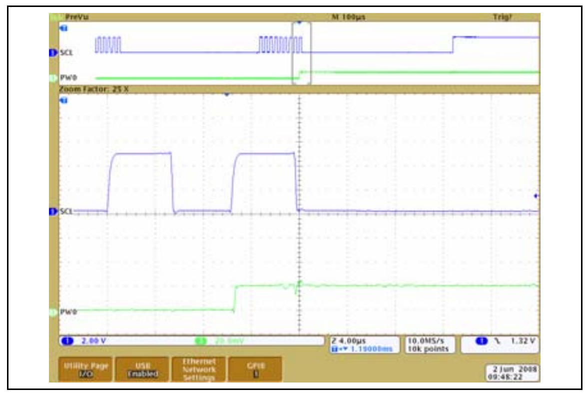

FIGURE 2-56: *100 kΩ – Low-Voltage Increment Wiper Settling Time (V_{DD} = 2.7V) (1 µs/Div)*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

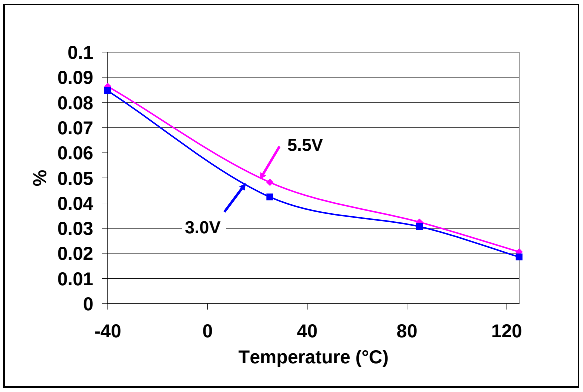

FIGURE 2-57: *Resistor Network 0 to Resistor Network 1 R_{AB} (5 kΩ) Mismatch vs. V_{DD} and Temperature.*

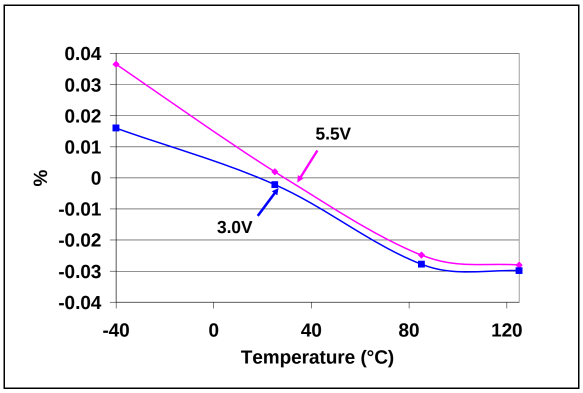

FIGURE 2-58: *Resistor Network 0 to Resistor Network 1 R_{AB} (10 kΩ) Mismatch vs. V_{DD} and Temperature.*

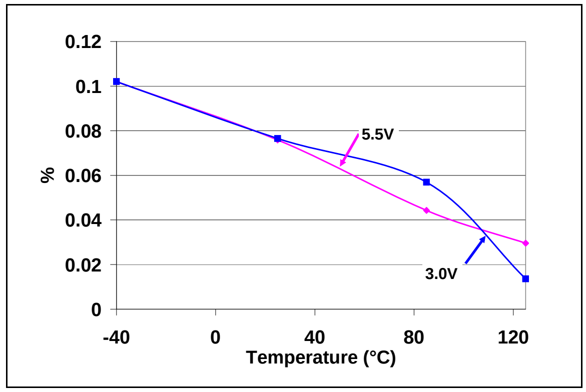

FIGURE 2-59: *Resistor Network 0 to Resistor Network 1 R_{AB} (50 kΩ) Mismatch vs. V_{DD} and Temperature.*

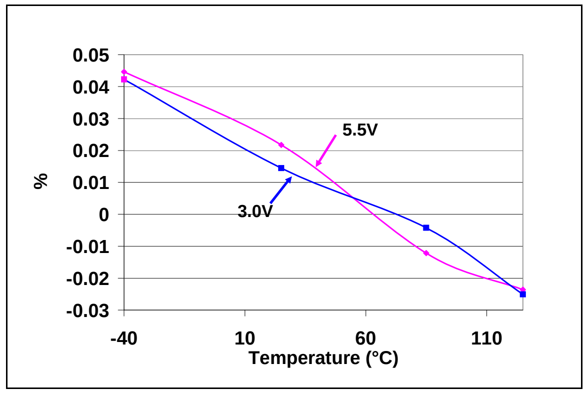

FIGURE 2-60: *Resistor Network 0 to Resistor Network 1 R_{AB} (100 kΩ) Mismatch vs. V_{DD} and Temperature.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

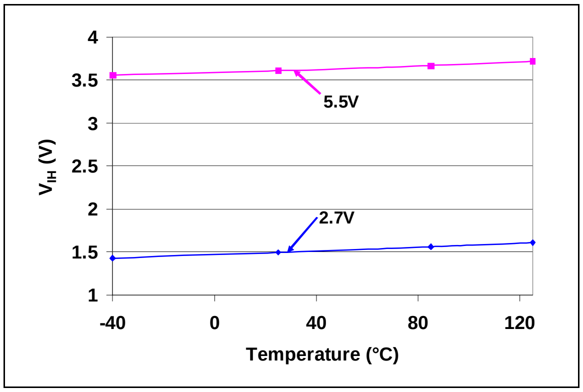

FIGURE 2-61: *V_{IH} (SDA, SCL) vs. V_{DD} and Temperature.*

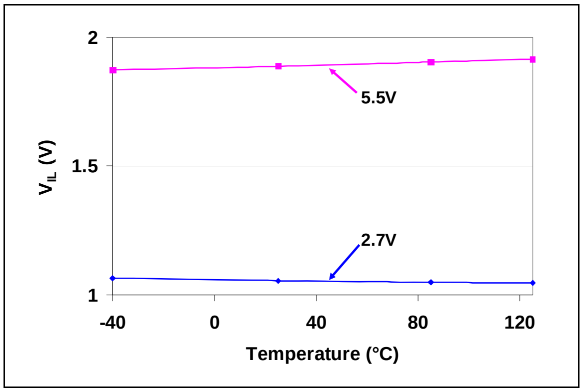

FIGURE 2-62: *V_{IL} (SDA, SCL) vs. V_{DD} Temperature.*

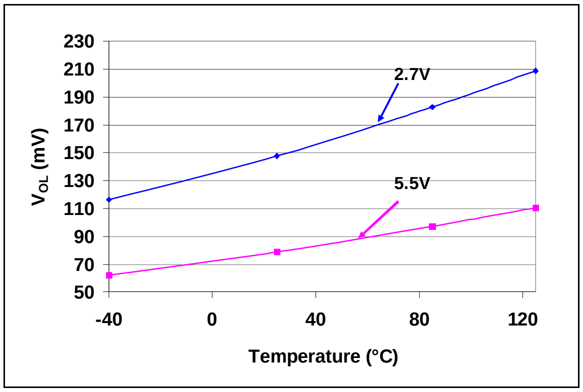

FIGURE 2-63: *V_{OL} (SDA) vs. V_{DD} and Temperature (I_{OL} = 3 mA).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5V, V_{SS} = 0V.

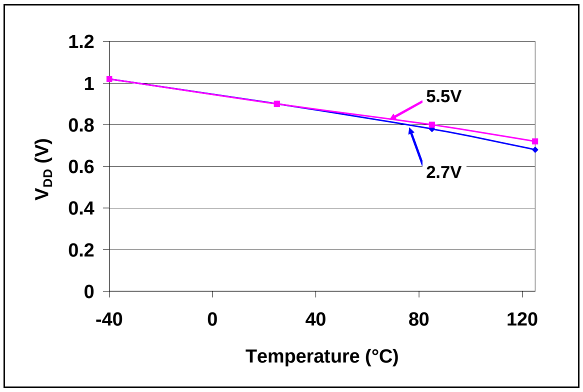

FIGURE 2-64: *POR/BOR Trip point vs. V_{DD} and Temperature.*

2.1 Test Circuits

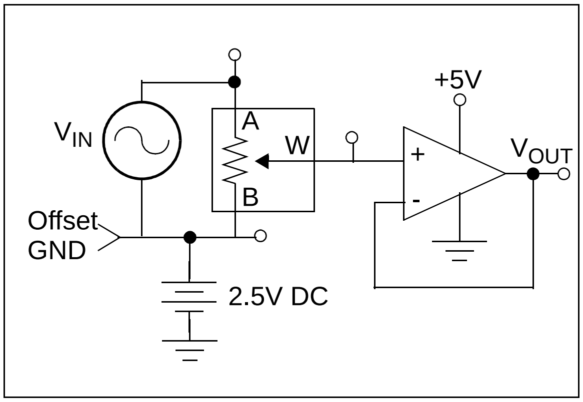

FIGURE 2-65: *-3 db Gain vs. Frequency Test.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1. Additional descriptions of the device pins follows.

TABLE 3-1: PINOUT DESCRIPTION FOR THE MCP453X/455X/463X/465X

Pin								Weak Pull-up/ down (1)	Standard Function
Single		Dual			Symbol	I/O	Buffer Type		
Rheo	Pot (1)	Rheo	Pot						
8L	8L	10L	14L	16L					
1	1	1	1	16	HVC/A0	I	HV w/ST	“smart”	High Voltage Command / Address 0.
2	2	2	2	1	SCL	I	HV w/ST	No	I^2C clock input.
3	3	3	3	2	SDA	I/O	HV w/ST	No	I^2C serial data I/O. Open Drain output
4	4	4	4	3, 4	V_{SS}	—	P	—	Ground
—	—	5	5	5	P1B	A	Analog	No	Potentiometer 1 Terminal B
—	—	6	6	6	P1W	A	Analog	No	Potentiometer 1 Wiper Terminal
—	—	—	7	7	P1A	A	Analog	No	Potentiometer 1 Terminal A
—	5	—	8	8	P0A	A	Analog	No	Potentiometer 0 Terminal A
5	6	7	9	9	P0W	A	Analog	No	Potentiometer 0 Wiper Terminal
6	7	8	10	10	P0B	A	Analog	No	Potentiometer 0 Terminal B
—	—	—	11	11, 12	NC	—	—	—	No Connection
—	—	—	12	13	A2	I	HV w/ST	“smart”	Address 2
7	—	9	13	14	A1	I	HV w/ST	“smart”	Address 1
8	8	10	14	15	V_{DD}	—	P	—	Positive Power Supply Input
9	9	11	—	17	EP	—	—	—	Exposed Pad **(Note 2)**

Legend: HV w/ST = High Voltage tolerant input (with Schmidtt trigger input)
A = Analog pins (Potentiometer terminals) I = digital input (high Z)
O = digital output I/O = Input / Output
P = Power

Note 1: The pin’s “smart” pull-up shuts off while the pin is forced low. This is done to reduce the standby and shut-down current.

2: The DFN and QFN packages have a contact on the bottom of the package. This contact is conductively connected to the die substrate, and therefore should be unconnected or connected to the same ground as the device’s V_{SS} pin.

3.1 High Voltage Command / Address 0 (HVC/A0)

The HVC/A0 pin is the Address 0 input for the I^2C interface as well as the High Voltage Command pin. At the device's POR/BOR the value of the A0 address bit is latched. This input along with the A2 and A1 pins completes the device address. This allows up to 8 MCP45xx/46xx devices can be on a single I^2C bus.

During normal operation the the voltage on this pin determines if the I^2C command is a normal command or a High Voltage command (when HVC/A0 = V_{IHH}).

3.2 Serial Clock (SCL)

The SCL pin is the serial interfaces Serial Clock pin. This pin is connected to the Host Controllers SCL pin. The MCP45XX/46XX is a slave device, so it's SCL pin accepts only external clock signals.

3.3 Serial Data (SDA)

The SDA pin is the serial interfaces Serial Data pin. This pin is connected to the Host Controllers SDA pin. The SDA pin is an open-drain N-channel driver.

3.4 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

3.5 Potentiometer Terminal B

The terminal B pin is connected to the internal potentiometer's terminal B.

The potentiometer's terminal B is the fixed connection to the Zero Scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x00 for both 7-bit and 8-bit devices.

The terminal B pin does not have a polarity relative to the terminal W or A pins. The terminal B pin can support both positive and negative current. The voltage on terminal B must be between V_{SS} and V_{DD}.

MCP46XX devices have two terminal B pins, one for each resistor network.

3.6 Potentiometer Wiper (W) Terminal

The terminal W pin is connected to the internal potentiometer's terminal W (the wiper). The wiper terminal is the adjustable terminal of the digital potentiometer. The terminal W pin does not have a polarity relative to terminals A or B pins. The terminal W pin can support both positive and negative current. The voltage on terminal W must be between V_{SS} and V_{DD}.

MCP46XX devices have two terminal W pins, one for each resistor network.

3.7 Potentiometer Terminal A

The terminal A pin is available on the MCP4XX1 devices, and is connected to the internal potentiometer's terminal A.

The potentiometer's terminal A is the fixed connection to the Full-Scale wiper value of the digital potentiometer. This corresponds to a wiper value of 0x100 for 8-bit devices or 0x80 for 7-bit devices.

The terminal A pin does not have a polarity relative to the terminal W or B pins. The terminal A pin can support both positive and negative current. The voltage on terminal A must be between V_{SS} and V_{DD}.

The terminal A pin is not available on the MCP4XX2 devices, and the internally terminal A signal is floating.

MCP46X1 devices have two terminal A pins, one for each resistor network.

3.8 Address 2 (A2)

The A2 pin is the I^2C interface's Address 2 pin. Along with the A1 and A0 pins, up to 8 MCP45XX/46XX devices can be on a single I^2C bus.

3.9 Address 1 (A1)

The A2 pin is the I^2C interface's Address 1 pin. Along with the A2 and A0 pins, up to 8 MCP45XX/46XX devices can be on a single I^2C bus.

3.10 Positive Power Supply Input (V_{DD})

The V_{DD} pin is the device's positive power supply input. The input power supply is relative to V_{SS}.

While the device $V_{DD} < V_{min}$ (2.7V), the electrical performance of the device may not meet the data sheet specifications.

3.11 No Connect (NC)

These pins should be either connected to V_{DD} or V_{SS}.

3.12 Exposed Pad (EP)

This pad is conductively connected to the device's substrate. This pad should be tied to the same potential as the V_{SS} pin (or left unconnected). This pad could be used to assist as a heat sink for the device when connected to a PCB heat sink.

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4.0 FUNCTIONAL OVERVIEW

This Data Sheet covers a family of thirty-two Digital Potentiometer and Rheostat devices that will be referred to as MCP4XXX. The MCP4XX1 devices are the Potentiometer configuration, while the MCP4XX2 devices are the Rheostat configuration.

As the **Device Block Diagram** shows, there are four main functional blocks. These are:

- **POR/BOR Operation**
- **Memory Map**
- **Resistor Network**
- **Serial Interface (I^2C)**

The POR/BOR operation and the Memory Map are discussed in this section and the Resistor Network and I^2C operation are described in their own sections. The **Device Commands** commands are discussed in **Section 7.0 "Device Commands"**.

4.1 POR/BOR Operation

The Power-on Reset is the case where the device is having power applied to it starting from the V_{SS} level. The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

The devices RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of incrementing, decrementing, reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

When the device powers up, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage. Once the V_{DD} voltage crosses the V_{POR}/V_{BOR} voltage the following happens:

- Volatile wiper register is loaded with value in the corresponding non-volatile wiper register
- The TCON register is loaded it's default value
- The device is capable of digital operation

4.1.2 BROWN-OUT RESET

When the device powers down, the device V_{DD} will cross the V_{POR}/V_{BOR} voltage.

Once the V_{DD} voltage decreases below the V_{POR}/V_{BOR} voltage the Serial Interface is disabled.

If the V_{DD} voltage decreases below the V_{RAM} voltage the following happens:

- Volatile wiper registers may become corrupted
- TCON register may become corrupted

As the voltage recovers above the V_{POR}/V_{BOR} voltage see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the volatile memory location to become corrupted.

4.2 Memory Map

The device memory map supports 16 locations, of which 3 locations are used. Each location is 9-bits wide (16x9 bits). This memory space is shown in Table 4-1.

TABLE 4-1: MEMORY MAP

Address	Function	Memory Type
00h	Volatile Wiper 0	RAM
01h	Volatile Wiper 1	RAM
02h	Reserved	—
03h	Reserved	—
04h	Volatile TCON Register	RAM
05h	Reserved	RAM
06h - 0Fh	Reserved	—

4.2.1 VOLATILE MEMORY (RAM)

There are four Volatile Memory locations. These are:

- Volatile Wiper 0
- Volatile Wiper 1
  (Dual Resistor Network devices only)
- Terminal Control (TCON) Register
- Reserved

The volatile memory starts functioning at the RAM retention voltage (V_{RAM}).

4.2.1.1 Address 05h (Reserved)

This memory location is Reserved and is mapped to the Status Register of the Non-Volatile MCP45XX/46XX devices. Since the Non-Volatile devices bits are not used by the volatile device, this location is reserved. Reading this address wil result in a value of 1F7h.

4.2.1.2 Terminal Control (TCON) Register

This register contains 8 control bits. Four bits are for Wiper 0, and four bits are for Wiper 1. Register 4-1 describes each bit of the TCON register.

The state of each resistor network terminal connection is individually controlled. That is, each terminal connection (A, B and W) can be individually connected/ disconnected from the resistor network. This allows the system to minimize the currents through the digital potentiometer.

The value that is written to this register will appear on the resistor network terminals when the serial command has completed.

When the WL1 bit is enabled, writes to the TCON register bits R1HW, R1A, R1W, and R1B are inhibited.

When the WL0 bit is enabled, writes to the TCON register bits R0HW, R0A, R0W, and R0B are inhibited.

On a POR/BOR this register is loaded with 1FFh (9-bits), for all terminals connected. The Host Controller needs to detect the POR/BOR event and then update the Volatile TCON register value.

Additionally, there is a bit which enables the operation of General Call commands.

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REGISTER 4-1: TCON BITS (ADDRESS = 0x04) (1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
GCEN	R1HW	R1A	R1W	R1B	R0HW	R0A	R0W	R0B
bit 8								bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 8 **GCEN:** General Call Enable bit
This bit specifies if I^2C General Call commands are accepted
1 = Enable Device to “Accept” the General Call Address (0000h)
0 = The General Call Address is disabled

bit 7 **R1HW:** Resistor 1 Hardware Configuration Control bit
This bit forces Resistor 1 into the “shutdown” configuration of the Hardware pin
1 = Resistor 1 is NOT forced to the hardware pin “shutdown” configuration
0 = Resistor 1 is forced to the hardware pin “shutdown” configuration

bit 6 **R1A:** Resistor 1 Terminal A (P1A pin) Connect Control bit
This bit connects/disconnects the Resistor 1 Terminal A to the Resistor 1 Network
1 = P1A pin is connected to the Resistor 1 Network
0 = P1A pin is disconnected from the Resistor 1 Network

bit 5 **R1W:** Resistor 1 Wiper (P1W pin) Connect Control bit
This bit connects/disconnects the Resistor 1 Wiper to the Resistor 1 Network
1 = P1W pin is connected to the Resistor 1 Network
0 = P1W pin is disconnected from the Resistor 1 Network

bit 4 **R1B:** Resistor 1 Terminal B (P1B pin) Connect Control bit
This bit connects/disconnects the Resistor 1 Terminal B to the Resistor 1 Network
1 = P1B pin is connected to the Resistor 1 Network
0 = P1B pin is disconnected from the Resistor 1 Network

bit 3 **R0HW:** Resistor 0 Hardware Configuration Control bit
This bit forces Resistor 0 into the “shutdown” configuration of the Hardware pin
1 = Resistor 0 is NOT forced to the hardware pin “shutdown” configuration
0 = Resistor 0 is forced to the hardware pin “shutdown” configuration

bit 2 **R0A:** Resistor 0 Terminal A (P0A pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Terminal A to the Resistor 0 Network
1 = P0A pin is connected to the Resistor 0 Network
0 = P0A pin is disconnected from the Resistor 0 Network

bit 1 **R0W:** Resistor 0 Wiper (P0W pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Wiper to the Resistor 0 Network
1 = P0W pin is connected to the Resistor 0 Network
0 = P0W pin is disconnected from the Resistor 0 Network

bit 0 **R0B:** Resistor 0 Terminal B (P0B pin) Connect Control bit
This bit connects/disconnects the Resistor 0 Terminal B to the Resistor 0 Network
1 = P0B pin is connected to the Resistor 0 Network
0 = P0B pin is disconnected from the Resistor 0 Network

Note 1: These bits do not affect the wiper register values.

NOTES:

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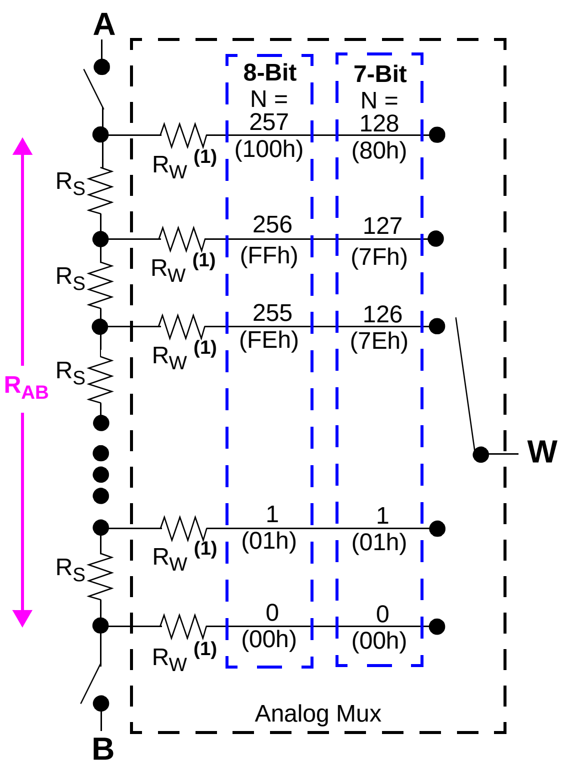
5.0 RESISTOR NETWORK

The Resistor Network has either 7-bit or 8-bit resolution. Each Resistor Network allows zero scale to full-scale connections. Figure 5-1 shows a block diagram for the resistive network of a device.

The Resistor Network is made up of several parts. These include:

- Resistor Ladder
- Wiper
- Shutdown (Terminal Connections)

Devices have either one or two resistor networks, These are referred to as Pot 0 and Pot 1.



Note 1: The wiper resistance is dependent on several factors including, wiper code, device V_{DD}, Terminal voltages (on A, B, and W), and temperature.
Also for the same conditions, each tap selection resistance has a small variation. This R_W variation has greater effects on some specifications (such as INL) for the smaller resistance devices (5.0 kΩ) compared to larger resistance devices (100.0 kΩ).

FIGURE 5-1: *Resistor Block Diagram.*

5.1 Resistor Ladder Module

The resistor ladder is a series of equal value resistors (R_S) with a connection point (tap) between the two resistors. The total number of resistors in the series (ladder) determines the R_{AB} resistance (see Figure 5-1). The end points of the resistor ladder are connected to analog switches which are connected to the device Terminal A and Terminal B pins. The R_{AB} (and R_S) resistance has small variations over voltage and temperature.

For an 8-bit device, there are 256 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 256 resistors thus providing 257 possible settings (including terminal A and terminal B).

For a 7-bit device, there are 128 resistors in a string between terminal A and terminal B. The wiper can be set to tap onto any of these 128 resistors thus providing 129 possible settings (including terminal A and terminal B).

Equation 5-1 shows the calculation for the step resistance.

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{AB}}{(256)} \quad \text{8-bit Device}$$

$$R_S = \frac{R_{AB}}{(128)} \quad \text{7-bit Device}$$

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5.2 Wiper

Each tap point (between the R_S resistors) is a connection point for an analog switch. The opposite side of the analog switch is connected to a common signal which is connected to the Terminal W (Wiper) pin.

A value in the volatile wiper register selects which analog switch to close, connecting the W terminal to the selected node of the resistor ladder.

The wiper can connect directly to Terminal B or to Terminal A. A zero-scale connections, connects the Terminal W (wiper) to Terminal B (wiper setting of 000h). A full-scale connections, connects the Terminal W (wiper) to Terminal A (wiper setting of 100h or 80h). In these configurations the only resistance between the Terminal W and the other Terminal (A or B) is that of the analog switches.

A wiper setting value greater than full-scale (wiper setting of 100h for 8-bit device or 80h for 7-bit devices) will also be a Full-Scale setting (Terminal W (wiper) connected to Terminal A). Table 5-1 illustrates the full wiper setting map.

Equation 5-2 illustrates the calculation used to determine the resistance between the wiper and terminal B.

EQUATION 5-2: R_{WB} CALCULATION

$$R_{WB} = \frac{R_{AB}N}{(256)} + R_W$$

8-bit Device

N = 0 to 256 (decimal)

$$R_{WB} = \frac{R_{AB}N}{(128)} + R_W$$

7-bit Device

N = 0 to 128 (decimal)

TABLE 5-1: VOLATILE WIPER VALUE VS. WIPER POSITION MAP

Wiper Setting		Properties
7-bit Pot	**8-bit Pot**	
3FFh 081h	3FFh 101h	Reserved (Full-Scale (W = A)), Increment and Decrement commands ignored
080h	100h	Full-Scale (W = A), Increment commands ignored
07Fh 041h	0FFh 081	W = N
040h	080h	W = N (Mid-Scale)
03Fh 001h	07Fh 001	W = N
000h	000h	Zero Scale (W = B) Decrement command ignored

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5.3 Shutdown

Shutdown is used to minimize the device's current consumption. The MCP4XXX achieves this through the **Terminal Control Register (TCON)**.

5.3.1 TERMINAL CONTROL REGISTER (TCON)

The Terminal Control (TCON) register is a volatile register used to configure the connection of each resistor network terminal pin (A, B, and W) to the Resistor Network. This bits are described in Register 4-1.

When the RxHW bit is a "0", the selected resistor network is forced into the following state:

- The PxA terminal is disconnected
- The PxW terminal is simultaneously connected to the PxB terminal (see Figure 5-2)
- The Serial Interface is NOT disabled, and all Serial Interface activity is executed

Alternate low power configurations may be achieved with the RxA, RxW, and RxB bits.

> **Note 1:** The RxHW bits are identical to the RxHW bits of the MCP41XX/42XX devices. The MCP42XX devices also have a $\overline{\text{SHDN}}$ pin which forces the resistor network into the same state as that resistor networks RxHW bit.
>
> **2:** When RxHW = "0", the state of the TCON register RxA, RxW, and RxB bits is overridden (ignored). When the state of the RxHW bit returns to "1", the TCON register RxA, RxW, and RxB bits return to controlling the terminal connection state. In other words, the RxHW bit does not corrupt the state of the RxA, RxW, and RxB bits.

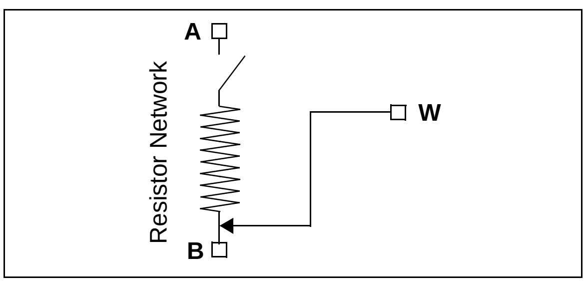

FIGURE 5-2: Resistor Network Shutdown Configuration.

5.3.2 INTERACTION OF RxHW BIT AND RxA, RxW, AND RxB BITS (TCON REGISTER)

Using the TCON bits allows each resistor network (Pot 0 and Pot 1) to be individually "shutdown".

The state of the RxHW bit does NOT corrupt the other bit values in the TCON register nor the value of the Volatile Wiper Registers. When the Shutdown mode is exited (RxHW changes state from "0" to "1"):

- The device returns to the Wiper setting specified by the Volatile Wiper value
- The RxA, RxB, and RxW bits return to controlling the terminal connection state of that resistor network

NOTES:

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6.0 SERIAL INTERFACE (I^2C)

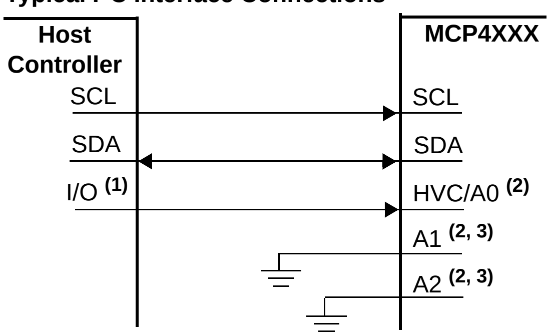
The MCP45XX/46XX devices support the I^2C serial protocol. The MCP45XX/46XX I^2C's module operates in Slave mode (does not generate the serial clock).

Figure 6-1 shows a typical I^2C Interface connection. All I^2C interface signals are high-voltage tolerant.

The MCP45XX/46XX devices use the two-wire I^2C serial interface. This interface can operate in standard, fast or High-Speed mode. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions. The MCP45XX/46XX device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller) which sends the START bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits, and the $R/\overline{W}$ bit.

Refer to the Phillips I^2C document for more details of the I^2C specifications.

Typical I^2C Interface Connections



Note 1: If High voltage commands are desired, some type of external circuitry needs to be implemented.

2: These pins have internal pull-ups. If faster rise times are required, then external pull-ups should be added.

3: This pin could be tied high, low, or connected to an I/O pin of the Host Controller.

FIGURE 6-1: *Typical I^2C Interface Block Diagram.*

6.1 Signal Descriptions

The I^2C interface uses up to five pins (signals). These are:

- SDA (Serial Data)
- SCL (Serial Clock)
- A0 (Address 0 bit)
- A1 (Address 1 bit)
- A2 (Address 2 bit)

6.1.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the START and STOP conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is HIGH will be interpreted as a START or a STOP condition.

6.1.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin. The MCP45XX/46XX supports three I^2C interface clock modes:

- Standard Mode: clock rates up to 100 kHz
- Fast Mode: clock rates up to 400 kHz
- High-Speed Mode (HS mode): clock rates up to 3.4 MHz

The MCP4XXX will not strech the clock signal (SCL) since memory read acceses occur fast enough.

Depending on the clock rate mode, the interface will display different characteristics.

6.1.3 THE ADDRESS BITS (A2:A1:A0)

There are up to three hardware pins used to specify the device address. The number of adress pins is determined by the part number.

Address 0 is multiplexed with the High Voltage Command (HVC) function. So the state of A0 is latched on the MCP4XXX's POR/BOR event.

The state of the A2 and A1 pins should be static, that is they should be tied high or tied low.

6.1.3.1 The High Voltage Command (HVC) Signal

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. High Voltage commands are supported for compatibility with the non-volatile devices.

The HVC pin has an internal resistor connection to the MCP45XX/46XXs internal V_{DD} signal.

6.2 I²C Operation

The MCP45XX/46XX's I²C module is compatible with the Philips I²C specification. The following lists some of the modules features:

- 7-bit slave addressing
- Supports three clock rate modes:
  - Standard mode, clock rates up to 100 kHz
  - Fast mode, clock rates up to 400 kHz
  - High-speed mode (HS mode), clock rates up to 3.4 MHz
- Support Multi-Master Applications
- General call addressing
- Internal weak pull-ups on interface signals

The I²C 10-bit addressing mode is not supported.

The Philips I²C specification only defines the field types, field lengths, timings, etc. of a frame. The frame *content* defines the behavior of the device. The frame content for the MCP4XXX is defined in **Section 7.0**.

6.2.1 I²C BIT STATES AND SEQUENCE

Figure 6-8 shows the I²C transfer sequence. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low) / No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

6.2.1.1 Start Bit

The Start bit (see Figure 6-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is "High".

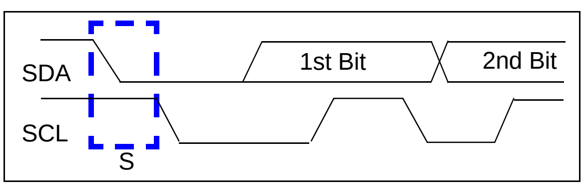


FIGURE 6-2: *Start Bit.*

6.2.1.2 Data Bit

The SDA signal may change state while the SCL signal is Low. While the SCL signal is High, the SDA signal MUST be stable (see Figure 6-5).

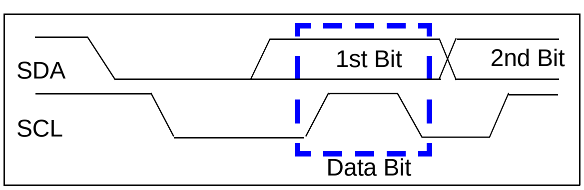


FIGURE 6-3: *Data Bit.*

6.2.1.3 Acknowledge (A) Bit

The A bit (see Figure 6-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically the Slave device will supply an A response after the Start bit and 8 "data" bits have been received. an A bit has the SDA signal low.

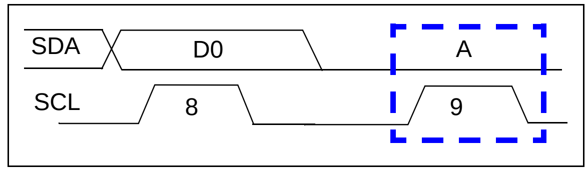


FIGURE 6-4: *Acknowledge Waveform.*

Not A ($\overline{A}$) Response

The $\overline{A}$ bit has the SDA signal high. Table 6-1 shows some of the conditions where the Slave Device will issue a Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then an START bit must be issued to reset the command state machine.

TABLE 6-1: MCP45XX/MCP46XX A / $\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	A	Only if GCEN bit is set
Slave Address valid	A	
Slave Address not valid	$\overline{A}$	
Device Memory Address and specified command (AD3:AD0 and C1:C0) are an invalid combination	$\overline{A}$	After device has received address and command
Bus Collision	N.A.	I²C Module Resets, or a "Don't Care" if the collision occurs on the Masters "Start bit".

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6.2.1.4 Repeated Start Bit

The Repeated Start bit (see Figure 6-5) indicates the current Master Device wishes to continue communicating with the current Slave Device without releasing the I^{2}C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is "High".

> **Note 1:** A bus collision during the Repeated Start condition occurs if:
> - SDA is sampled low when SCL goes from low to high.
> - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

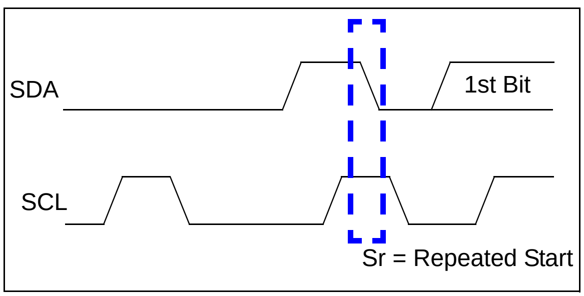

FIGURE 6-5: *Repeat Start Condition Waveform.*

6.2.1.5 Stop Bit

The Stop bit (see Figure 6-6) Indicates the end of the I^{2}C Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is "High".

A Stop bit resets the I^{2}C interface of all MCP4XXX devices.

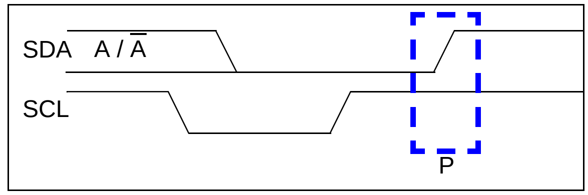

FIGURE 6-6: *Stop Condition Receive or Transmit Mode.*

6.2.2 CLOCK STRETCHING

"Clock Stretching" is something that the receiving Device can do, to allow additional time to "respond" to the "data" that has been received.

The MCP4XXX will not strech the clock signal (SCL) since memory read acceses occur fast enough.

6.2.3 ABORTING A TRANSMISSION

If any part of the I^{2}C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a START or STOP condition. This is done so that noisy transmissions (usually an extra START or STOP condition) are aborted before they corrupt the device.

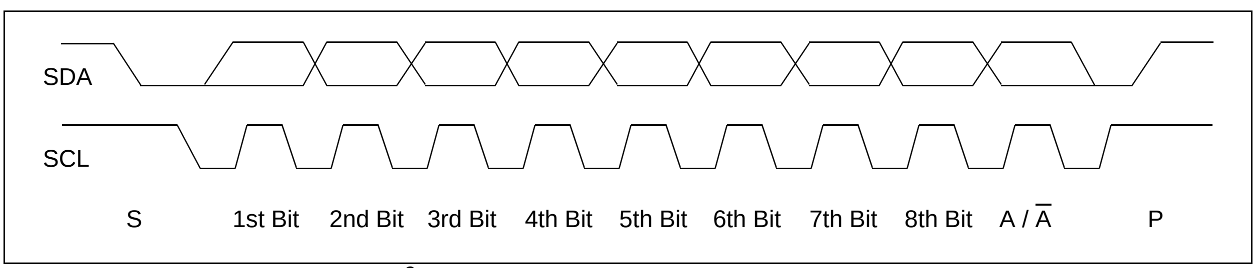

FIGURE 6-7: *Typical 8-Bit I^{2}C Waveform Format.*

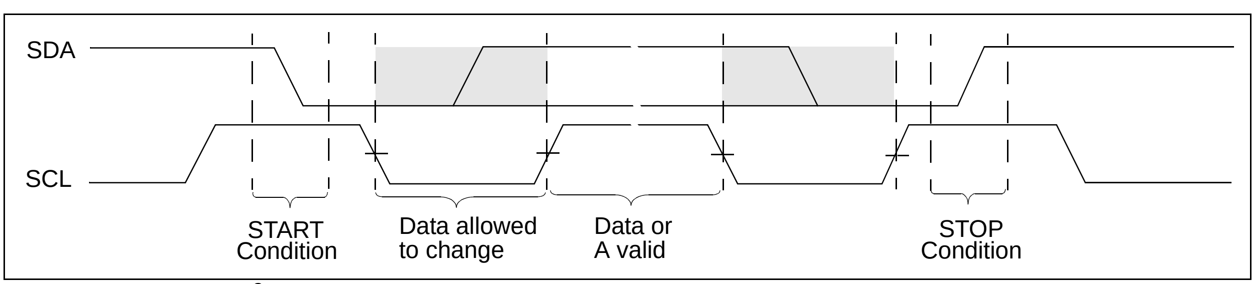

FIGURE 6-8: *I^{2}C Data States and Bit Sequence.*

6.2.4 ADDRESSING

The address byte is the first byte received following the START condition from the master device. The address contains four (or more) fixed bits and (up to) three user defined hardware address bits (pins A2, A1, and A0). These 7-bits address the desired I^{2}C device. The A7:A4 address bits are fixed to "`0101`" and the device appends the value of following three address pins (A2, A1, A0). Address pins that are not present on the device are pulled up (a bit value of '`1`').

Since there are up to three adress bits controlled by hardware pins, there may be up to eight MCP4XXX devices on the same I^{2}C bus.

Figure 6-9 shows the slave address byte format, which contains the seven address bits. There is also a read/write bit. Table 6-2 shows the fixed address for device.

Hardware Address Pins

The hardware address bits (A2, A1, and A0) correspond to the logic level on the associated address pins. This allows up to eight devices on the bus.

These pins have a weak pull-up enabled when the $V_{DD} < V_{BOR}$. The weak pull-up utilizes the "smart" pull-up technology and exhibits the same characteristics as the High-voltage tolerant I/O structure.

The state of the A0 address pin is latch on POR/BOR. This is required since High Voltage commands force this pin (HVC/A0) to the V_{IHH} level.

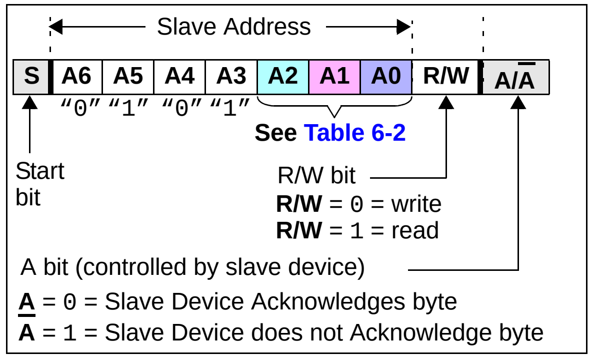

FIGURE 6-9: Slave Address Bits in the I^{2}C Control Byte.

TABLE 6-2: DEVICE SLAVE ADDRESSES

Device	Address	Comment
MCP45X1	'`0101 11`'b + A0	Supports up to 2 devices. **Note 1**
MCP45X2	'`0101 1`'b + A1:A0	Supports up to 4 devices. **Note 1**
MCP46X1	'`0101`'b + A2:A1:A0	Supports up to 8 devices. **Note 1**
MCP46X2	'`0101 1`'b + A1:A0	Supports up to 4 devices. **Note 1**

Note 1: A0 is used for High-Voltage commands and the value is latched at POR.

6.2.5 SLOPE CONTROL

The MCP45XX/46XX implements slope control on the SDA output.

As the device transitions from HS mode to FS mode, the slope control parmameter will change from the HS specification to the FS specification.

For Fast (FS) and High-Speed (HS) modes, the device has a spike suppression and a Schmidt trigger at SDA and SCL inputs.

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6.2.6 HS MODE

The I²C specification requires that a high-speed mode device must be ‘activated’ to operate in high-speed (3.4 Mbit/s) mode. This is done by the Master sending a special address byte following the START bit. This byte is referred to as the high-speed Master Mode Code (HSMMC).

The MCP45XX/46XX device does not acknowledge this byte. However, upon receiving this command, the device switches to HS mode. The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next STOP condition.

The master code is sent as follows:

1. START condition (S)
2. High-Speed Master Mode Code (`0000 1XXX`), The `XXX` bits are unique to the high-speed (HS) mode Master.
3. No Acknowledge ($\overline{A}$)

After switching to the High-Speed mode, the next transferred byte is the I²C control byte, which specifies the device to communicate with, and any number of data bytes plus acknowledgements. The Master Device can then either issue a Repeated Start bit to address a different device (at High-Speed) or a Stop bit to return to Fast/Standard bus speed. After the Stop bit, any other Master Device (in a Multi-Master system) can arbitrate for the I²C bus.

See Figure 6-10 for illustration of HS mode command sequence.

For more information on the HS mode, or other I²C modes, please refer to the Phillips I²C specification.

6.2.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

6.2.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.

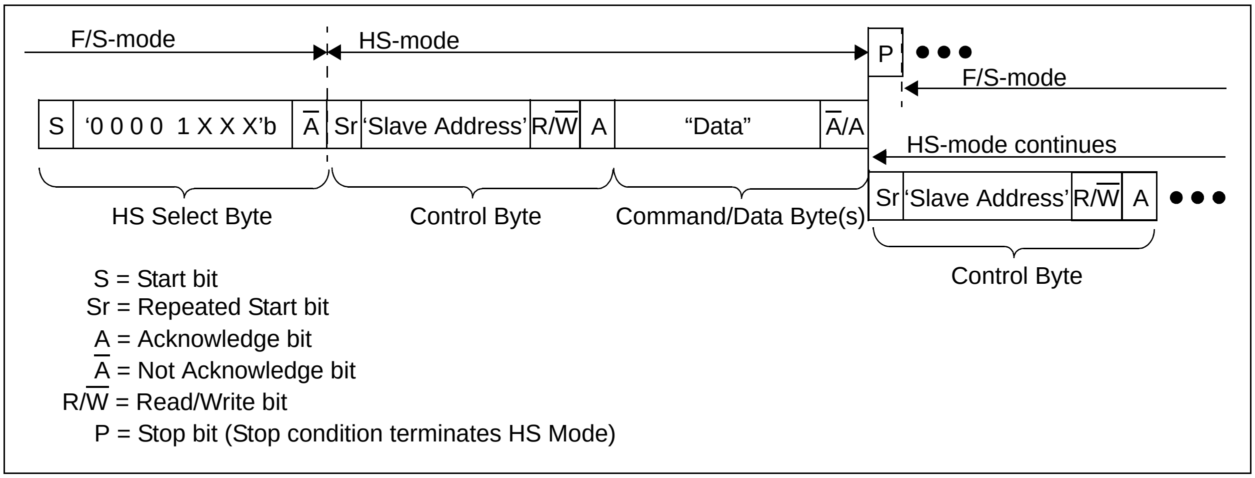

FIGURE 6-10: *HS Mode Sequence.*

6.2.7 GENERAL CALL

The General Call is a method that the “Master” device can communicate with all other “Slave” devices. In a Multi-Master application, the other Master devices are operating in Slave mode. The General Call address has two documented formats. These are shown in Figure 6-11. We have added a MCP45XX/46XX format in this figure as well.

This will allow customers to have multiple I^{2}C Digital Potentiometers on the bus and have them operate in a synchronous fashion (analogous to the DAC Sync pin functionality). If these MCP45XX/46XX 7-bit commands conflict with other I^{2}C devices on the bus, then the customer will need two I^{2}C busses and ensure that the devices are on the correct bus for their desired application functionality.

Dual Pot devices can not update both Pot0 and Pot1 from a single command. To address this, there are General Call commands for the Wiper 0, Wiper 1, and the TCON registers.

Table 6-3 shows the General Call Commands. Three commands are specified by the I^{2}C specification and are not applicable to the MCP45XX/46XX (so command is Not Acknowledged) The MCP45XX/46XX General Call Commands are Acknowledge. Any other command is Not Acknowledged.

Note:	Only one General Call command per issue of the General Call control byte. Any additional General Call commands are ignored and Not Acknowledged.

TABLE 6-3: GENERAL CALL COMMANDS

7-bit Command (1, 2, 3)	Comment
‘1000 00d’b	Write Next Byte (Third Byte) to Volatile Wiper 0 Register
‘1001 00d’b	Write Next Byte (Third Byte) to Volatile Wiper 1 Register
‘1100 00d’b	Write Next Byte (Third Byte) to TCON Register
‘1000 010’b or ‘1000 011’b	Increment Wiper 0 Register
‘1001 010’b or ‘1001 011’b	Increment Wiper 1 Register
‘1000 100’b or ‘1000 101’b	Decrement Wiper 0 Register
‘1001 100’b or ‘1001 101’b	Decrement Wiper 1 Register

Note 1: Any other code is Not Acknowledged. These codes may be used by other devices on the I^{2}C bus.

2: The 7-bit command always appends a “0” to form 8-bits. .

3: “d” is the D8 bit for the 9-bit write value.

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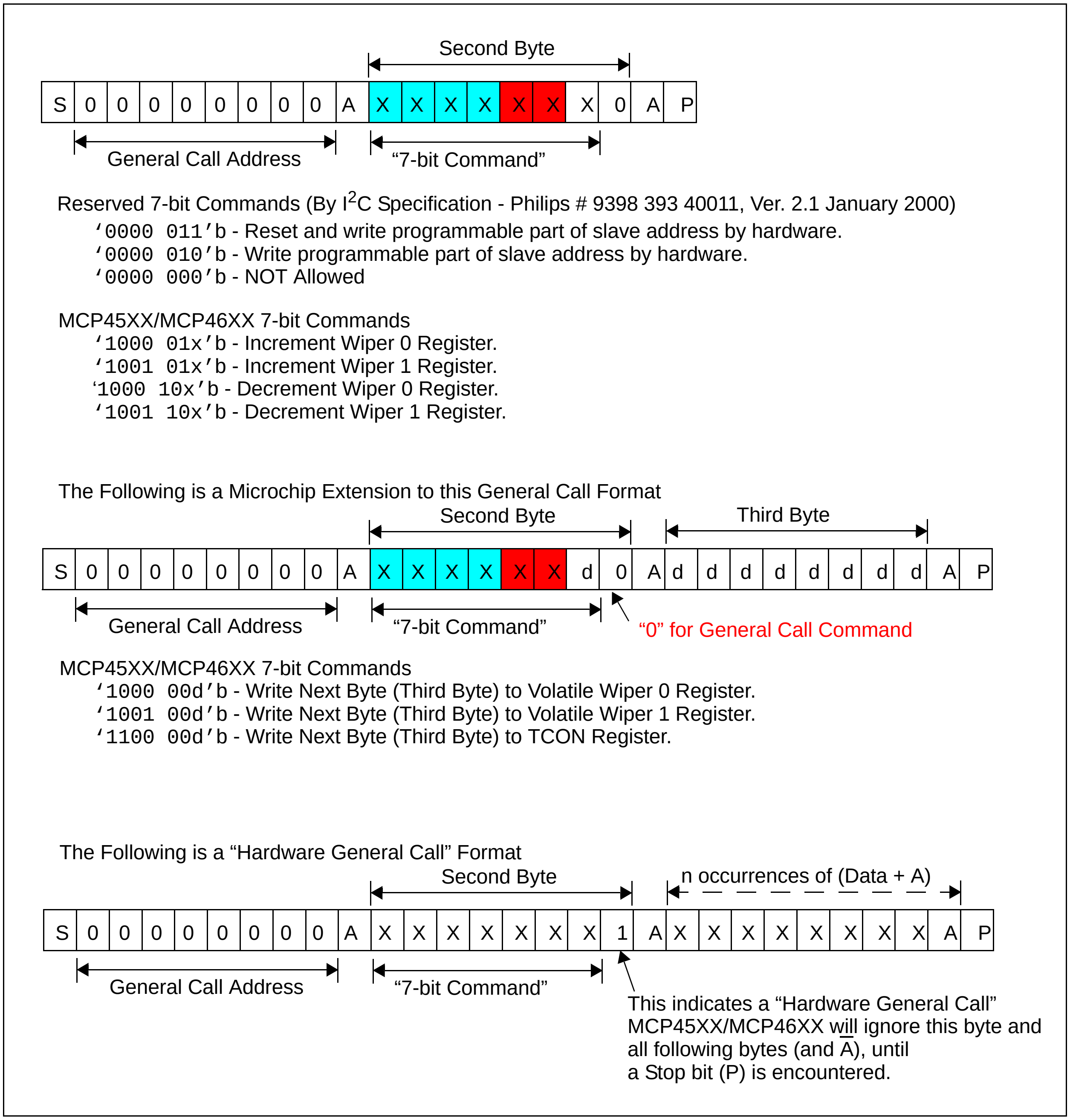

FIGURE 6-11: *General Call Formats.*

NOTES:

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7.0 DEVICE COMMANDS

The MCP4XXX's I²C command formats are specified in this section. The I²C protocol does not specify how commands are formatted.

The MCP4XXX supports four basic commands. Depending on the location accessed determines the commands that are supported.

For the Volatile Wiper Registers, these commands are:

- Write Data
- Read Data
- Increment Data
- Decrement Data

For the TCON Register, these commands are:

- Write Data
- Read Data

These commands have formats for both a single command or continuous commands. These commands are shown in Table 7-1.

Each command has two operational states. These operational states are referred to as:

- Normal Serial Commands
- High-Voltage Serial Commands

Note: High Voltage commands are supported for compatibility with Non-Volatile devices in the family.

TABLE 7-1: I²C COMMANDS

Command		# of Bit Clocks (1)	Operates on Volatile/ Non-Volatile memory
Operation	**Mode**		
Write Data	Single	29	Both
	Continuous	18n + 11	Volatile Only
Read Data	Single	29	Both
	Random	48	Both
	Continuous	18n + 11	Both
Increment	Single	20	Volatile Only
	Continuous	9n + 11	Volatile Only
Decrement	Single	20	Volatile Only
	Continuous	9n + 11	Volatile Only

Note 1: "n" indicates the number of times the command operation is to be repeated.

Normal serial commands are those where the HVC pin is driven to V_{IH} or V_{IL}. With High-Voltage Serial Commands, the HVC pin is driven to V_{IHH}. In each mode, there are four possible commands.

Table 7-2 shows the supported commands for each memory location.

Table 7-3 shows an overview of all the device commands and their interaction with other device features.

7.1 Command Byte

The MCP4XXX's Command Byte has three fields: the Address, the Command Operation, and 2 Data bits, see Figure 7-1. Currently only one of the data bits is defined (D8).

The device memory is accessed when the Master sends a proper Command Byte to select the desired operation. The memory location getting accessed is contained in the Command Byte's AD3:AD0 bits. The action desired is contained in the Command Byte's C1:C0 bits, see Table 7-1. C1:C0 determines if the desired memory location will be read, written, Incremented (wiper setting +1) or Decremented (wiper setting -1). The Increment and Decrement commands are only valid on the volatile wiper registers.

If the Address bits and Command bits are not a valid combination, then the MCP4XXX will generate a Not Acknowledge pulse to indicate the invalid combination. The I²C Master device must then force a Start Condition to reset the MCP4XXX's ²C module.

D9 and D8 are the most significant bits for the digital potentiometer's wiper setting. The 8-bit devices utilize D8 as their MSb while the 7-bit devices utilize D7 (from the data byte) as it's MSb.

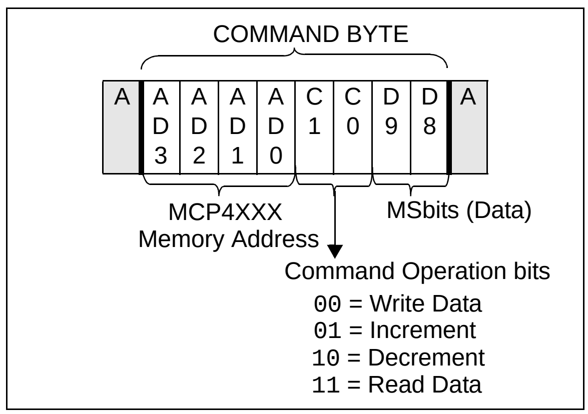

FIGURE 7-1: *Command Byte Format.*

TABLE 7-2: MEMORY MAP AND THE SUPPORTED COMMANDS

Address		Command Operation	Data (10-bits) (1)	Comment
Value	**Function**			
00h	Volatile Wiper 0	Write Data	nn nnnn nnnn	
		Read Data (3)	nn nnnn nnnn	
		Increment Wiper	—	
		Decrement Wiper	—	
01h	Volatile Wiper 1	Write Data	nn nnnn nnnn	
		Read Data (3)	nn nnnn nnnn	
		Increment Wiper	—	
		Decrement Wiper	—	
02h	Reserved	—	—	
03h	Reserved	—	—	
04h (2)	Volatile TCON Register	Write Data	nn nnnn nnnn	
		Read Data (3)	nn nnnn nnnn	
05h (2)	Reserved	Read Data (3)	nn nnnn nnnn	Maps to Non-Volitile MCP45XX/46XX device's STATUS Register
06h - 0Fh (2)	Reserved	—	—	

Note 1: The Data Memory is only 9-bits wide, so the MSb is ignored by the device.
2: Increment or Decrement commands are invalid for these addresses.
3: I^2C read operation will read 2 bytes, of which the 10-bits of data are contained within.

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7.2 Data Byte

Only the Read Command and the Write Command have Data Byte(s).

The Write command concatenates the 8-bits of the Data Byte with the one data bit (D8) contained in the Command Byte to form 9-bits of data (D8:D0). The Command Byte format supports up to 9-bits of data so that the 8-bit resistor network can be set to Full-Scale (100h or greater). This allows wiper connections to Terminal A and to Terminal B. The D9 bit is currently unused.

7.3 Error Condition

If the four address bits received (AD3:AD0) and the two command bits received (C1:C0) are a valid combination, the MCP4XXX will Acknowledge the I^2C bus.

If the address bits and command bits are an invalid combination, then the MCP4XXX will Not Acknowledge the I^2C bus.

Once an error condition has occurred, any following commands are ignored until the I^2C bus is reset with a Start Condition.

7.3.1 ABORTING A TRANSMISSION

A Restart or Stop condition in the expected data bit position will abort the current command sequence and

TABLE 7-3: COMMANDS

Command Name	# of Bits	High Voltage (V_{IHH}) on HVC pin?
Write Data	29	—
Read Data	29	—
Increment Wiper	20	—
Decrement Wiper	20	—
High Voltage **Write Data**	29	Yes
High Voltage **Read Data**	29	Yes
High Voltage **Increment Wiper**	20	Yes
High Voltage **Decrement Wiper**	20	Yes

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7.4 Write Data Normal and High Voltage

The Write Command can be issued to both the Volatile and Non-Volatile memory locations. The format of the command, see Figure 7-2, includes the I^2C Control Byte, an A bit, the MCP4XXX Command Byte, an A bit, the MCP4XXX Data Byte, an A bit, and a Stop (or Restart) condition. The MCP4XXX generates the A / $\overline{A}$ bits.

A Write command to a Volatile memory location changes that location after a properly formatted Write Command and the A / $\overline{A}$ clock have been received.

7.4.1 SINGLE WRITE TO VOLATILE MEMORY

For volatile memory locations, data is written to the MCP4XXX after every byte transfer (during the Acknowledge). If a Stop or Restart condition is generated during a data transfer (before the A), the data will not be written to the MCP4XXX. After the A bit, the master can initiate the next sequence with a Stop or Restart condition.

Refer to Figure 7-2 for the byte write sequence.

7.4.2 CONTINUOUS WRITES TO VOLATILE MEMORY

A continuous write mode of operation is possible when writing to the volatile memory registers (address 00h, 01h, and 04h). This continuous write mode allows writes without a Stop or Restart condition or repeated transmissions of the I^2C Control Byte. Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address. The sequence ends with the master sending a STOP or RESTART condition.

7.4.3 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage operational state. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

The HVC pin has an internal resistor connection to the MCP45XX/46XXs internal V_{DD} signal.

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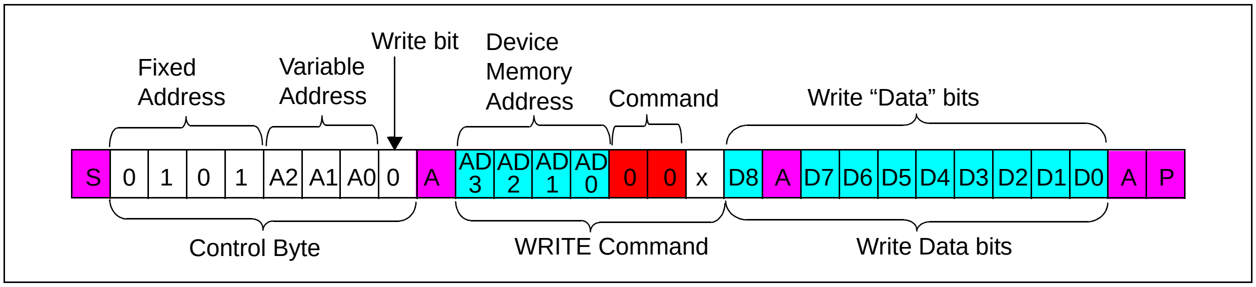
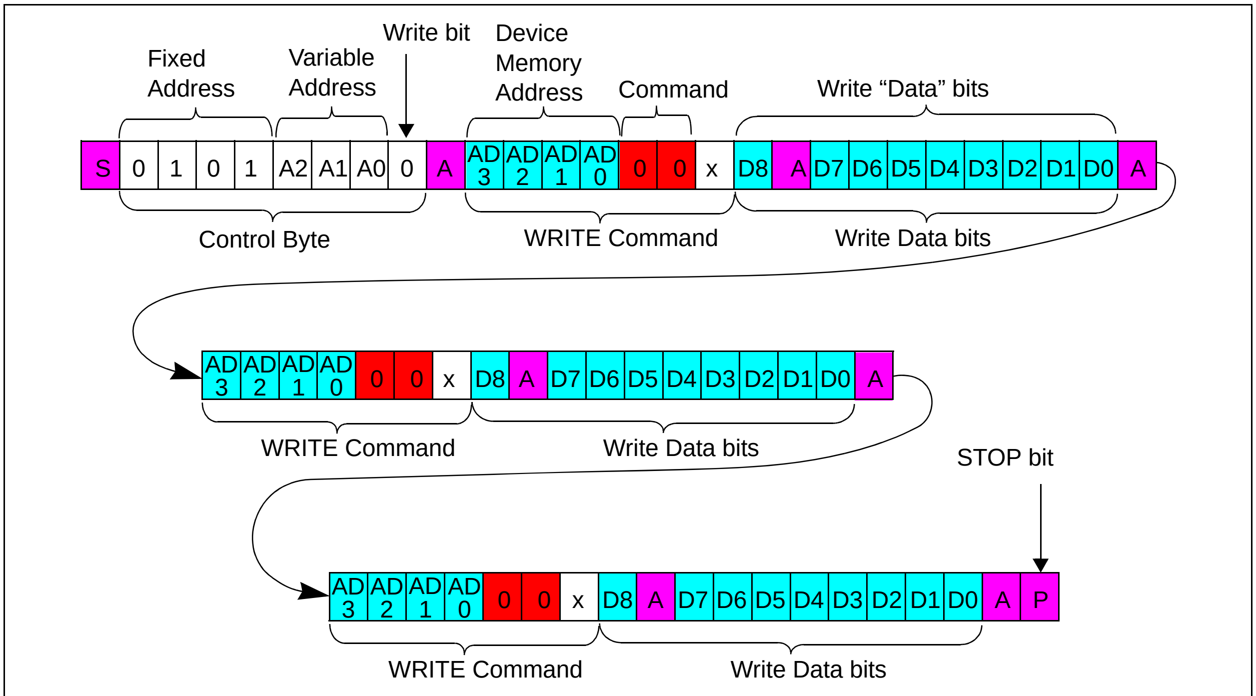


FIGURE 7-2: *I^2C Write Sequence.*



Note: Only functions when writing the volatile wiper registers (AD3:AD0 = 00h, 01h, and 04h) or the TCON register

FIGURE 7-3: *I^2C Continuous Volatile Wiper Write.*

7.5 Read Data Normal and High Voltage

The Read Command can be issued to both the Volatile and Non-Volatile memory locations. The format of the command, see Figure 7-4, includes the Start condition, I^2C Control Byte (with R/W bit set to "0"), A bit, MCP4XXX Command Byte, A bit, followed by a Repeated Start bit, I^2C Control Byte (with R/W bit set to "1"), and the MCP4XXX transmitting the requested Data High Byte, and A bit, the Data Low Byte, the Master generating the $\overline{A}$, and Stop condition.

The I^2C Control Byte requires the R/W bit equal to a logic one (R/W = 1) to generate a read sequence. The memory location read will be the last address contained in a valid write MCP4XXX Command Byte or address 00h if no write operations have occurred since the device was reset (Power-on Reset or Brown-out Reset).

Read operations initially include the same address byte sequence as the write sequence (shown in Figure 6-9). This sequence is followed by another control byte (including the Start condition and Ackowledge) with the R/W bit equal to a logic one (R/W = 1) to indicate a read. The MCP4XXX will then transmit the data contained in the addressed register. This is followed by the master generating an A bit in preparation for more data, or an $\overline{A}$ bit followed by a Stop. The sequence is ended with the master generating a Stop or Restart condition.

The internal address pointer is maintained.

7.5.1 SINGLE READ

Figure 7-4 show the waveforms for a single read.

For ***single reads*** the master sends a STOP or RESTART condition after the data byte is sent from the slave.

7.5.1.1 Random Read

Figure 7-5 shows the sequence for a Random Reads.

Refer to Figure 7-5 for the random byte read sequence.

7.5.2 CONTINUOUS READS

Continuous reads allows the devices memory to be read quickly. Continuous reads are possible to all memory locations. If a non-volatile memory write cycle is occurring, then Read commands may only access the volatile memory locations.

Figure 7-6 shows the sequence for three continuous reads.

For ***continuous reads***, instead of transmitting a Stop or Restart condition after the data transfer, the master reads the next data byte. The sequence ends with the master Not Acknowledging and then sending a Stop or Restart.

7.5.3 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. High Voltage commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

The HVC pin has an internal resistor connection to the MCP4XXXs internal V_{DD} signal.

7.5.4 IGNORING AN I^2C TRANSMISSION AND "FALLING OFF" THE BUS

The MCP4XXX expects to receive entire, valid I^2C commands and will assume any command not defined as a valid command is due to a bus corruption and will enter a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and Control Byte are received.

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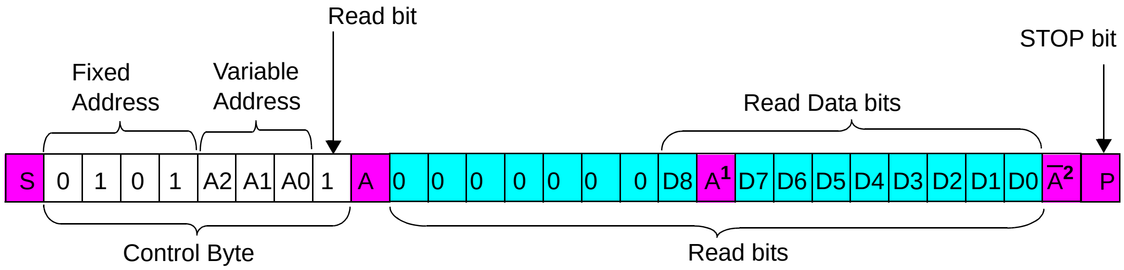


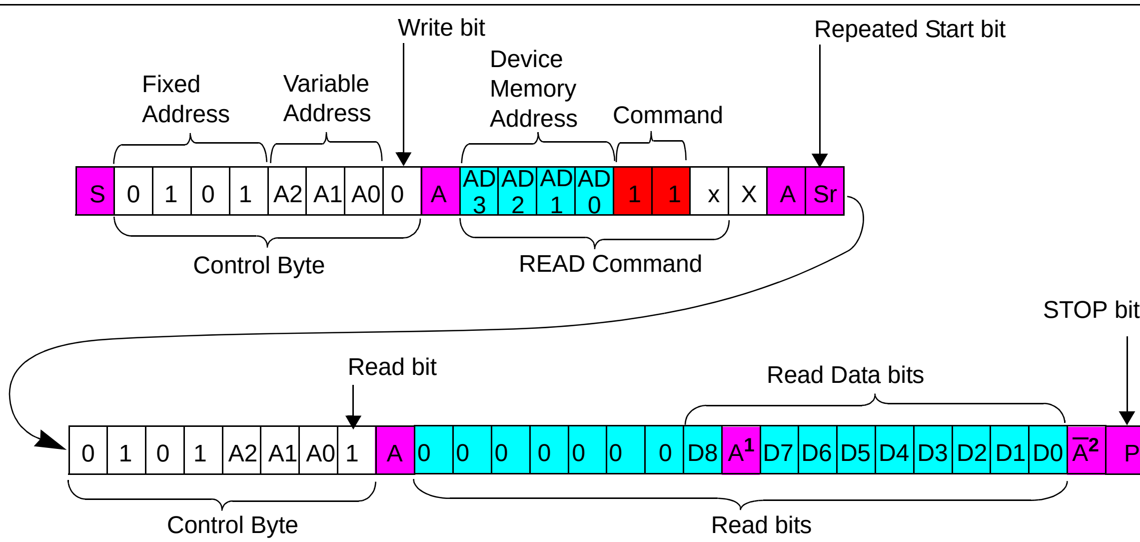
Note 1: Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP45XX/46XX will abort this transfer and release the bus.

2: The Master Device will Not Acknowledge, and the MCP45XX/46XX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

3: The MCP45xx/46xx retains the last "Device Memory Address" that it has received. This is the MCP45XX/46XX does not "corrupt" the "Device Memory Address" after Repeated Start or Stop conditions.

4: The Device Memory Address pointer defaults to 00h on POR and BOR conditions.

FIGURE 7-4: *I²C Read (Last Memory Address Accessed).*

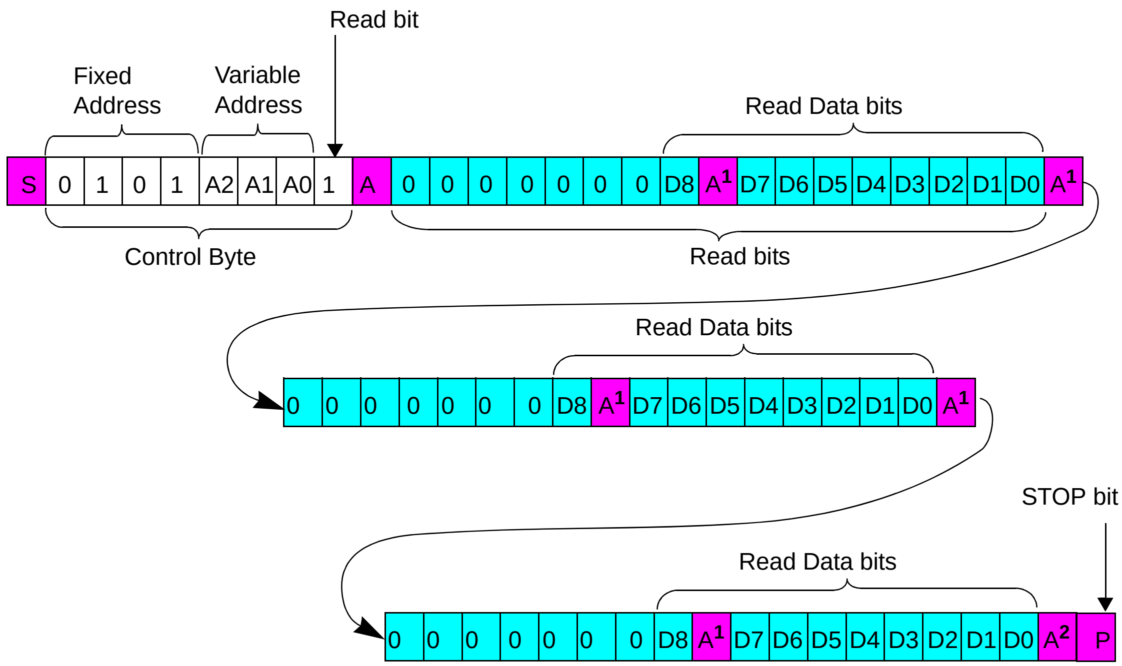


Note 1: Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP45XX/46XX will abort this transfer and release the bus.

2: The Master Device will Not Acknowledge, and the MCP45XX/46XX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

3: The MCP45XX/46XX retains the last "Device Memory Address" that it has received. This is the MCP45XX/46XX does not "corrupt" the "Device Memory Address" after Repeated Start or Stop conditions.

FIGURE 7-5: *I²C Random Read.*



Note 1: Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP45XX/46XX will abort this transfer and release the bus.

2: The Master Device will Not Acknowledge, and the MCP45XX/46XX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

FIGURE 7-6: *I²C Continuos Reads.*

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7.6 Increment Wiper Normal and High Voltage

The Increment Command provide a quick and easy method to modify the potentiometer's wiper by +1 with minimal overhead. The Increment Command will only function on the volatile wiper setting memory locations 00h and 01h.

> **Note:** Table 7-2 shows the valid addresses for the Increment Wiper command. Other addresses are invalid.

When executing an Increment Command, the volatile wiper setting will be altered from n to n+1 for each Increment Command received. The value will increment up to 100h max on 8-bit devices and 80h on 7-bit devices. If multiple Increment Commands are received after the value has reached 100h (or 80h), the value will not be incremented further. Table 7-4 shows the Increment Command versus the current volatile wiper value.

Refer to Figure 7-7 for the Increment Command sequence. The sequence is terminated by the Stop condition. So when executing a continuous command string, The Increment command can be followed by any other valid command. this means that writes do not need to be to the same volatile memory address.

> **Note:** The command sequence can go from an increment to any other valid command for the specified address.

The advantage of using an Increment Command instead of a read-modify-write series of commands is speed and simplicity. The wiper will transition after each Command Acknowledge when accessing the volatile wiper registers.

TABLE 7-4: INCREMENT OPERATION VS. VOLATILE WIPER VALUE

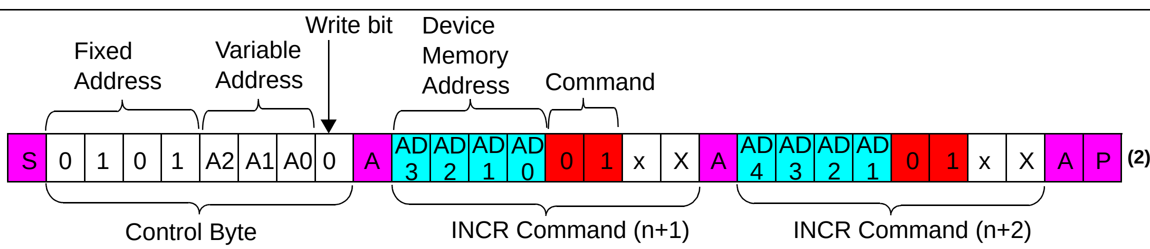
Current Wiper Setting		Wiper (W) Properties	Increment Command Operates?
7-bit Pot	8-bit Pot		
3FFh 081h	3FFh 101h	Reserved (Full-Scale (W = A))	No
080h	100h	Full-Scale (W = A)	No
07Fh 041h	0FFh 081	W = N	Yes
040h	080h	W = N (Mid-Scale)	
03Fh 001h	07Fh 001	W = N	
000h	000h	Zero Scale (W = B)	Yes

7.6.1 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. Signals > V_{IHH} (~8.5V) on the HVC/A0 pin puts MCP45XX/46XX devices into High Voltage mode.

> **Note:** There is a required delay after the HVC pin is driven to the V_{IHH} level to the 1st edge of the SCL pin.

The HVC pin has an internal resistor connection to the MCP45XX/46XXs internal V_{DD} signal.



Note 1: Increment Command (INCR) only functions when accessing the volatile wiper registers (AD3:AD0 = 0h and 1h).

2: This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (Increment, Read, or Write).

FIGURE 7-7: *I^2C Increment Command Sequence.*

7.7 Decrement Wiper Normal and High Voltage

The Decrement Command provide a quick and easy method to modify the potentiometer's wiper by -1 with minimal overhead. The Decrement Command will only function on the volatile wiper setting memory locations 00h and 01h.

> **Note:** Table 7-2 shows the valid addresses for the Decrement Wiper command. Other addresses are invalid.

When executing a Decrement Command, the volatile wiper setting will be altered from n to n-1 for each Decrement Command received. The value will decrement down to 000h min. If multiple Decrement Commands are received after the value has reached 000h, the value will not be decremented further. Table 7-5 shows the Increment Command versus the current volatile wiper value.

Refer to Figure 7-8 for the Decrement Command sequence. The sequence is terminated by the Stop condition. So when executing a continuous command string, The Increment command can be followed by any other valid command. this means that writes do not need to be to the same volatile memory address.

> **Note:** The command sequence can go from an increment to any other valid command for the specified address.

The advantage of using an Decrement Command instead of a read-modify-write series of commands is speed and simplicity. The wiper will transition after each Command Acknowledge when accessing the volatile wiper registers.

TABLE 7-5: DECREMENT OPERATION VS. VOLATILE WIPER VALUE

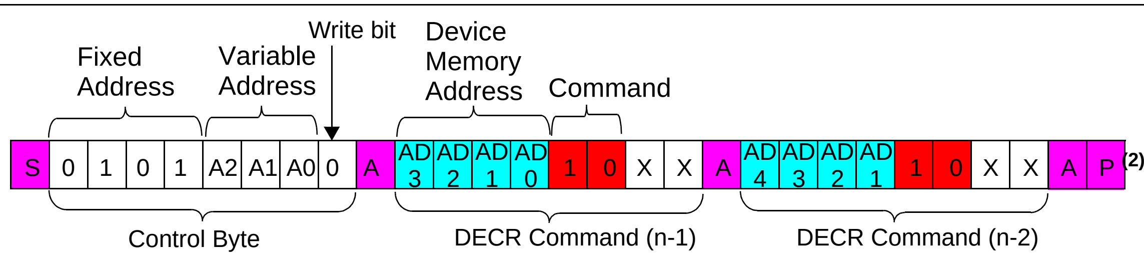
Current Wiper Setting		Wiper (W) Properties	Decrement Command Operates?
7-bit Pot	8-bit Pot		
3FFh 081h	3FFh 101h	Reserved (Full-Scale (W = A))	No
080h	100h	Full-Scale (W = A)	Yes
07Fh 041h	0FFh 081	W = N	
040h	080h	W = N (Mid-Scale)	Yes
03Fh 001h	07Fh 001	W = N	
000h	000h	Zero Scale (W = B)	No

7.7.1 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The High Voltage Command (HVC) signal is multiplexed with Address 0 (A0) and is used to indicate that the command, or sequence of commands, are in the High Voltage mode. Signals > V_{IHH} (~8.5V) on the HVC/A0 pin puts MCP45XX/46XX devices into High Voltage mode.

> **Note:** There is a required delay after the HVC pin is driven to the V_{IHH} level to the 1st edge of the SCL pin.

The HVC pin has an internal resistor connection to the MCP45XX/46XXs internal V_{DD} signal.



Note 1: Decrement Command (DECR) only functions when accessing the volatile wiper registers (AD3:AD0 = 0h and 1h).

2: This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (INCR, Read, or Write).

FIGURE 7-8: I^2C Decrement Command Sequence.

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8.0 APPLICATIONS EXAMPLES

Non-volatile digital potentiometers have a multitude of practical uses in modern electronic circuits. The most popular uses include precision calibration of set point thresholds, sensor trimming, LCD bias trimming, audio attenuation, adjustable power supplies, motor control overcurrent trip setting, adjustable gain amplifiers and offset trimming. The MCP453X/455X/463X/465X devices can be used to replace the common mechanical trim pot in applications where the operating and terminal voltages are within CMOS process limitations (V_{DD} = 2.7V to 5.5V).

8.1 Techniques to force the HVC pin to V_{IHH}

The circuit in Figure 8-1 shows a method using the TC1240A doubling charge pump. When the SHDN pin is high, the TC1240A is off, and the level on the HVC pin is controlled by the PIC® microcontrollers (MCUs) IO2 pin.

When the SHDN pin is low, the TC1240A is on and the V_{OUT} voltage is 2 * V_{DD}. The resistor R_1 allows the HVC pin to go higher than the voltage such that the PIC MCU's IO2 pin "clamps" at approximately VDD.

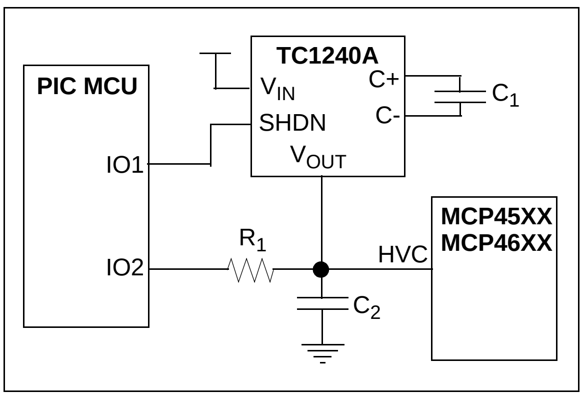

FIGURE 8-1: *Using the TC1240A to generate the V_{IHH} voltage.*

The circuit in Figure 8-2 shows the method used on the MCP402X Non-volatile Digital Potentiometer Evaluation Board (Part Number: MCP402XEV). This method requires that the system voltage be approximately 5V. This ensures that when the PIC10F206 enters a brown-out condition, there is an insufficient voltage level on the HVC pin to change the stored value of the wiper. The MCP402X Non-volatile Digital Potentiometer Evaluation Board User's Guide (DS51546) contains a complete schematic.

GP0 is a general purpose I/O pin, while GP2 can either be a general purpose I/O pin or it can output the internal clock.

For the serial commands, configure the GP2 pin as an input (high impedance). The output state of the GP0 pin will determine the voltage on the HVC pin (V_{IL} or V_{IH}).

For high-voltage serial commands, force the GP0 output pin to output a high level (V_{OH}) and configure the GP2 pin to output the internal clock. This will form a charge pump and increase the voltage on the HVC pin (when the system voltage is approximately 5V).

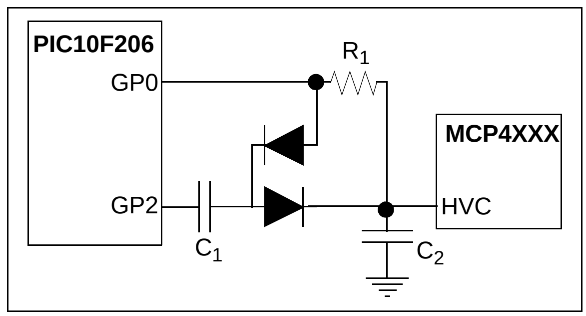

FIGURE 8-2: *MCP4XXX Non-Volatile Digital Potentiometer Evaluation Board (MCP402XEV) implementation to generate the V_{IHH} voltage.*

8.2 Using Shutdown

Figure 8-3 shows a possible application circuit where the independent terminals could be used. Disconnecting the wiper allows the transistor input to be taken to the Bias voltage level (disconnecting A and or B may be desired to reduce system current). Disconnecting Terminal A modifies the transistor input by the R_{BW} rheostat value to the Common B. Disconnecting Terminal B modifies the transistor input by the R_{AW} rheostat value to the Common A. The Common A and Common B connections could be connected to V_{DD} and V_{SS}.

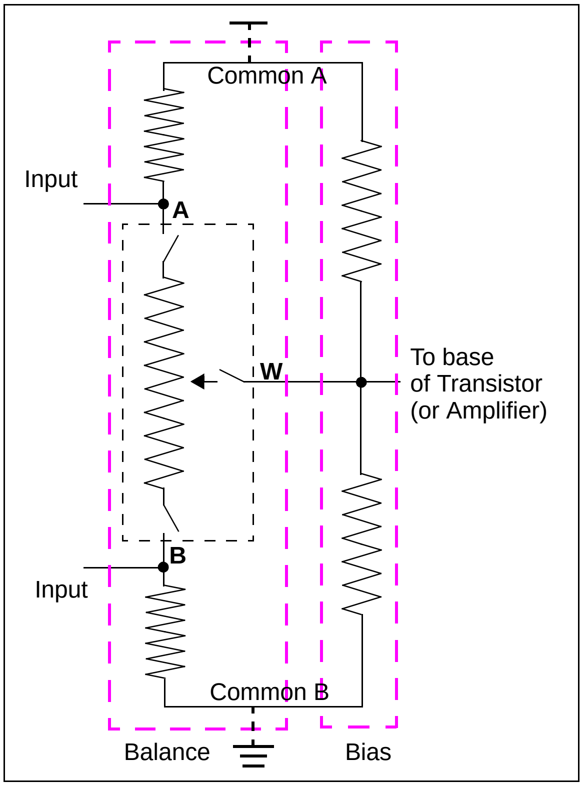

FIGURE 8-3: Example Application Circuit using Terminal Disconnects.

8.3 Software Reset Sequence

Note:	This technique is documented in AN1028.

At times it may become necessary to perform a Software Reset Sequence to ensure the MCP45XX/46XX device is in a correct and known I^2C Interface state. This technique only resets the I^2C state machine.

This is useful if the MCP45XX/46XX device powers up in an incorrect state (due to excessive bus noise, ...), or if the Master Device is reset during communication. Figure 8-4 shows the communication sequence to software reset the device.

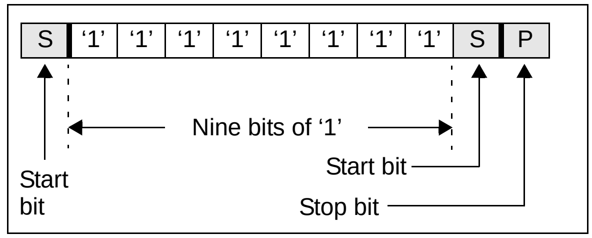

FIGURE 8-4: Software Reset Sequence Format.

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the Master Device. In this mode, the device is monitoring the data bus in Receive mode and can detect the Start bit forces an internal Reset.

The nine bits of ‘1’ are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP45XX/46XX is driving an A bit on the I^2C bus, or is in output mode (from a Read command) and is driving a data bit of ‘0’ onto the I^2C bus. In both of these cases, the previous Start bit could not be generated due to the MCP45XX/46XX holding the bus low. By sending out nine ‘1’ bits, it is ensured that the device will see a $\overline{A}$ bit (the Master Device does not drive the I^2C bus low to acknowledge the data sent by the MCP45XX/46XX), which also forces the MCP45XX/46XX to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the Master Device was reset while sending a Write command to the MCP45XX/46XX, AND then as the Master Device returns to normal operation and issues a Start condition while the MCP45XX/46XX is issuing an Acknowledge. In this case, if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP45XX/46XX could initiate a write cycle.

Note:	The potential for this erroneous write ONLY occurs if the Master Device is reset while sending a Write command to the MCP45XX/46XX.

The Stop bit terminates the current I^2C bus activity. The MCP45XX/46XX wait to detect the next Start condition.

This sequence does not effect any other I^2C devices which may be on the bus, as they should disregard this as an invalid command.

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8.4 Using the General Call Command

The use of the General Call Address Increment, Decrement, or Write commands is analogous to the “Load” feature (LDAC pin) on some DACs (such as the MCP4921). This allows all the devices to “Update” the output level “at the same time”.

For some applications, the ability to update the wiper values “at the same time may be a requirement, since they delay from writing to one wiper value and then the next may cause application issues. A possible example would be a “tuned” circuit that uses several MCP45XX/46XX in rheostat configuration. As the system condition changes (temperature, load, ...) these devices need to be changed (incremented/decremented) to adjust for the system change. These changes will either be in the same direction or in opposite directions. With the Potentiometer device the customer can either select the PxB terminals (same direction) or the PxA terminal(s) (opposite direction).

Figure 8-6 shows that the update of six devices takes $6{*}T_{I2CDLY}$ time in “normal” operation, but only $1{*}T_{I2CDLY}$ time in “General Call” operation.

Note:	The application system may need to partition the I^2C bus into multiple busses to ensure that the MCP45XX/46XX General Call commands do not conflict with the General Call commands that the other I^2C devices may have defined. Also if only a portion of the MCP45XX/46XX devices are to require this synchronous operation, then the devices that should not receive these commands should be on the second I^2C bus.

Figure 8-5 shows two I^2C bus configurations. In many cases, the single I^2C bus configuration will be adequate. For applications that do not want all the MCP45XX/46XX devices to do General Call support or have a conflict with General Call commands, the multiple I^2C bus configuration would be used.

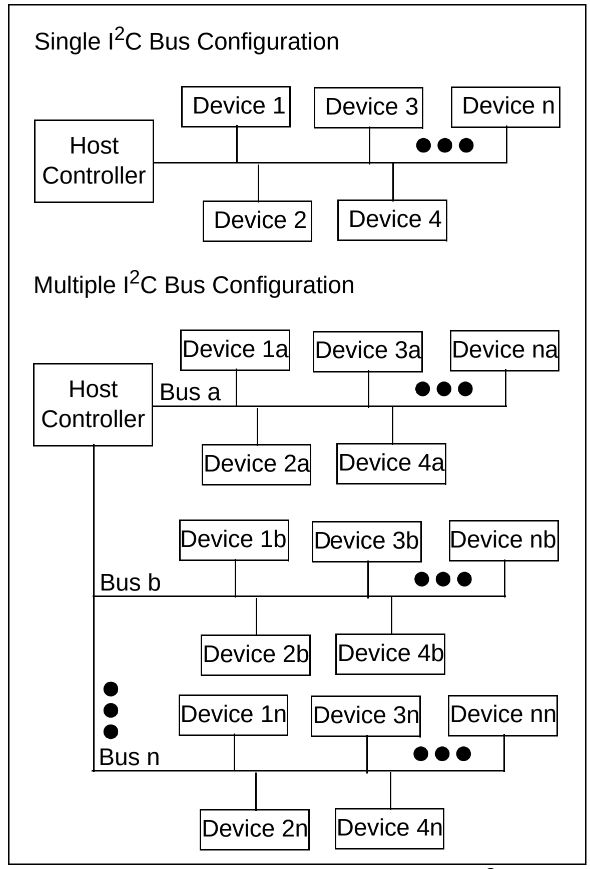

FIGURE 8-5: *Typical Application I^2C Bus Configurations.*

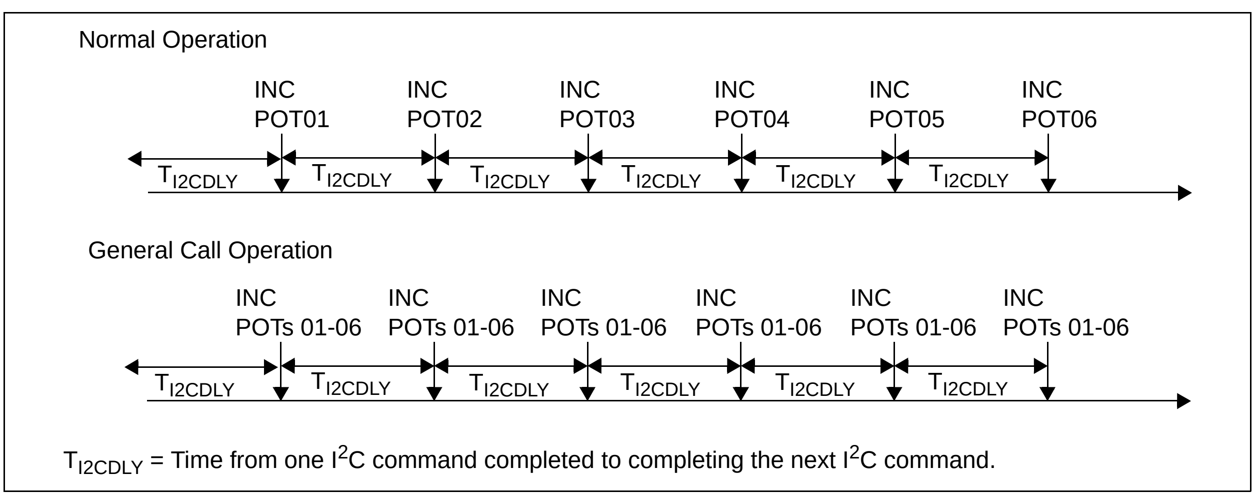

FIGURE 8-6: *Example Comparison of “Normal Operation” vs. “General Call Operation” wiper Updates.*

8.5 Design Considerations

In the design of a system with the MCP4XXX devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

8.5.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-7 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_{DD}) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

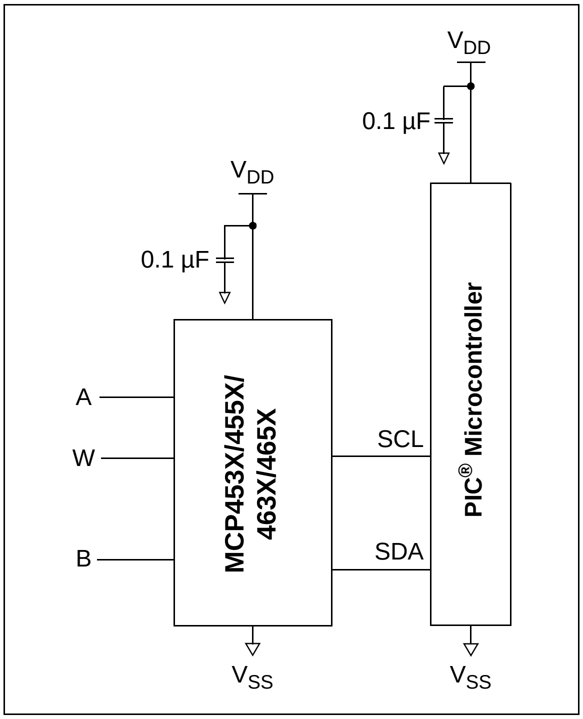

FIGURE 8-7: *Typical Microcontroller Connections.*

8.5.2 LAYOUT CONSIDERATIONS

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP4XXX's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

If low noise is desired, breadboards and wire-wrapped boards are not recommended.

8.5.3 RESISTOR TEMPCO

Characterization curves of the resistor temperature coefficient (Tempco) are shown in Figure 2-12, Figure 2-25, Figure 2-38, and Figure 2-51.

These curves show that the resistor network is designed to correct for the change in resistance as temperature increases. This technique reduces the end to end change is R_{AB} resistance.

8.5.4 HIGH VOLTAGE TOLERANT PINS

High Voltage support (V_{IHH}) on the Serial Interface pins is for compatibility with the non-volatile devices..

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9.0 DEVICE OPTIONS

Additional, custom devices are available. These devices have weak pull-up resistors on the SDA and SCL pins. This is useful for applications where the wiper value is programmed durning manufacture and not modified by the system during normal operation.

Please contact your local sales office for current information and minimum volumn requirements.

9.1 Custom Options

The custom device will have a “P” (for Pull-up) after the resistance version in the Product Identification System. These device will not be available through Microchip’s online Microchip Direct nor Microchip’s Sample systems.

Example part number:
MCP4631-103**P**E/ST

NOTES:

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10.0 DEVELOPMENT SUPPORT

10.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP45XX/46XX devices. The currently available tools are shown in Table 10-1.

These boards may be purchased directly from the Microchip web site at www.microchip.com.

10.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 10-2 shows some of these documents.

TABLE 10-1: DEVELOPMENT TOOLS

Board Name	Part #	Supported Devices
MCP42XX PICTail Plus Daughter Board (2)	MCP42XXDM-PTPLS	MCP42XX
MCP4XXX Digital Potentiometer Daughter Board (1)	MCP4XXXDM-DB	MCP42XXX, MCP42XX, MCP46XX, MCP4021, and MCP4011
8-pin SOIC/MSOP/TSSOP/DIP Evaluation Board	SOIC8EV	Any 8-pin device in DIP, SOIC, MSOP, or TSSOP package
14-pin SOIC/MSOP/DIP Evaluation Board	SOIC14EV	Any 14-pin device in DIP, SOIC, or MSOP package

Note 1: Requires the use of a PICDEM Demo Board (see User’s Guide for details)

2: Requires the use of the PIC24 Explorer 16 Demo Board (see User’s Guide for details)

3: The desired MCP46XX device (in MSOP package) must be soldered onto the extra board.

TABLE 10-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1080	Understanding Digital Potentiometers Resistor Variations	DS01080
AN737	Using Digital Potentiometers to Design Low Pass Adjustable Filters	DS00737
AN692	Using a Digital Potentiometer to Optimize a Precision Single Supply Photo Detect	DS00692
AN691	Optimizing the Digital Potentiometer in Precision Circuits	DS00691
AN219	Comparing Digital Potentiometers to Mechanical Potentiometers	DS00219
—	Digital Potentiometer Design Guide	DS22017
—	Signal Chain Design Guide	DS21825

NOTES:

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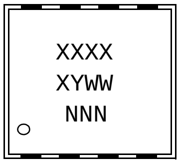
11.0 PACKAGING INFORMATION

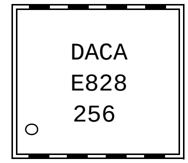
11.1 Package Marking Information

8-Lead DFN (3x3)

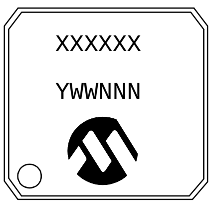


Part Number	Code	Part Number	Code
MCP4531-502E/MF	DACA	MCP4532-502E/MF	DACE
MCP4531-103E/MF	DACB	MCP4532-103E/MF	DACF
MCP4531-104E/MF	DACD	MCP4532-104E/MF	DACH
MCP4531-503E/MF	DACC	MCP4532-503E/MF	DACG
MCP4551-502E/MF	DACT	MCP4552-502E/MF	DACX
MCP4551-103E/MF	DACU	MCP4552-103E/MF	DACY
MCP4551-104E/MF	DACW	MCP4552-104E/MF	DADA
MCP4551-503E/MF	DACV	MCP4552-503E/MF	DACZ

Example:

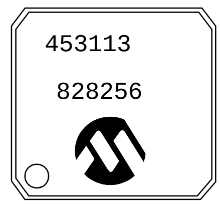


8-Lead MSOP



Part Number	Code	Part Number	Code
MCP4531-103E/MS	453113	MCP4532-103E/MS	453213
MCP4531-104E/MS	453114	MCP4532-104E/MS	453214
MCP4531-502E/MS	453152	MCP4532-502E/MS	453252
MCP4531-503E/MS	453153	MCP4532-503E/MS	453253
MCP4551-103E/MS	455113	MCP4552-103E/MS	455213
MCP4551-104E/MS	455114	MCP4552-104E/MS	455214
MCP4551-502E/MS	455152	MCP4552-502E/MS	455252
MCP4551-503E/MS	455153	MCP4552-503E/MS	455253

Example



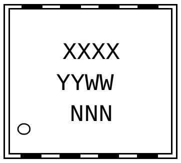
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
e3	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

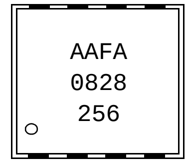
Package Marking Information (Continued)

10-Lead DFN (3x3)

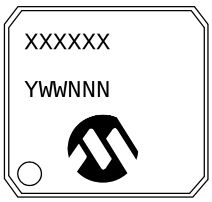


Part Number	Code	Part Number	Code
MCP4632-502E/MF	AABA	MCP4652-502E/MF	AAKA
MCP4632-103E/MF	AACA	MCP4652-103E/MF	AALA
MCP4632-104E/MF	AAEA	MCP4652-104E/MF	AAPA
MCP4632-503E/MF	AADA	MCP4652-503E/MF	AAMA

Example:

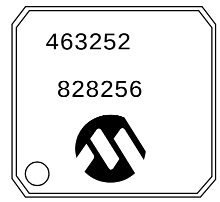


10-Lead MSOP

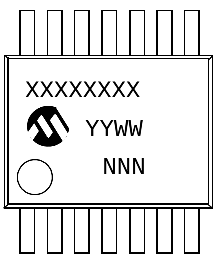


Part Number	Code	Part Number	Code
MCP4632-502E/UN	463252	MCP4652-502E/UN	465252
MCP4632-103E/UN	463213	MCP4652-103E/UN	465213
MCP4632-104E/UN	463214	MCP4652-104E/UN	465214
MCP4632-503E/UN	463253	MCP4652-503E/UN	465253

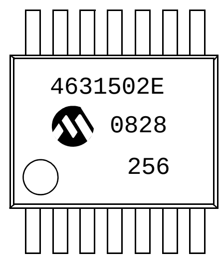
Example



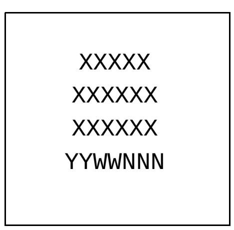
14-Lead TSSOP **(MCP4631, MCP4651)**



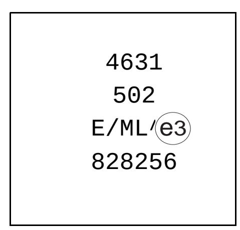
Example



16-Lead QFN **(MCP4631, MCP4651)**



Example



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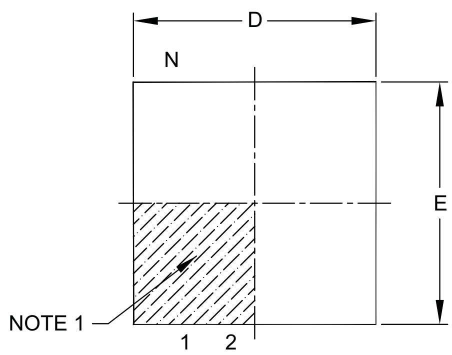
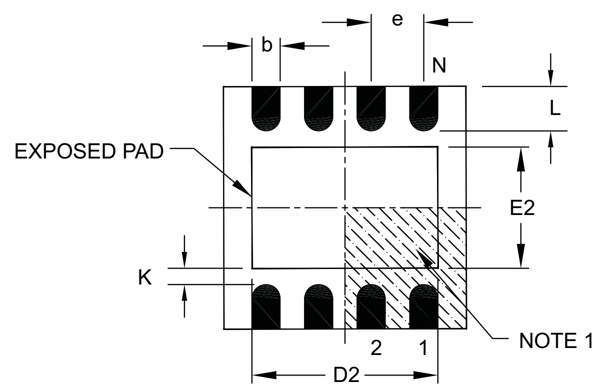
8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

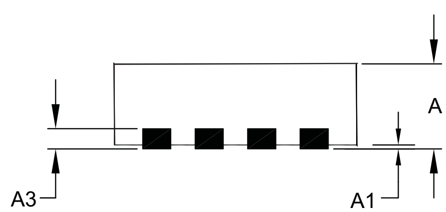
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

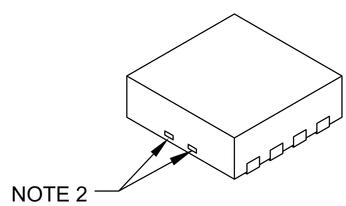


TOP VIEW



BOTTOM VIEW





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	0.00	–	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	0.00	–	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

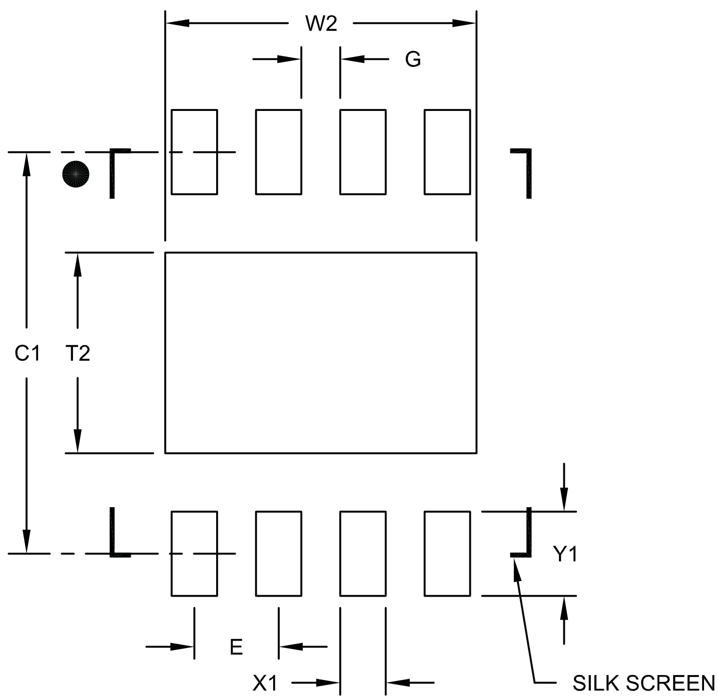
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B

8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062A

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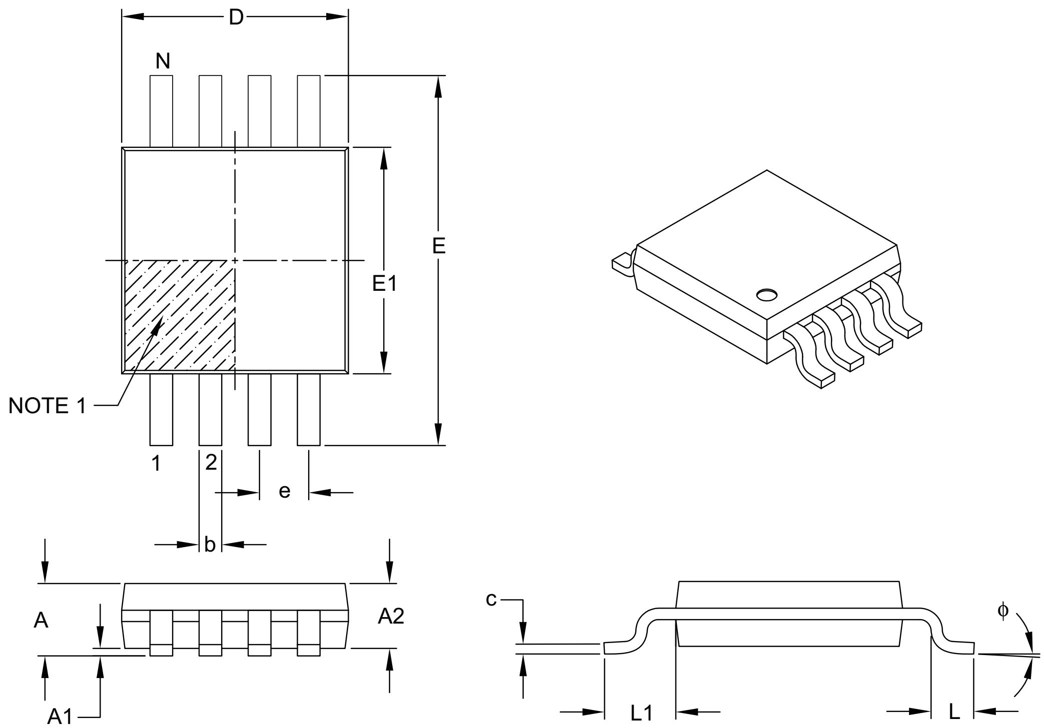
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

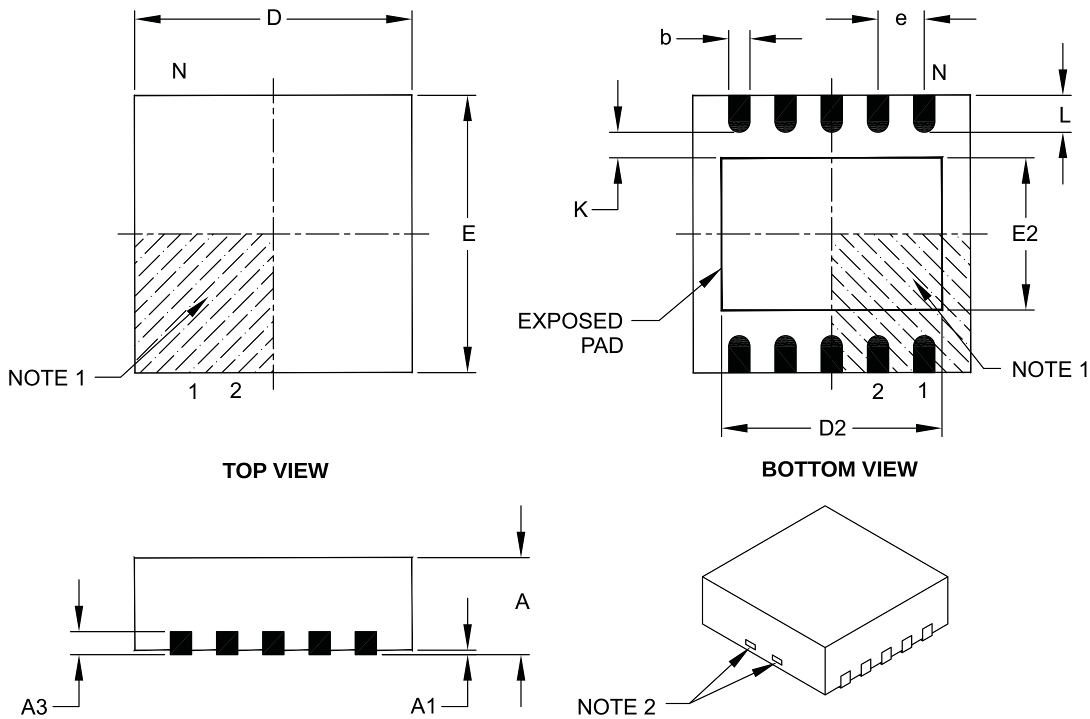
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.35	2.48
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.58	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-063B

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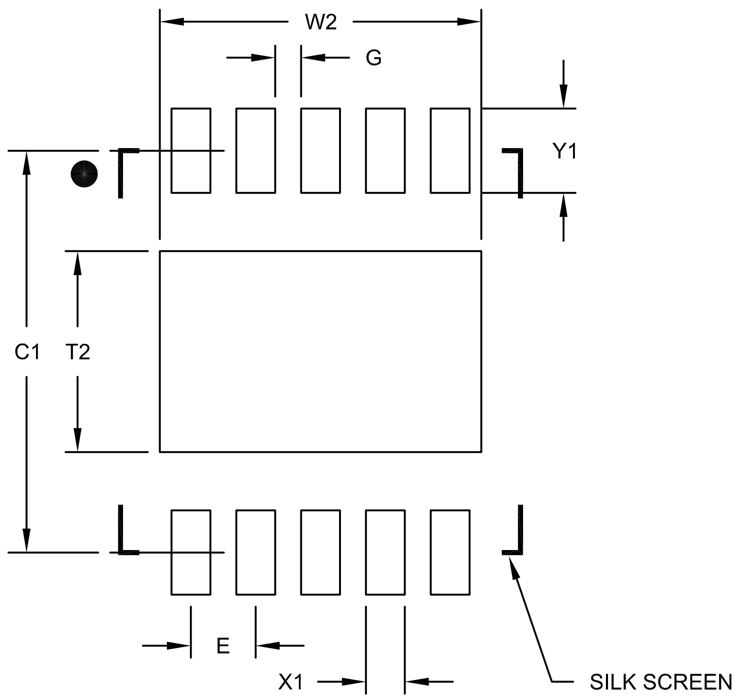
10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063A

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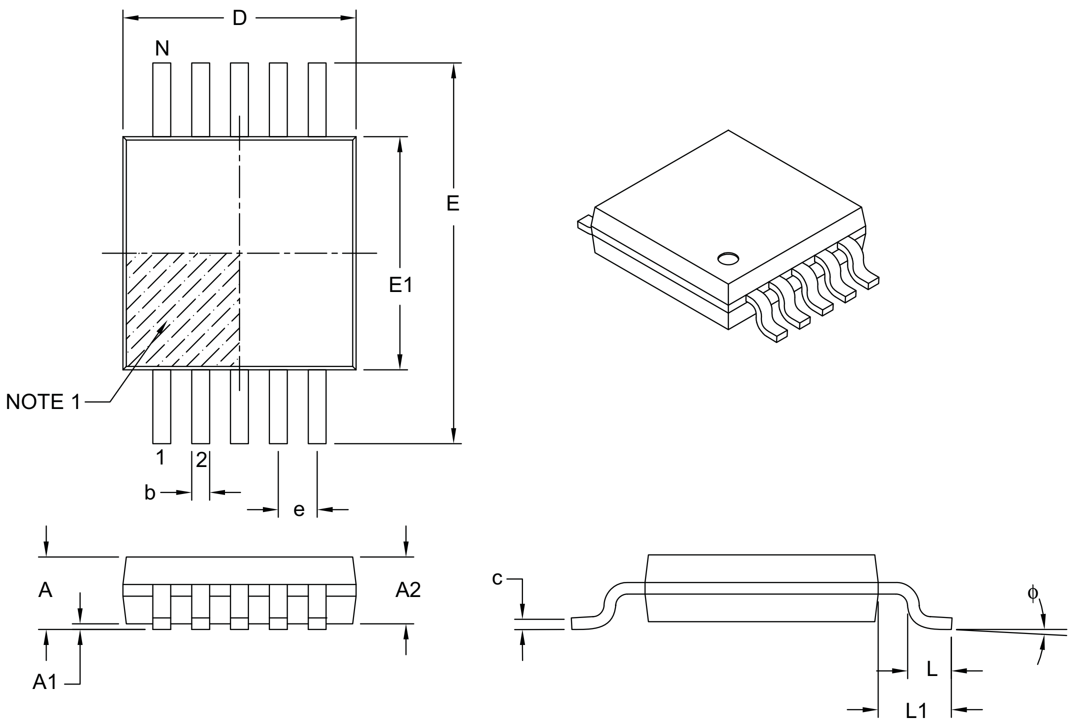
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.15	–	0.33

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

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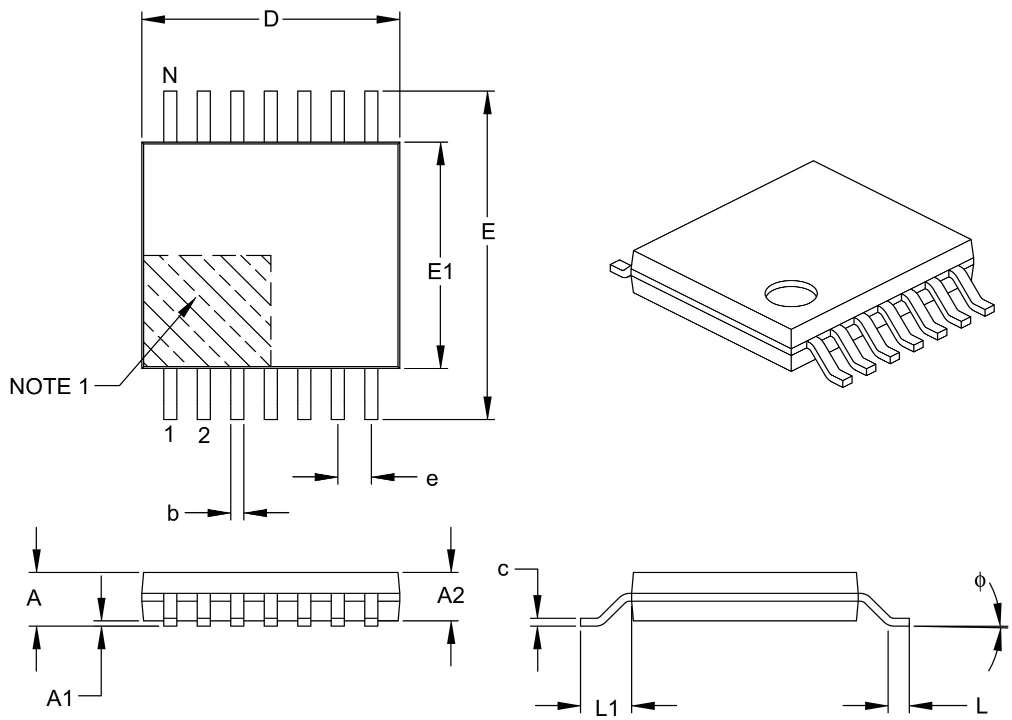
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

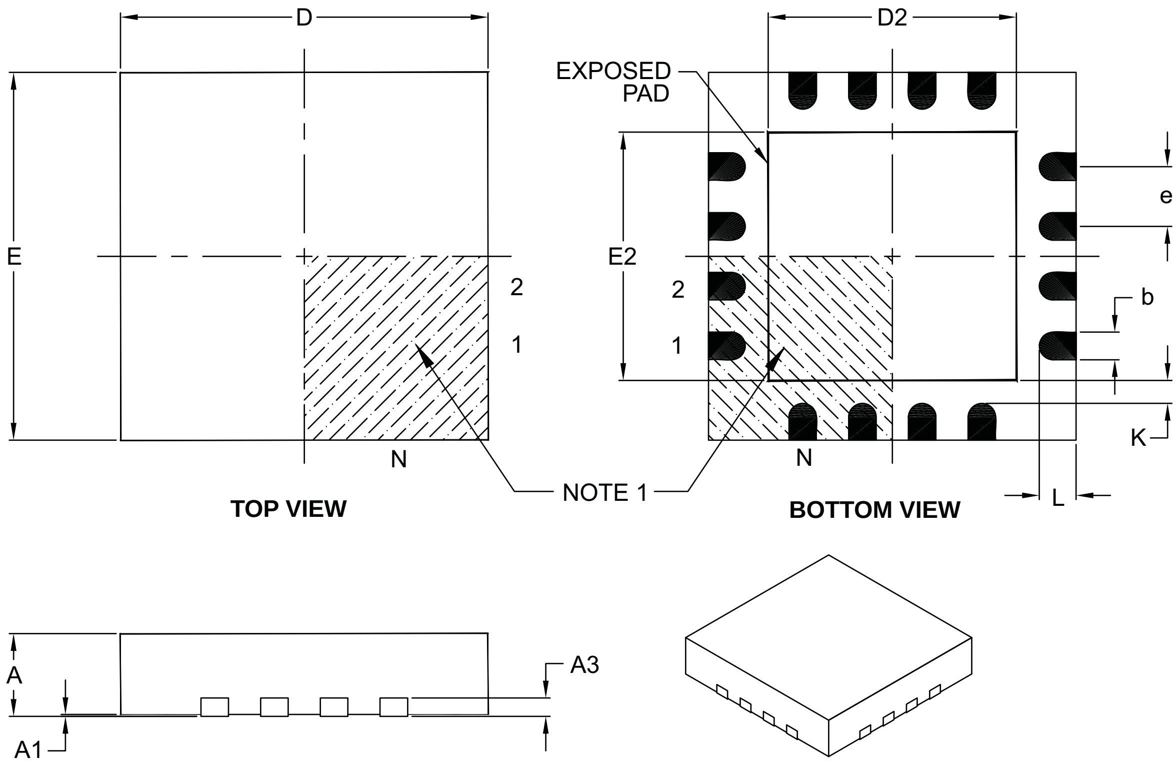
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

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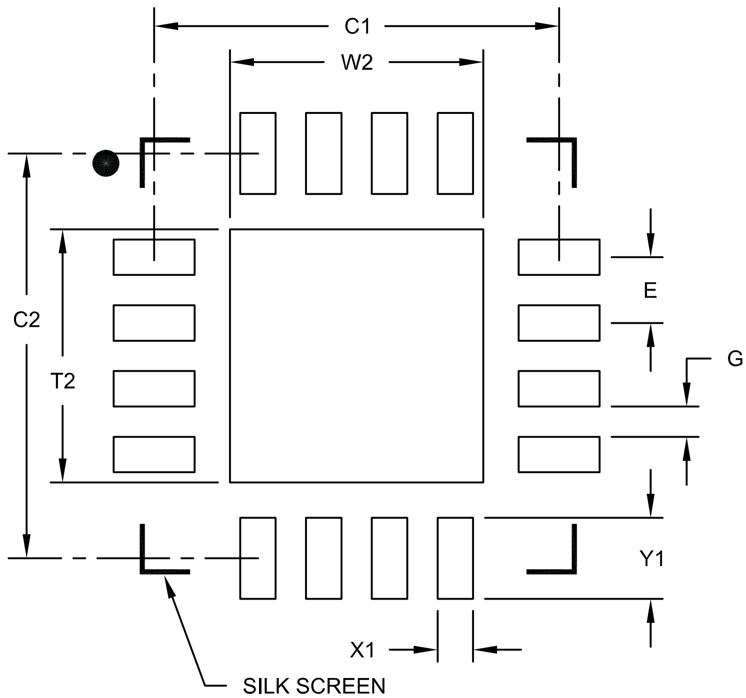
16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.35
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2127A

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (November 2008)

- Original Release of this Document.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XXX	X	/XX
Device	Resistance Version	Temperature Range	Package

Device:	MCP4531:	Single Non-Volatile 7-bit Potentiometer
	MCP4531T:	Single Non-Volatile 7-bit Potentiometer (Tape and Reel)
	MCP4532:	Single Non-Volatile 7-bit Rheostat
	MCP4532T:	Single Non-Volatile 7-bit Rheostat (Tape and Reel)
	MCP4551:	Single Non-Volatile 8-bit Potentiometer
	MCP4551T:	Single Non-Volatile 8-bit Potentiometer (Tape and Reel)
	MCP4552:	Single Non-Volatile8-bit Rheostat
	MCP4552T:	Single Non-Volatile 8-bit Rheostat (Tape and Reel)
	MCP4631:	Dual Non-Volatile 7-bit Potentiometer
	MCP4631T:	Dual Non-Volatile 7-bit Potentiometer (Tape and Reel)
	MCP4632:	Dual Non-Volatile 7-bit Rheostat
	MCP4632T:	Dual Non-Volatile 7-bit Rheostat (Tape and Reel)
	MCP4651:	Dual Non-Volatile 8-bit Potentiometer
	MCP4651T:	Dual Non-Volatile 8-bit Potentiometer (Tape and Reel)
	MCP4652:	Dual Non-Volatile8-bit Rheostat
	MCP4652T:	Dual Non-Volatile 8-bit Rheostat (Tape and Reel)
Resistance Version:	502 = 5 kΩ	
	103 = 10 kΩ	
	503 = 50 kΩ	
	104 = 100 kΩ	
Temperature Range:	E = -40°C to +125°C	
Package:	MF =	Plastic Dual Flat No-lead (3x3 DFN), 8/10-lead
	ML =	Plastic Quad Flat No-lead (QFN), 16-lead
	MS =	Plastic Micro Small Outline (MSOP), 8-lead
	ST =	Plastic Thin Shrink Small Outline (TSSOP), 14-lead
	UN =	Plastic Micro Small Outline (MSOP), 10-lead

Examples:

a) MCP4531-502E/XX: 5 kΩ, 8LD Device
b) MCP4531-103E/XX: 10 kΩ, 8-LD Device
c) MCP4531-503E/XX: 50 kΩ, 8LD Device
d) MCP4531-104E/XX: 100 kΩ, 8LD Device
e) MCP4531T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4532-502E/XX: 5 kΩ, 8LD Device
b) MCP4532-103E/XX: 10 kΩ, 8-LD Device
c) MCP4532-503E/XX: 50 kΩ, 8LD Device
d) MCP4532-104E/XX: 100 kΩ, 8LD Device
e) MCP4532T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4551-502E/XX: 5 kΩ, 8LD Device
b) MCP4551-103E/XX: 10 kΩ, 8-LD Device
c) MCP4551-503E/XX: 50 kΩ, 8LD Device
d) MCP4551-104E/XX: 100 kΩ, 8LD Device
e) MCP4551T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4552-502E/XX: 5 kΩ, 8LD Device
b) MCP4552-103E/XX: 10 kΩ, 8-LD Device
c) MCP4552-503E/XX: 50 kΩ, 8LD Device
d) MCP4552-104E/XX: 100 kΩ, 8LD Device
e) MCP4552T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4631-502E/XX: 5 kΩ, 8LD Device
b) MCP4631-103E/XX: 10 kΩ, 8-LD Device
c) MCP4631-503E/XX: 50 kΩ, 8LD Device
d) MCP4631-104E/XX: 100 kΩ, 8LD Device
e) MCP4631T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4632-502E/XX: 5 kΩ, 8LD Device
b) MCP4632-103E/XX: 10 kΩ, 8-LD Device
c) MCP4632-503E/XX: 50 kΩ, 8LD Device
d) MCP4632-104E/XX: 100 kΩ, 8LD Device
e) MCP4632T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4651-502E/XX: 5 kΩ, 8LD Device
b) MCP4651-103E/XX: 10 kΩ, 8-LD Device
c) MCP4651-503E/XX: 50 kΩ, 8LD Device
d) MCP4651-104E/XX: 100 kΩ, 8LD Device
e) MCP4651T-104E/XX: T/R, 100 kΩ, 8LD Device

a) MCP4652-502E/XX: 5 kΩ, 8LD Device
b) MCP4652-103E/XX: 10 kΩ, 8-LD Device
c) MCP4652-503E/XX: 50 kΩ, 8LD Device
d) MCP4652-104E/XX: 100 kΩ, 8LD Device
e) MCP4652T-104E/XX: T/R, 100 kΩ, 8LD Device

XX = MF for 8/10-lead 3x3 DFN
= ML for 16-lead QFN
= MS for 8-lead MSOP
= ST for 14-lead TSSOP
= UN for 10-lead MSOP

NOTES:

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