

DS25CP152 3.125 Gbps LVDS 2x2 Crosspoint Switch

Check for Samples: [DS25CP152](#)

FEATURES

- DC - 3.125 Gbps Low Jitter, Low Skew, Low Power Operation
- Pin Configurable, Fully Differential, Non-Blocking Architecture
- On-Chip 100Ω Input and Output Terminations Minimize Return Losses, Reduce Component Count and Minimize Board Space
- 8 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small 4 mm x 4 mm WQFN-16 Space Saving Package

APPLICATIONS

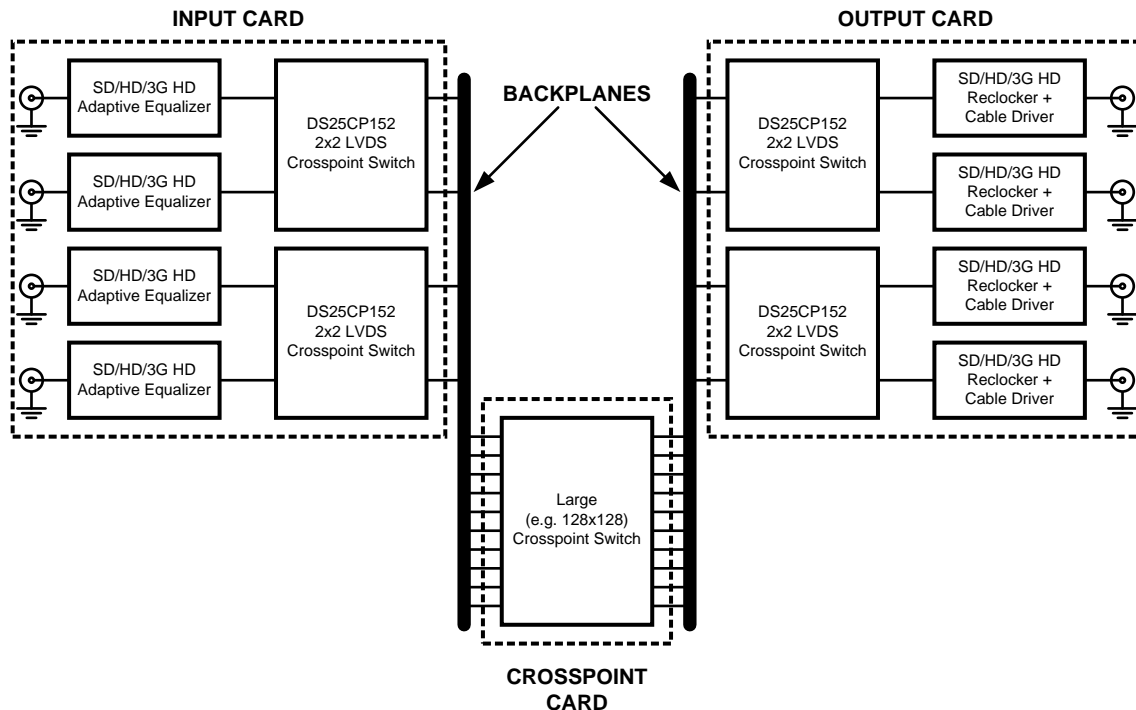
- High-Speed Channel select Applications
- Clock and Data Buffering and Muxing
- OC-48 / STM-16
- SD/HD/3G HD SDI Routers

DESCRIPTION

The DS25CP152 is a 3.125 Gbps 2x2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower device return losses, reduce component count and further minimize board space.

Typical Application


Figure 1. Typical Application


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Block Diagram

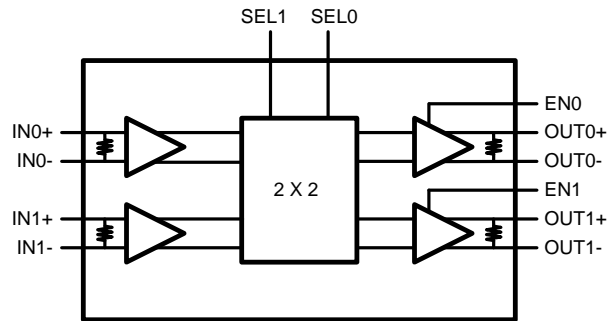


Figure 2. Block Diagram

Connection Diagram

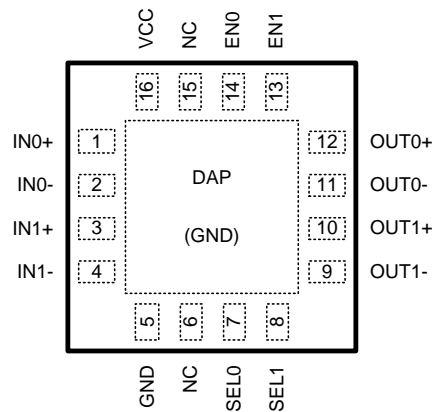


Figure 3. DS25CP152 Pin Diagram

PIN DESCRIPTIONS

| Pin Name | Pin Number | I/O, Type | Pin Description |
|----------------------------|---------------|-----------|---|
| IN0+, IN0-, IN1+, IN1- | 1, 2, 3, 4 | I, LVDS | Inverting and non-inverting high speed LVDS input pins. |
| OUT0+, OUT0-, OUT1+, OUT1- | 12, 11, 10, 9 | O, LVDS | Inverting and non-inverting high speed LVDS output pins. |
| SEL0, SEL1 | 7, 8 | I, LVCMOS | Switch configuration pins. There is a 20 kΩ pull-down resistor on each pin. |
| EN0, EN1 | 14, 13 | I, LVCMOS | Output enable pins. There is a 20 kΩ pull-down resistor on each pin. |
| NC | 6, 15 | I, LVCMOS | "NO CONNECT" pins. |
| VDD | 16 | Power | Power supply pin. |
| GND | 5, DAP | Power | Ground pin and Device Attach Pad (DAP) ground. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | |
|--|------------------------------|
| Supply Voltage | -0.3V to +4V |
| LVCMOS Input Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Input Voltage | -0.3V to +4V |
| Differential Input Voltage VID | 1.0V |
| LVDS Output Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Differential Output Voltage | 0V to 1.0V |
| LVDS Output Short Circuit Current Duration | 5 ms |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature Range | |
| Soldering (4 sec.) | +260°C |
| Maximum Package Power Dissipation at 25°C | |
| RGH0016A Package | 2.99W |
| Derate RGH0016A Package | 23.9 mW/°C above +25°C |
| Package Thermal Resistance | |
| θ_{JA} | +41.8°C/W |
| θ_{JC} | +6.9°C/W |
| ESD Susceptibility | |
| HBM ⁽³⁾ | ≥8 kV |
| MM ⁽⁴⁾ | ≥250V |
| CDM ⁽⁵⁾ | ≥1250V |

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

| | Min | Typ | Max | Units |
|--|-----|-----|-----|-------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Receiver Differential Input Voltage (V_{ID}) | 0 | | 1 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |

DC Electrical Characteristics

 Over recommended operating supply and temperature ranges unless otherwise specified.^{(1) (2) (3)}

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------------|--------------------------|------------------------------------|-----|-----|----------|-------|
| LVCMOS DC SPECIFICATIONS | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{CC} | V |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V |
| I_{IH} | High Level Input Current | $V_{IN} = 3.6V$ $V_{CC} = 3.6V$ | 40 | 175 | 250 | μA |
| I_{IL} | Low Level Input Current | $V_{IN} = GND$ $V_{CC} = 3.6V$ | | 0 | ±10 | μA |

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .
- (3) Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25°C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.^{(1) (2) (3)}

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------------|--|---|------|------|------------------------|-------|
| V _{CL} | Input Clamp Voltage | I _{CL} = -18 mA, V _{CC} = 0V | | -0.9 | -1.5 | V |
| LVDS INPUT DC SPECIFICATIONS | | | | | | |
| V _{ID} | Input Differential Voltage | | 0 | | 1 | V |
| V _{TH} | Differential Input High Threshold | V _{CM} = +0.05V or V _{CC} -0.05V | | 0 | +100 | mV |
| V _{TL} | Differential Input Low Threshold | | -100 | 0 | | mV |
| V _{CMR} | Common Mode Voltage Range | V _{ID} = 100 mV | 0.05 | | V _{CC} - 0.05 | V |
| I _{IN} | Input Current | V _{IN} = +3.6V or 0V V _{CC} = 3.6V or 0V | | ±1 | ±10 | µA |
| C _{IN} | Input Capacitance | Any LVDS Input Pin to GND | | 1.7 | | pF |
| R _{IN} | Input Termination Resistor | Between IN+ and IN- | | 100 | | Ω |
| LVDS OUTPUT DC SPECIFICATIONS | | | | | | |
| V _{OD} | Differential Output Voltage | | 250 | 350 | 450 | mV |
| ΔV _{OD} | Change in Magnitude of V _{OD} for Complimentary Output States | R _L = 100Ω | -35 | | 35 | mV |
| V _{OS} | Offset Voltage | | 1.05 | 1.2 | 1.375 | V |
| ΔV _{OS} | Change in Magnitude of V _{OS} for Complimentary Output States | R _L = 100Ω | -35 | | 35 | mV |
| I _{OS} | Output Short Circuit Current ⁽⁴⁾ | OUT to GND | | -35 | -55 | mA |
| | | OUT to V _{CC} | | 7 | 55 | mA |
| C _{OUT} | Output Capacitance | Any LVDS Output Pin to GND | | 1.2 | | pF |
| R _{OUT} | Output Termination Resistor | Between OUT+ and OUT- | | 100 | | Ω |
| SUPPLY CURRENT | | | | | | |
| I _{CC} | Supply Current | EN0 = EN1 = High | | 64 | 77 | mA |
| I _{CCZ} | Supply Current with Outputs Disabled | EN0 = EN1 = Low | | 23 | 29 | mA |

(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.^{(1) (2)}

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|-----------------------|-----|-----|-----|-------|
| LVDS OUTPUT AC SPECIFICATIONS | | | | | | |
| t _{PLHD} | Differential Propagation Delay Low to High ⁽³⁾ | R _L = 100Ω | | 340 | 500 | ps |
| t _{PHLD} | Differential Propagation Delay High to Low ⁽³⁾ | | | 344 | 500 | ps |
| t _{SKD1} | Pulse Skew t _{PLHD} - t _{PHLD} ^{(3) (4)} | | | 4 | 35 | ps |
| t _{SKD2} | Channel to Channel Skew ^{(3) (5)} | | | 12 | 40 | ps |
| t _{SKD3} | Part to Part Skew ^{(3) (6)} | | | 50 | 150 | ps |

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (3) Specification is ensured by characterization and is not tested in production.
- (4) t_{SKD1}, |t_{PLHD} - t_{PHLD}|, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (5) t_{SKD2}, Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).
- (6) t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified ⁽¹⁾ ⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|--|------------|------|------|-------------------|
| t_{LHT} | Rise Time ⁽³⁾ | $R_L = 100\Omega$ | | 65 | 120 | ps |
| t_{HLT} | Fall Time ⁽³⁾ | | | 65 | 120 | ps |
| t_{ON} | Output Enable Time | ENn = LH to output active | | 7 | 20 | μ s |
| t_{OFF} | Output Disable Time | ENn = HL to output inactive | | 5 | 12 | ns |
| t_{SEL} | Select Time | SELn LH or HL to output | | 3.5 | 12 | ns |
| JITTER PERFORMANCE ⁽³⁾ | | | | | | |
| t_{RJ1} | Random Jitter (RMS Value) ⁽⁷⁾ | $V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ Clock (RZ) | 2.5 Gbps | 0.5 | 1 | ps |
| t_{RJ2} | | | 3.125 Gbps | 0.5 | 1 | ps |
| t_{DJ1} | Deterministic Jitter (Peak to Peak) ⁽⁸⁾ | $V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ K28.5 (NRZ) | 2.5 Gbps | 8 | 25 | ps |
| t_{DJ2} | | | 3.125 Gbps | 3 | 19 | ps |
| t_{TJ1} | Total Jitter (Peak to Peak) ⁽⁹⁾ | $V_{ID} = 350\text{ mV}$ $V_{CM} = 1.2\text{ V}$ PRBS-23 (NRZ) | 2.5 Gbps | 0.04 | 0.08 | UI _{P-P} |
| t_{TJ2} | | | 3.125 Gbps | 0.03 | 0.09 | UI _{P-P} |

(7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

(8) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

(9) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

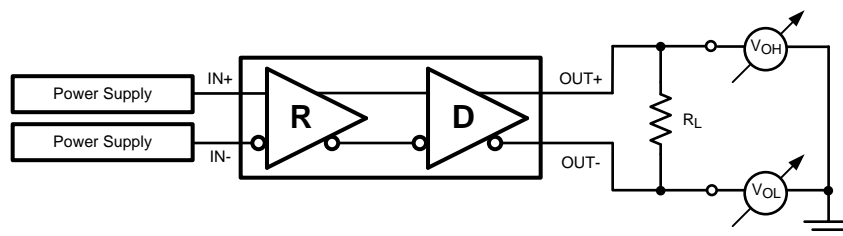


Figure 4. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

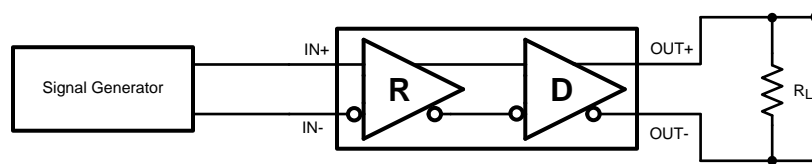


Figure 5. Differential Driver AC Test Circuit

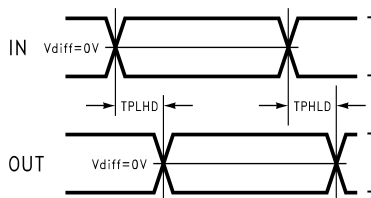


Figure 6. Propagation Delay Timing Diagram

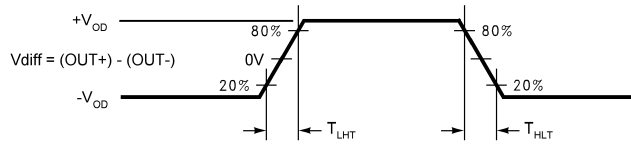


Figure 7. LVDS Output Transition Times

Functional Description

The DS25CP152 is a 3.125 Gbps 2x2 LVDS digital crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables.

Table 1. Switch Configuration Truth Table

| S1 | S0 | OUT1 | OUT0 |
|----|----|------|------|
| 0 | 0 | IN0 | IN0 |
| 0 | 1 | IN0 | IN1 |
| 1 | 0 | IN1 | IN0 |
| 1 | 1 | IN1 | IN1 |

Table 2. Output Enable Truth Table

| EN1 | EN0 | OUT1 | OUT0 |
|-----|-----|----------|----------|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Disabled | Enabled |
| 1 | 0 | Enabled | Disabled |
| 1 | 1 | Enabled | Enabled |

Input Interfacing

The DS25CP152 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25CP152 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25CP152 inputs are internally terminated with a 100Ω resistor.

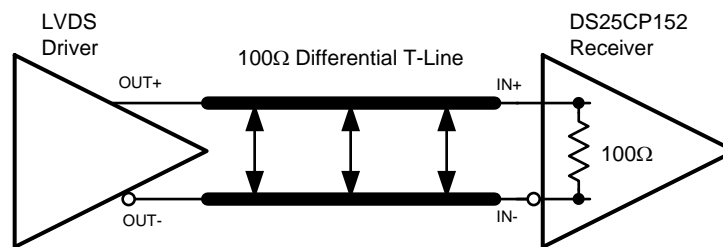


Figure 8. Typical LVDS Driver DC-Coupled Interface to DS25CP152 Input

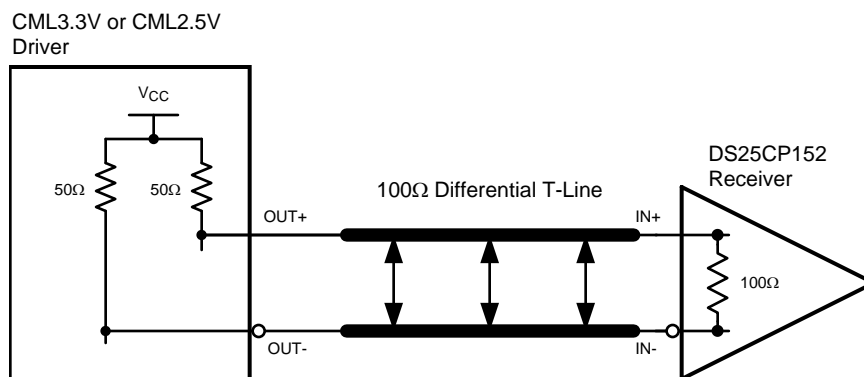


Figure 9. Typical CML Driver DC-Coupled Interface to DS25CP152 Input

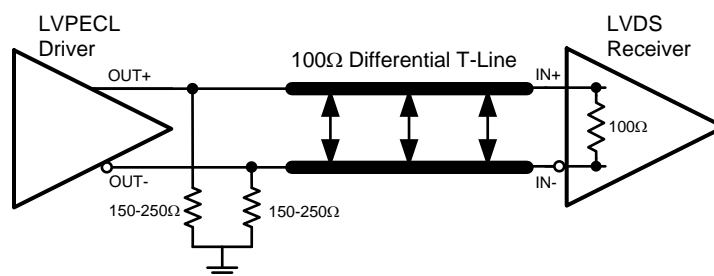


Figure 10. Typical LVPECL Driver DC-Coupled Interface to DS25CP152 Input

Output Interfacing

The DS25CP152 outputs signals that are compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's data sheet prior to implementing the suggested interface implementation.

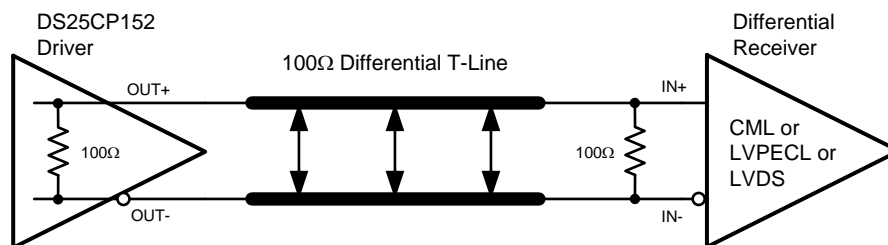


Figure 11. Typical DS25CP152 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics

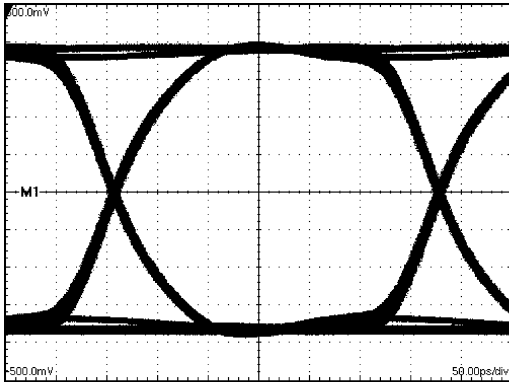


Figure 12. A 3.125 Gbps NRZ PRBS-7 After 2" Differential FR-4 Stripline
V:100 mV / DIV, H:50 ps / DIV

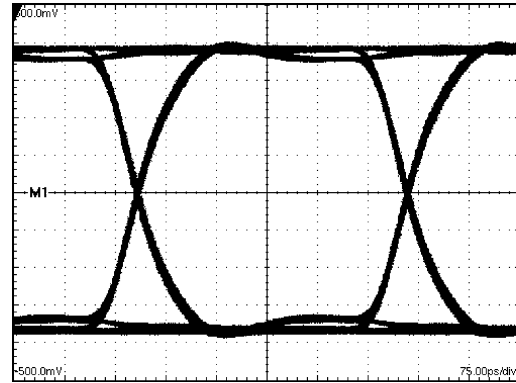


Figure 13. A 2.5 Gbps NRZ PRBS-7 After 2" Differential FR-4 Stripline
V:100 mV / DIV, H:75 ps / DIV

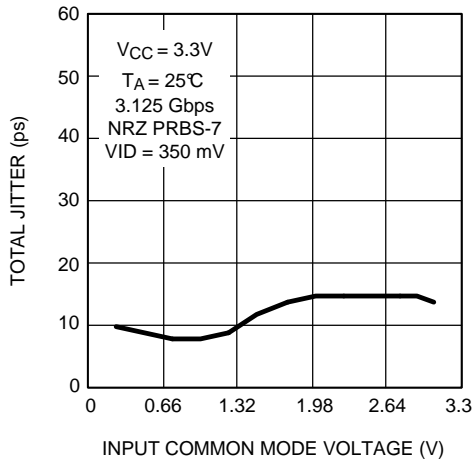


Figure 14. Total Jitter as a Function of Input Common Mode Voltage

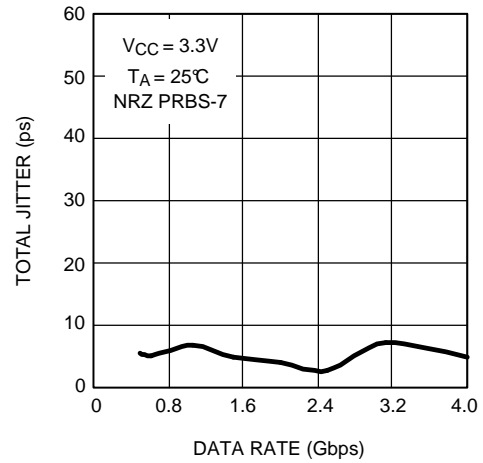


Figure 15. Total Jitter as a Function of Data Rate

REVISION HISTORY

| Changes from Revision C (April 2013) to Revision D | Page |
|--|----------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 8 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DS25CP152TSQ/NOPB | ACTIVE | WQFN | RGH | 16 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 85 | 2C152SQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

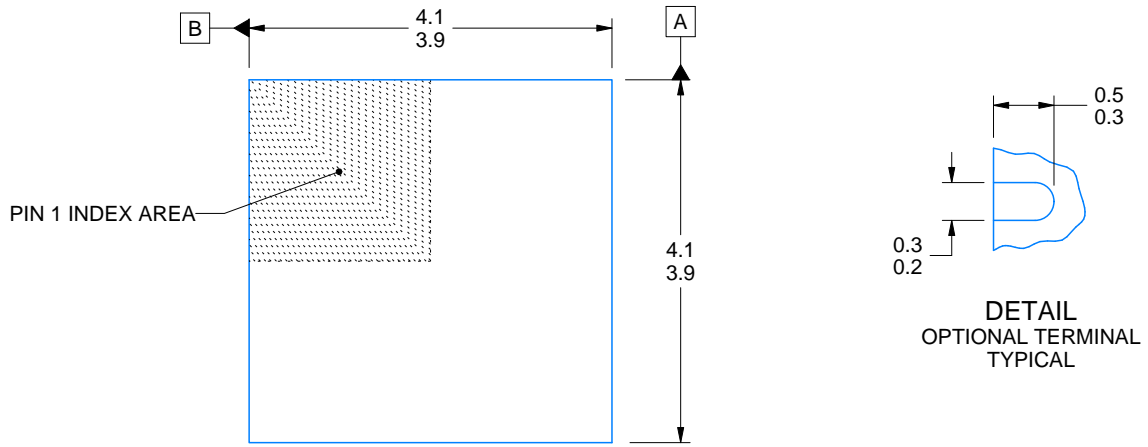
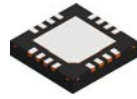
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS25CP152TSQ/NOPB | WQFN | RGH | 16 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

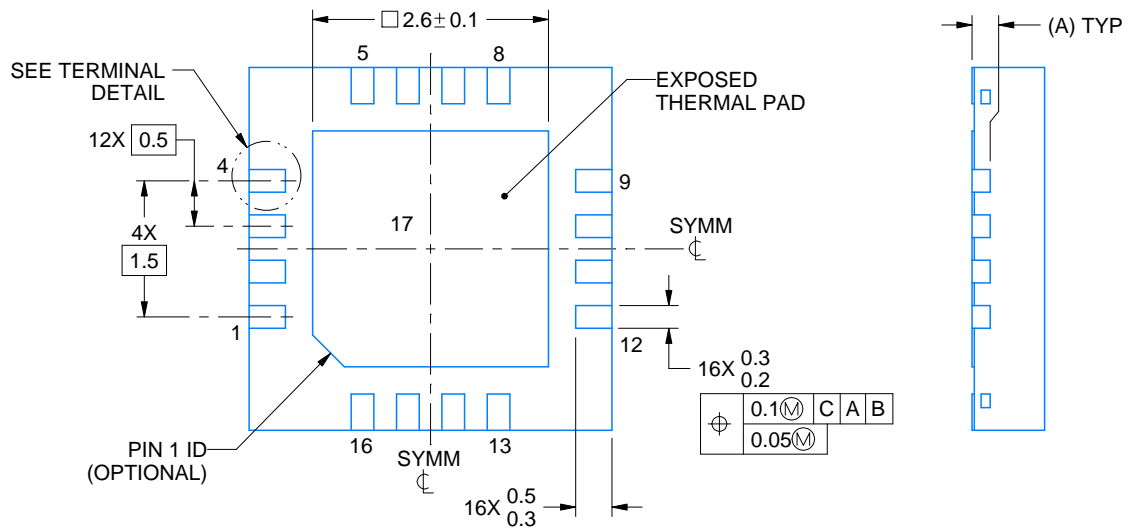
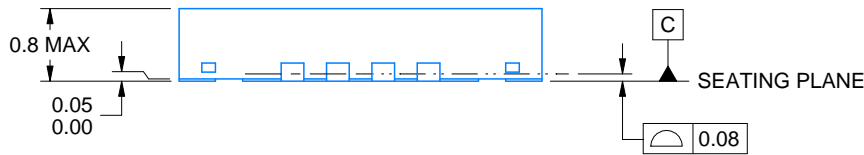


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS25CP152TSQ/NOPB | WQFN | RGH | 16 | 1000 | 210.0 | 185.0 | 35.0 |



| DIM A | |
|-------|-------|
| OPT 1 | OPT 1 |
| (0.1) | (0.2) |



4214978/B 01/2017

NOTES:

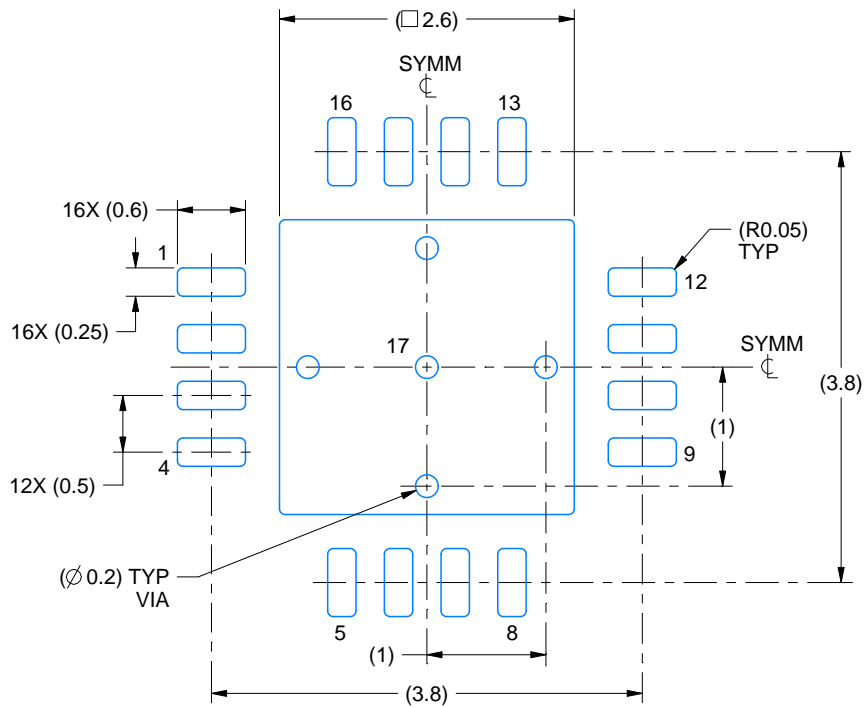
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

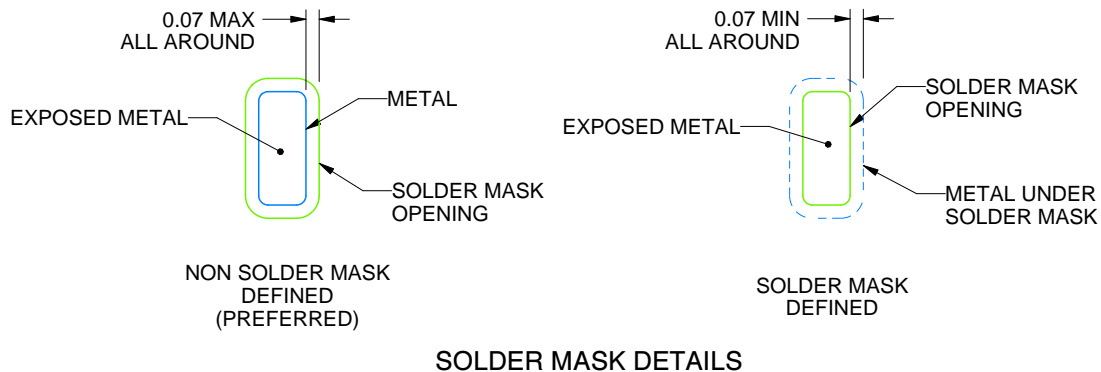
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



4214978/B 01/2017

NOTES: (continued)

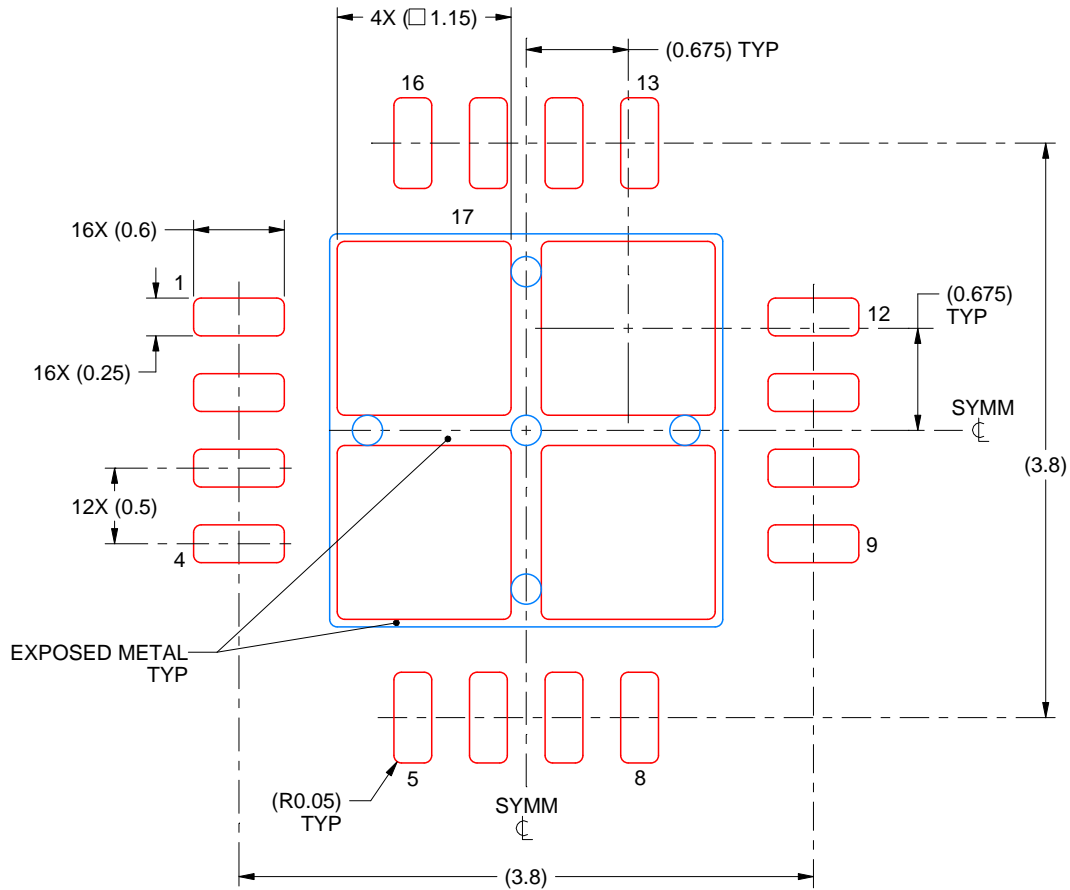
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214978/B 01/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated