LM4889 Boomer® Audio Power Amplifier Series 1 Watt Audio Power Amplifier

Check for Samples: LM4889

FEATURES

- **Available in Space-Saving VSSOP, SOIC, WSON, and DSBGA Packages**
- **Ultra Low Current Shutdown Mode (3.3 to 2.6V - 0.01µA)**
- **Can Drive Capacitive Loads up to 500 pF**
- **Improved Pop & Click Circuitry Eliminates Noises During Turn-On and Turn-Off Transitions**
- **2.2 - 5.5V Operation**
- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**
- **Unity-Gain Stable**
- **External Gain Configuration Capability**

APPLICATIONS

- **Mobile Phones**
- **PDAs**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **Improved PSRR at 217Hz, 5 - 3.3V 75dB**
- **Power Output at 5.0V & 2% THD 1.0W(typ.)**
- **Power Output at 3.3V & 1% THD 400mW(typ.)**
- **Shutdown Current at 3.3 & 2.6V 0.01µA(typ.)**

DESCRIPTION

The LM4889 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 2% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer™ audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4889 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4889 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with a logic low. Additionally, the LM4889 features an internal thermal shutdown protection mechanism.

The LM4889 contains advanced pop & click circuitry to eliminate noise which would otherwise occur during turn-on and turn-off transitions.

The LM4889 is unity-gain stable and can be configured by external gain-setting resistors.

Typical Application

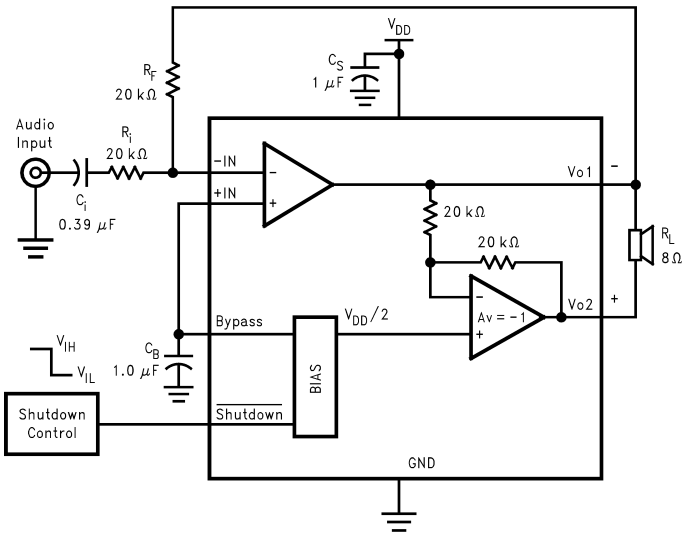


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

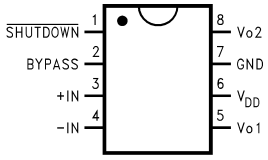


Figure 2. Small Outline (SOIC) Package - Top View
See Package Number D

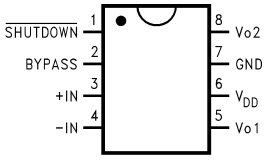


Figure 3. Mini Small Outline (VSSOP) Package – Top View
See Package Number DGK

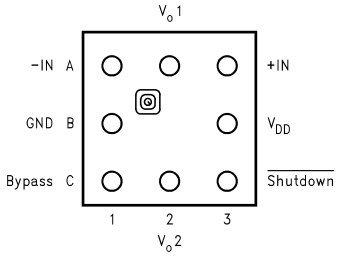


Figure 4. 8-Bump DSBGA - Top View
See Package Number YZR0008

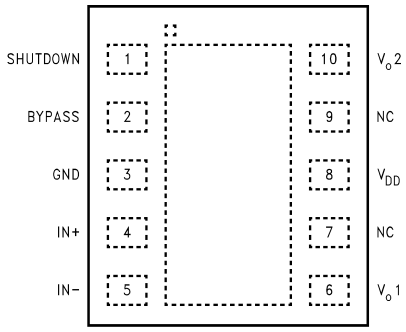


Figure 5. WSON Package - Top View
See Package Number NGZ

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(3)		Internally Limited
ESD Susceptibility(4)		2000V
ESD Susceptibility(5)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JC} (SOIC)	35°C/W
	θ_{JA} (SOIC)	150°C/W
	θ_{JA} (8 Bump DSBGA)(6)	210°C/W
	θ_{JC} (VSSOP)	56°C/W
	θ_{JA} (VSSOP)	190°C/W
	θ_{JA} (WSON)	220°C/W
Soldering Information		See the AN-1112 Application Report.

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4889, see power derating currents for additional information.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) Machine Model, 220 pF–240 pF discharged through all pins.
(6) All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. The LM4889ITL demo board (views featured in the Application Information section) has two inner layers, one for V_{DD} and one for GND. The planes each measure 600mils x 600mils (15.24mm x 15.24mm) and aid in spreading heat due to power dissipation within the IC.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage	$2.2V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V(1)(2)

The following specifications apply for V_{DD} = 5V, A_V = 2, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4889		Units (Limits)
			Typical(3)	Limit(4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, no Load	4	8	mA (max)
		V_{IN} = 0V, I_o = 0A, with BTL Load	5	8	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{shutdown}}$ = GND(6)	0.1	2	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
P_o	Output Power	THD = 2% (max); f = 1 kHz	1		W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.4 Wrms; f = 1kHz	0.1		%

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test or statistical analysis.
(6) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

Electrical Characteristics V_{DD} = 5V[1][2] (continued)

The following specifications apply for V_{DD} = 5V, A_V = 2, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4889		Units (Limits)
			Typical[3]	Limit[4][5]	
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p f_{ripple} = 217Hz f_{ripple} = 1kHz	 62 66		 dB dB
		V_{ripple} = 200mV sine p-p Input Floating	 75	 68	 dB

Electrical Characteristics V_{DD} = 3.3V[1][2]

The following specifications apply for V_{DD} = 3.3V, A_V = 2, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4889		Units (Limits)
			Typical[3]	Limit[4][5]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, no Load	3.5	7	mA (max)
		V_{IN} = 0V, I_o = 0A, with BTL Load	4.5	7	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{shutdown}}$ = GND[6]	0.01	2	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
P_o	Output Power	THD = 1% (max); f = 1kHz	0.4		W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.25Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p f_{ripple} = 217Hz f_{ripple} =1kHz	 60 62		 dB dB

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test or statistical analysis.
(6) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

Electrical Characteristics V_{DD} = 2.6V[1][2]

The following specifications apply for V_{DD} = 2.6V, A_V = 2, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4889		Units (Limits)
			Typical[3]	Limit[4][5]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A, no Load	2.6	6	mA (max)
		V_{IN} = 0V, I_o = 0A, with BTL Load	3.0	6	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{shutdown}}$ = GND[6]	0.01	2	µA (max)
P_0	Output Power (8Ω) Output Power (4Ω)	THD = 1% (max); f = 1 kHz THD = 1% (max); f = 1 kHz	0.2 0.22		W W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.1Wrms; f = 1kHz	0.08		%

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test or statistical analysis.
(6) For DSBGA only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2µA.

Electrical Characteristics V_{DD} = 2.6V[1][2] (continued)

The following specifications apply for V_{DD} = 2.6V, A_V = 2, and 8Ω load unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4889		Units (Limits)
			Typical[3]	Limit[4][5]	
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mV sine p-p f_{ripple} = 217Hz f_{ripple} = 1kHz	 44 44		 dB dB

External Components Description

(Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i. $A_{VD} = 2*(R_f/R_i)$.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics

THD+N vs Frequency
at V_{DD} = 5V, 8Ω R_L, and PWR = 250mW

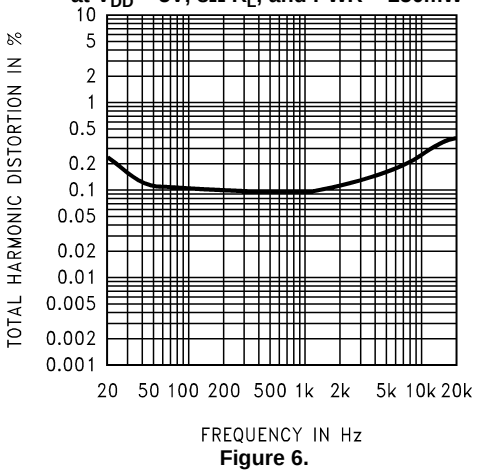


Figure 6.

THD+N vs Frequency
at V_{DD} = 3.3V, 8Ω R_L, and PWR = 150mW

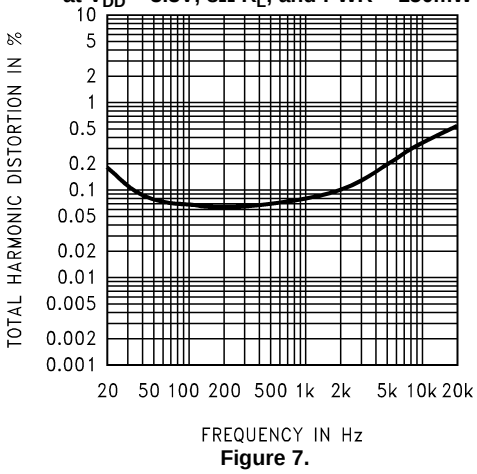


Figure 7.

THD+N vs Frequency
at V_{DD} = 2.6V, 8Ω R_L, and PWR = 100mW

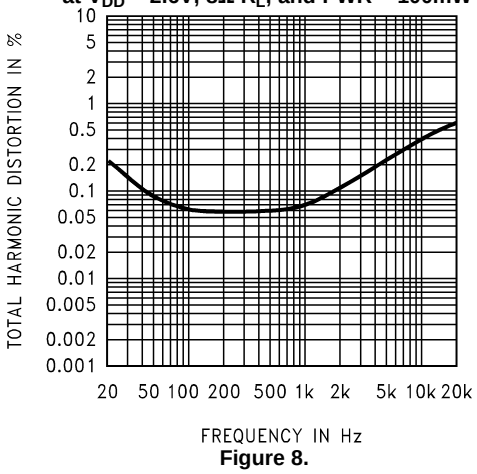


Figure 8.

THD+N vs Frequency
at V_{DD} = 2.6V, 4Ω R_L, and PWR = 100mW

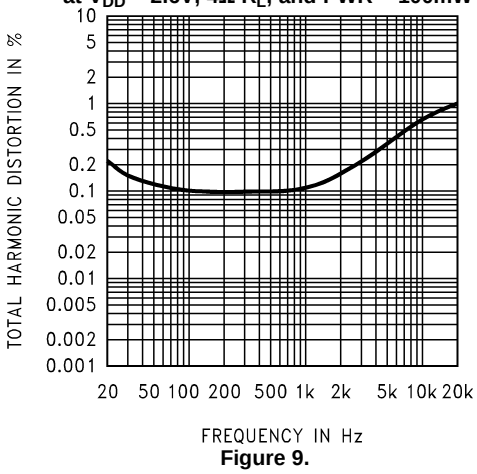


Figure 9.

THD+N vs Power Out
at V_{DD} = 5V, 8Ω R_L, 1kHz

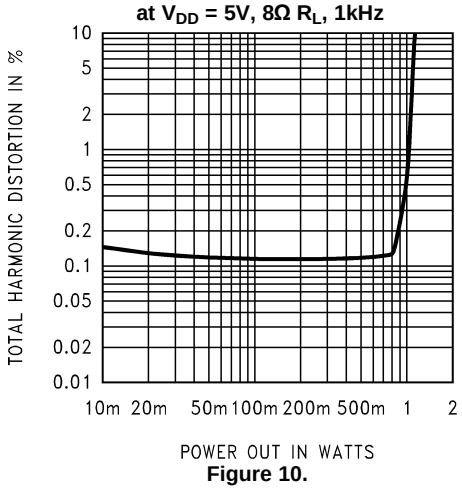


Figure 10.

THD+N vs Power Out
at V_{DD} = 3.3V, 8Ω R_L, 1kHz

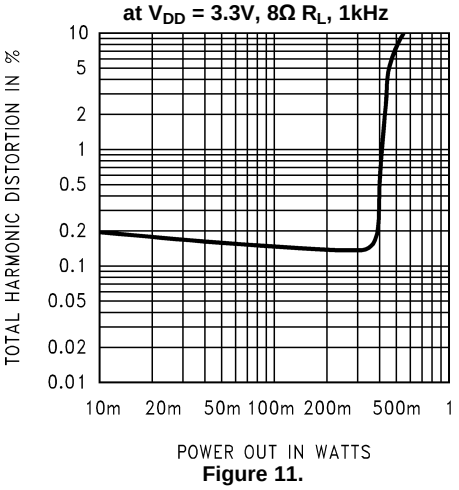


Figure 11.

Typical Performance Characteristics (continued)

THD+N vs Power Out at V_{DD} = 2.6V, 8Ω R_L, 1kHz

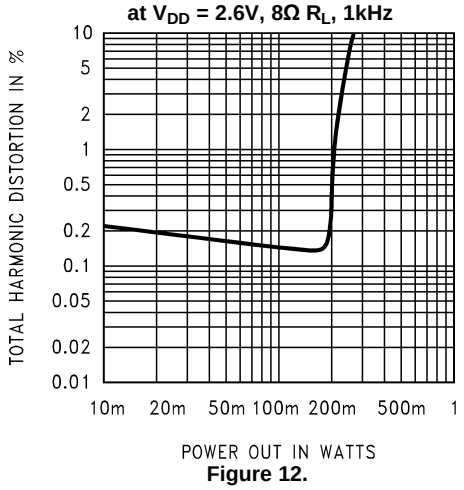


Figure 12.

THD+N vs Power Out at V_{DD} = 2.6V, 4Ω R_L, 1kHz

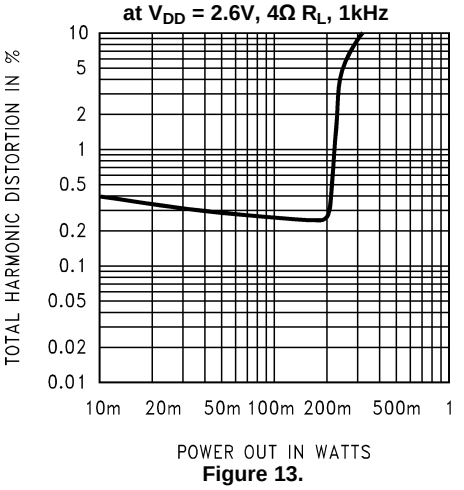


Figure 13.

Power Supply Rejection Ratio (PSRR) at V_{DD} = 5V

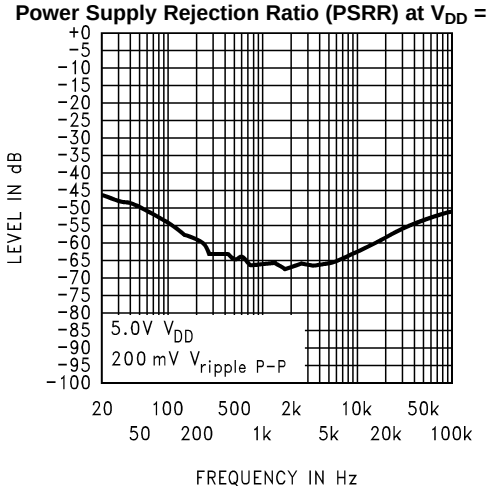


Figure 14. Input terminated with 10Ω R

Power Supply Rejection Ratio (PSRR) at V_{DD} = 5V

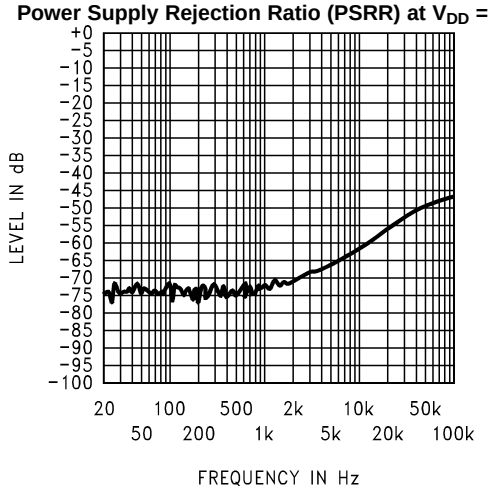


Figure 15. Input Floating

Power Supply Rejection Ratio (PSRR) at V_{DD} = 2.6V

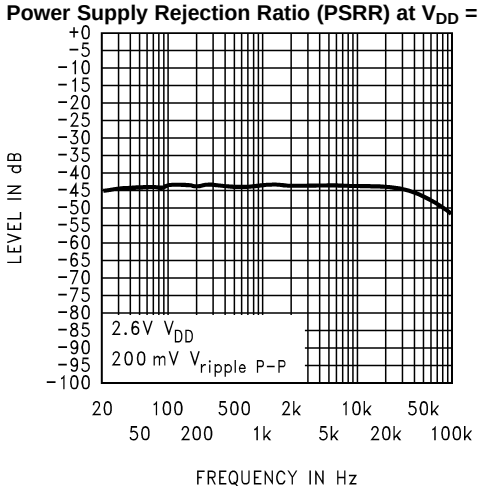


Figure 16. Input terminated with 10Ω R

Power Supply Rejection Ratio (PSRR) at V_{DD} = 3.3V

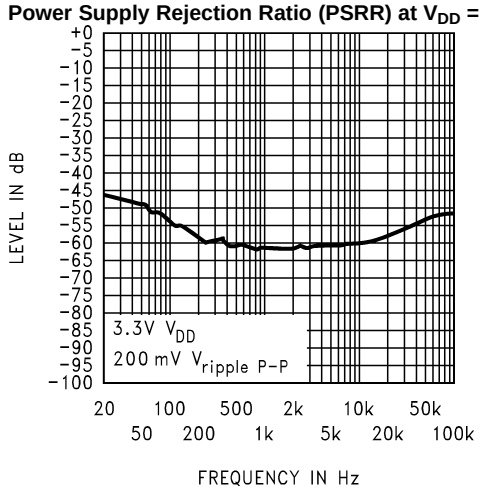


Figure 17. Input terminated with 10Ω R

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power V_{DD} = 3.3V

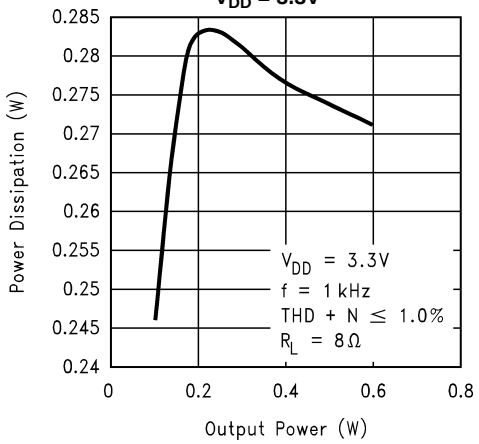


Figure 18.

Power Dissipation vs Output Power V_{DD} = 5V

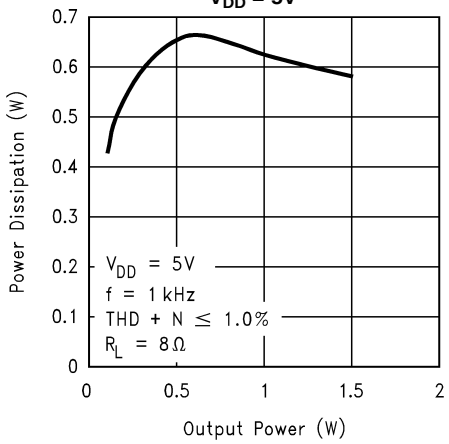


Figure 19.

Output Power vs Load Resistance

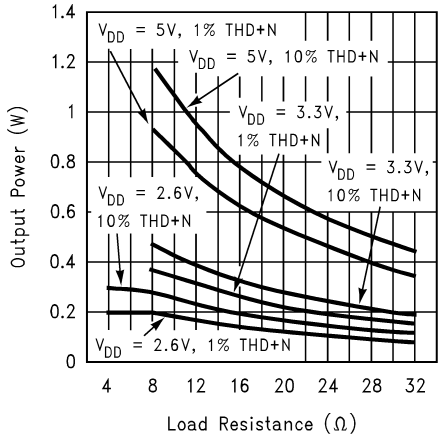


Figure 20.

Power Dissipation vs Output Power V_{DD} = 2.6V

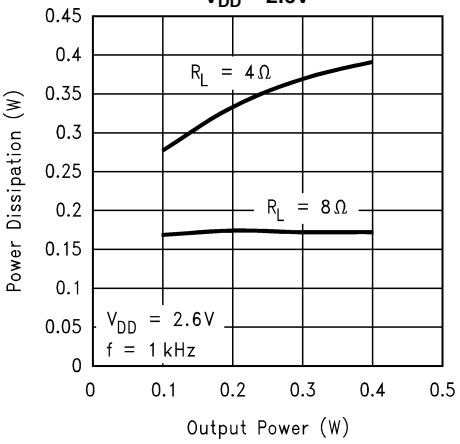


Figure 21.

Supply Current vs Shutdown Voltage

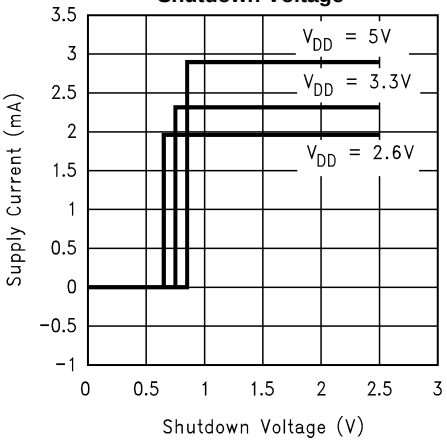


Figure 22.

Clipping (Dropout) Voltage vs Supply Voltage

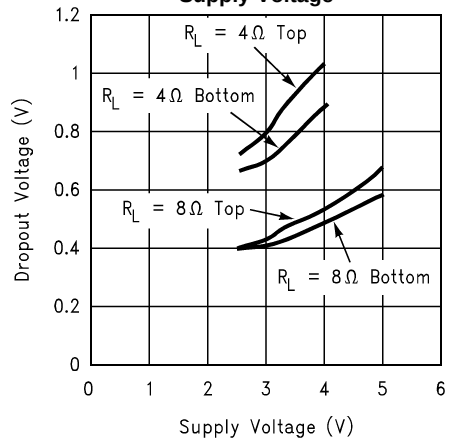


Figure 23.

Typical Performance Characteristics (continued)

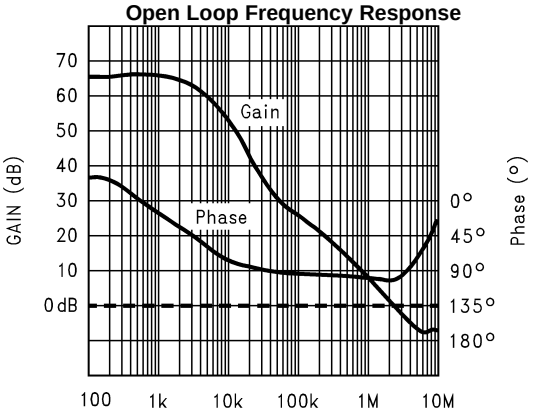


Figure 24.

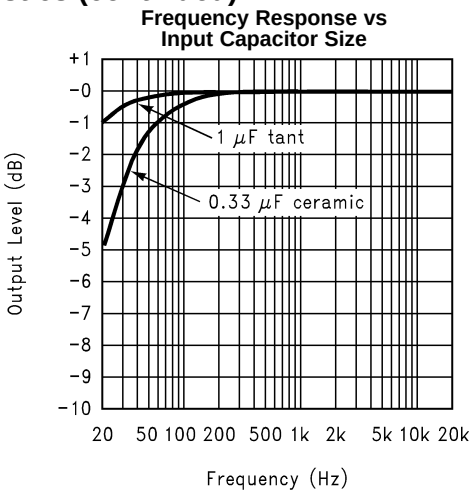


Figure 25.

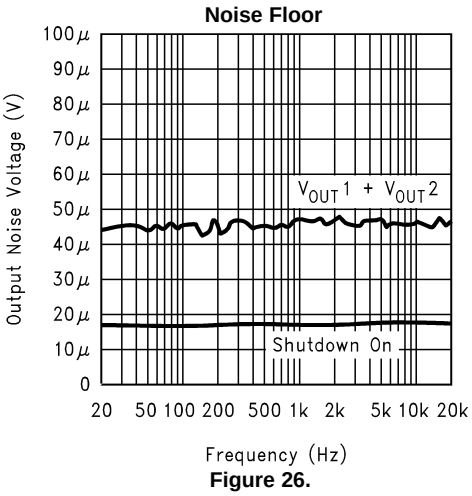


Figure 26.

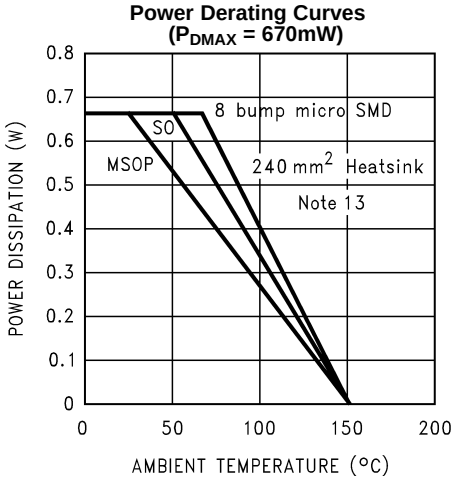


Figure 27.

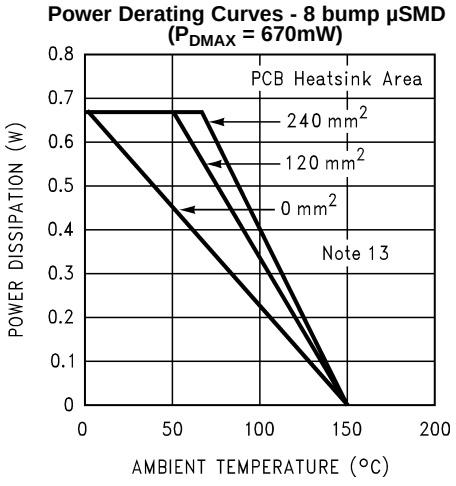


Figure 28.

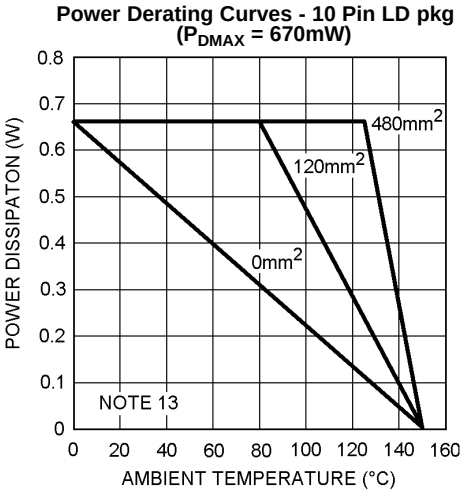


Figure 29.

Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4889 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_i) \quad (1)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has an advantage over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4889, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4889 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from a free air value of 150°C/W, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM4889. It is especially effective when connected to V_{DD}, G_{ND}, and the output pins. Refer to the application information on the LM4889 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4889. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4889 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the LM4889 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than $0.5V_{DC}$, the idle current may be greater than the typical value of 0.1µA. (Idle current is measured with the shutdown pin grounded).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and disables the amplifier. If the switch is open, then the external pull-up resistor will enable the LM4889. This scheme ensures that the shutdown pin will not float thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4889 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4889 is unity-gain stable which gives the designer maximum system flexibility. The LM4889 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few reasons.

SELECTION OF INPUT CAPACITOR SIZE

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz to 150 Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_B, is the most critical component to minimize turn-on pops since it determines how fast the LM4889 turns on. The slower the LM4889's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_B equal to 1.0 µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω Audio Amplifier

- Given:
  - Power Output: 1 Wrms
  - Load Impedance: 8Ω
  - Input Level: 1 Vrms
  - Input Impedance: 20 kΩ
  - Bandwidth: 100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 3 and add the output voltage. Using this method, the minimum supply voltage would be (V_{opeak} + (V_{ODTOP} + V_{ODBOT})), where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in the Typical Performance Characteristics section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (3)$$

5V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4889 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

$$R_f/R_i = A_{VD}/2 \quad (5)$$

From Equation 3, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance was 20 kΩ, and with a A_{VD} impedance of 2, a ratio of 1.5:1 of R_f to R_i results in an allocation of R_i = 20 kΩ and R_f = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

$$f_L = 100 \text{ Hz}/5 = 20 \text{ Hz} \quad (6)$$

$$f_H = 20 \text{ kHz} * 5 = 100 \text{ kHz} \quad (7)$$

As stated in the External Components Description section, R_i in conjunction with C_i create a highpass filter.

$$C_i \geq 1/(2\pi * 20 \text{ k}\Omega * 20 \text{ Hz}) = 0.397 \ \mu\text{F}; \text{ use } 0.39 \ \mu\text{F} \quad (8)$$

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100 kHz, the resulting GBWP = 300kHz which is much smaller than the LM4889 GBWP of 2.5MHz. This calculation shows that if a designer has a need to design an amplifier with a higher differential gain, the LM4889 can still be used without running into bandwidth limitations.

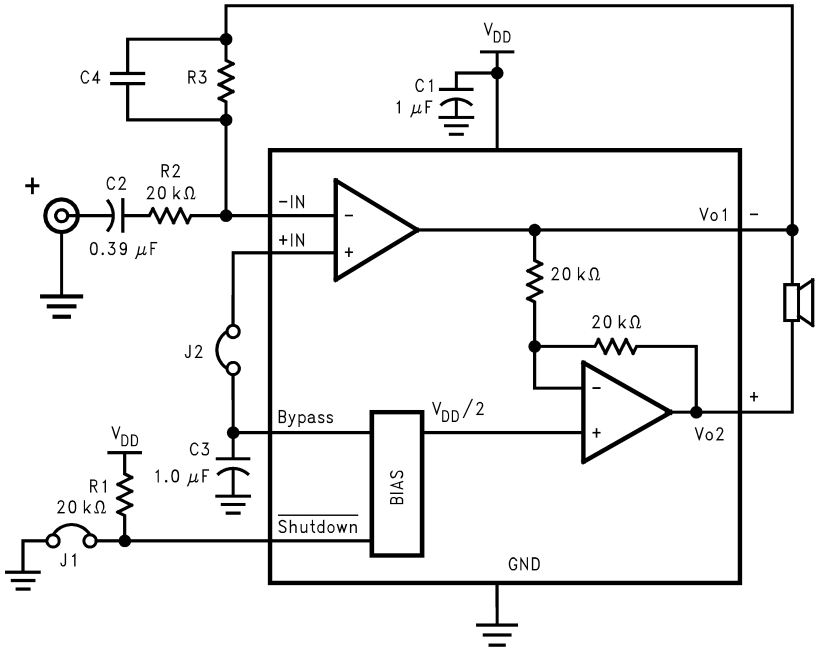


Figure 30. Higher Gain Audio Amplifier

The LM4889 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 30 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320kHz.

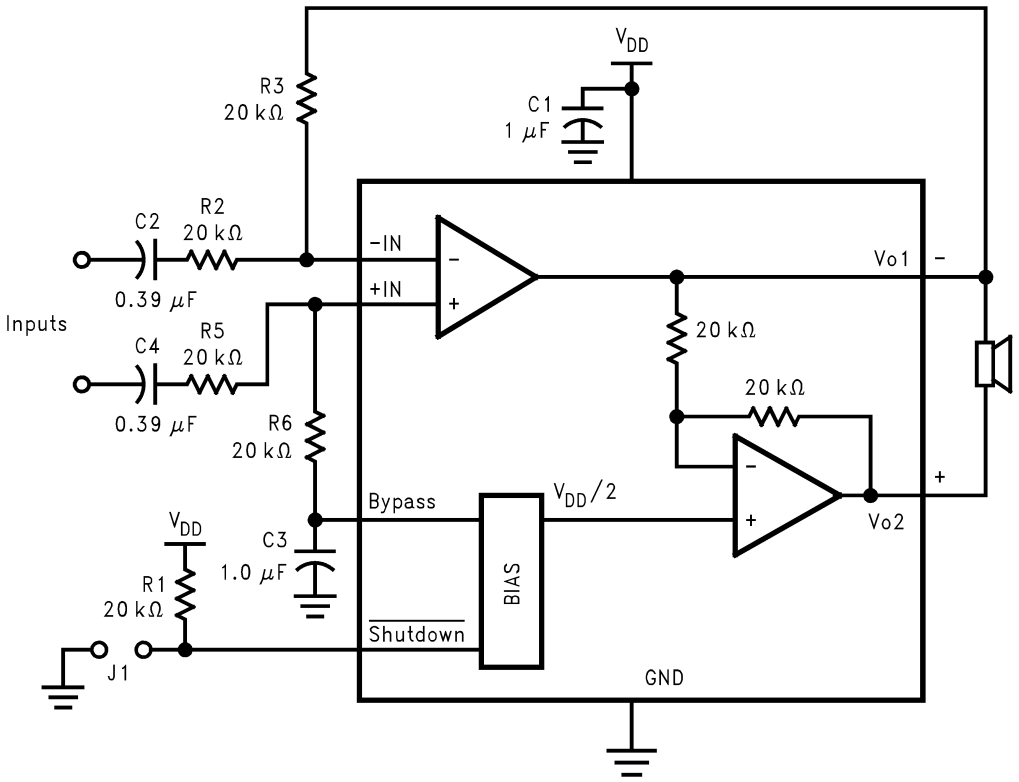


Figure 31. Differential Amplifier Configuration for LM4889

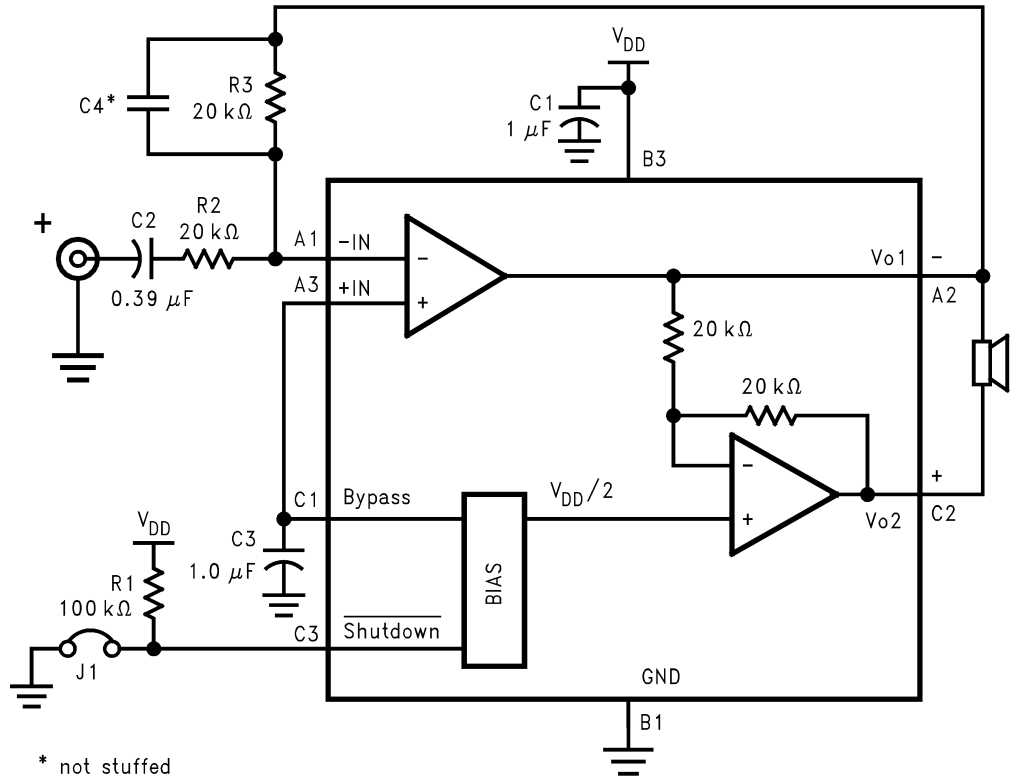
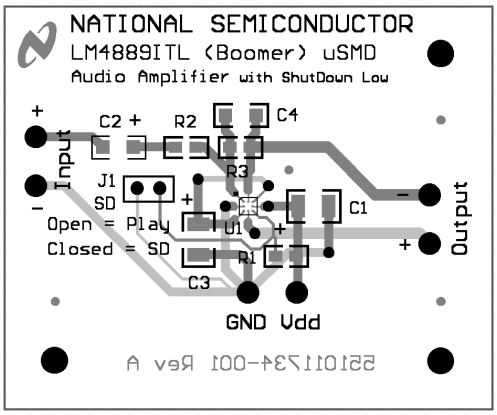


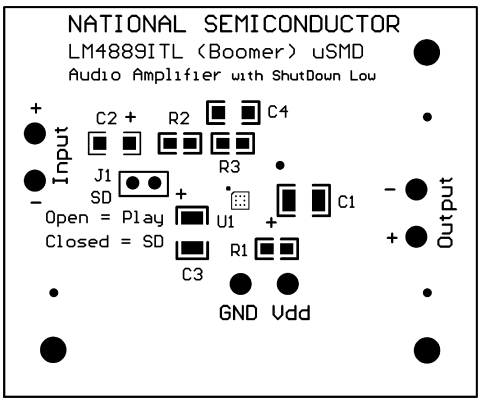
Figure 32. Reference Design Board and Layout - DSBGA

LM4889 DSBGA DEMO BOARD ARTWORK

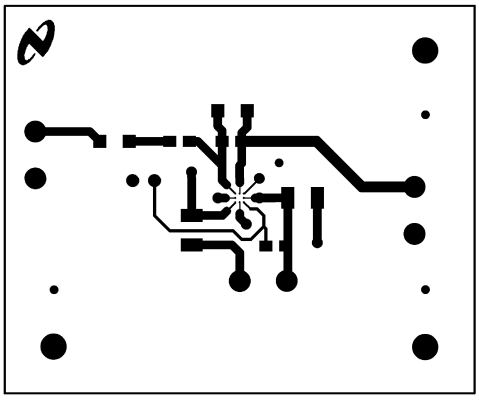
Composite View



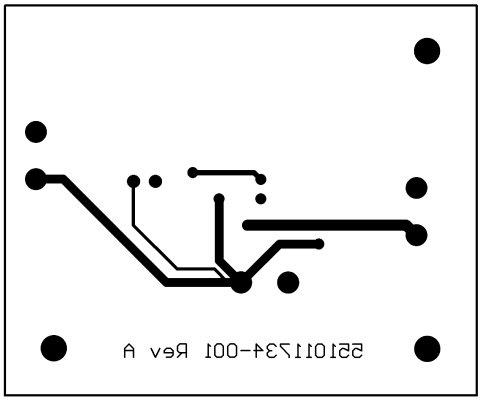
Silk Screen



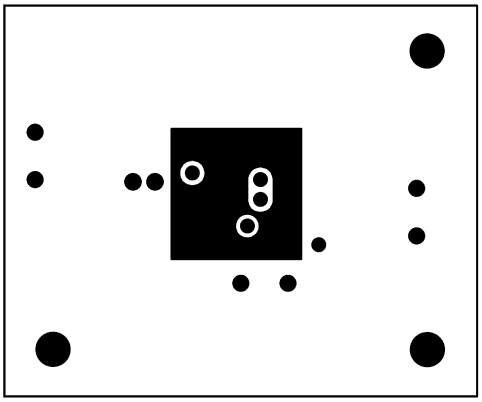
Top Layer



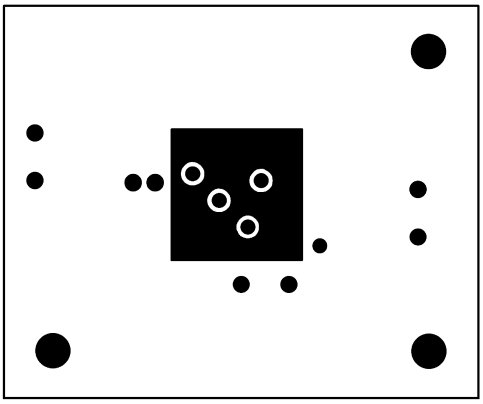
Bottom Layer



Inner Layer Ground



Inner Layer V_{DD}



REFERENCE DESIGN BOARD AND PCB LAYOUT GUIDELINES - VSSOP & SOIC BOARDS

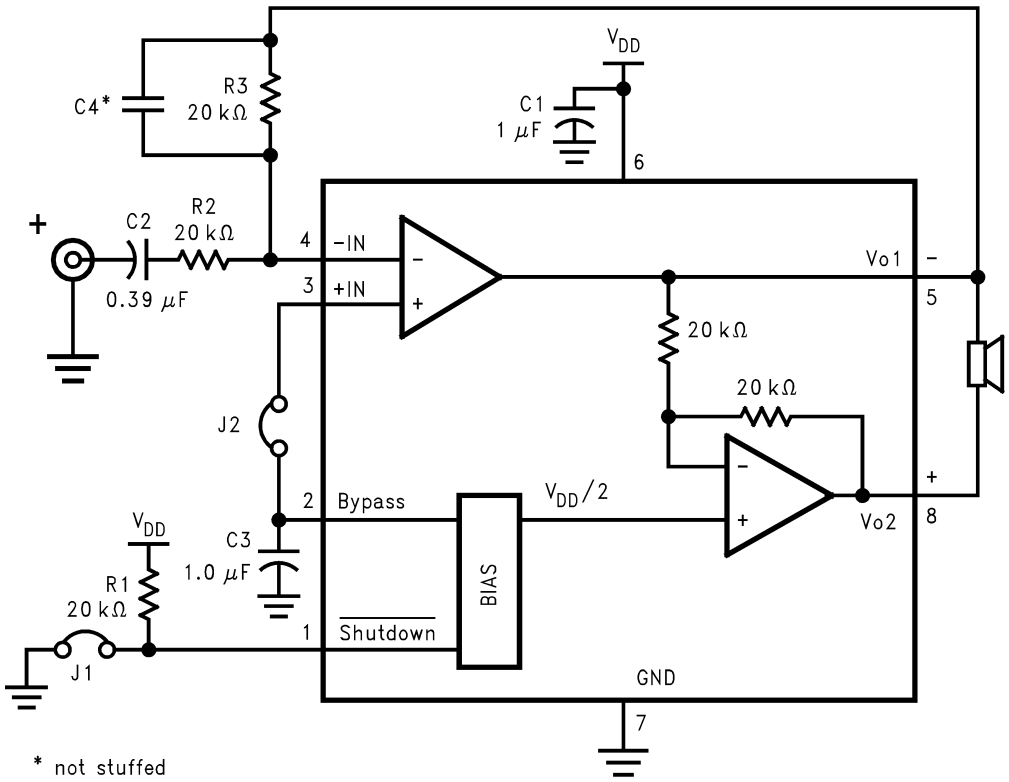


Figure 33. Reference Design Board

LM4889 SOIC DEMO BOARD ARTWORK

Figure 34. Silk Screen

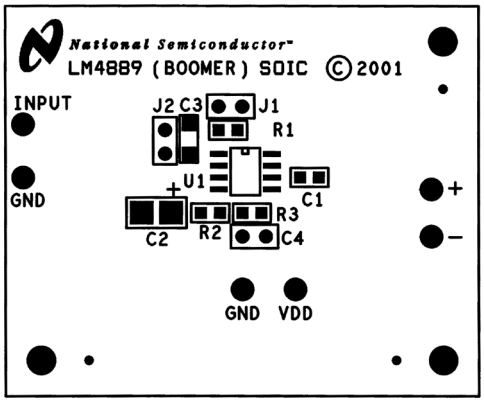


Figure 35. Top Layer

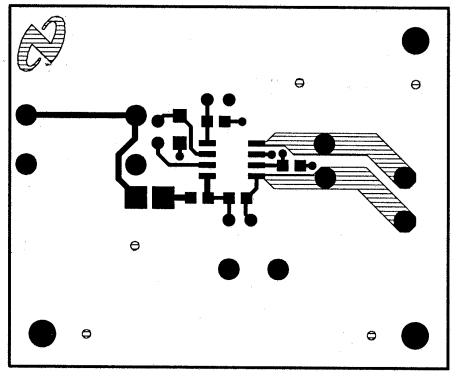
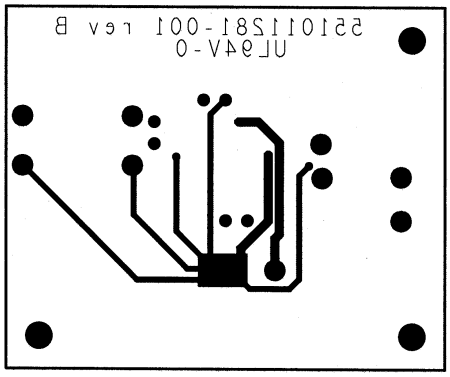


Figure 36. Bottom Layer



LM4889 VSSOP DEMO BOARD ARTWORK

Figure 37. Silk Screen

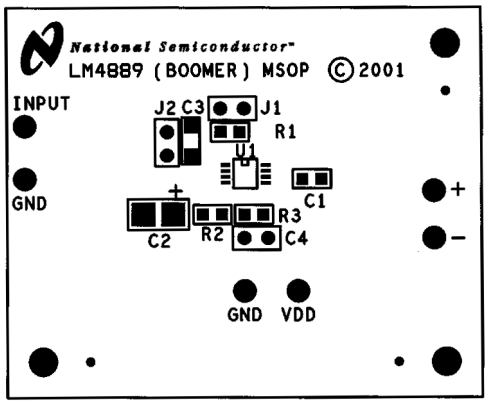


Figure 38. Top Layer

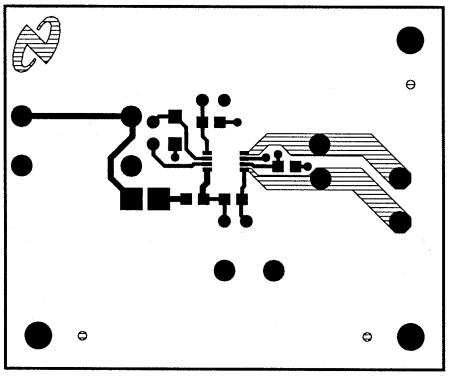
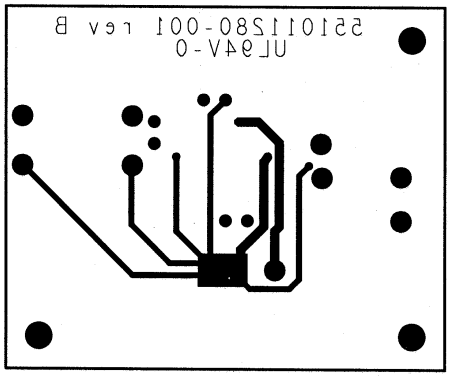


Figure 39. Bottom Layer



REVISION HISTORY

Changes from Revision G (May 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4889MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM48 89MA	Samples
LM4889MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM48 89MA	Samples
LM4889MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	GA2	Samples
LM4889MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	GA2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

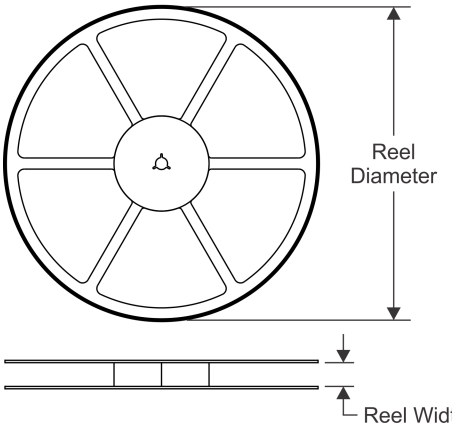
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

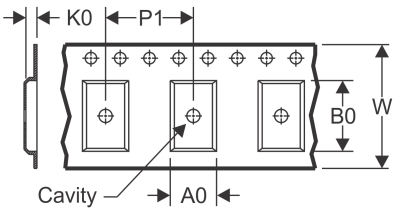
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

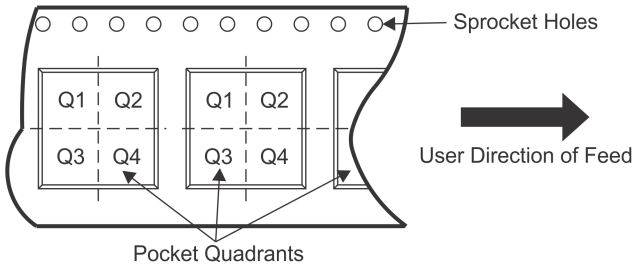


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

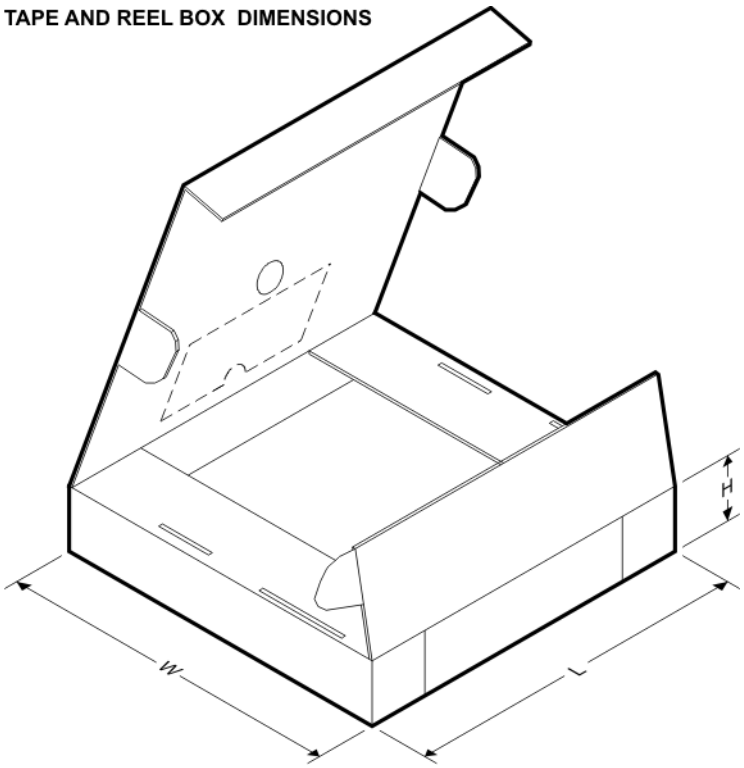
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

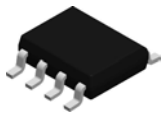
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4889MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM4889MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4889MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4889MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM4889MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM4889MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

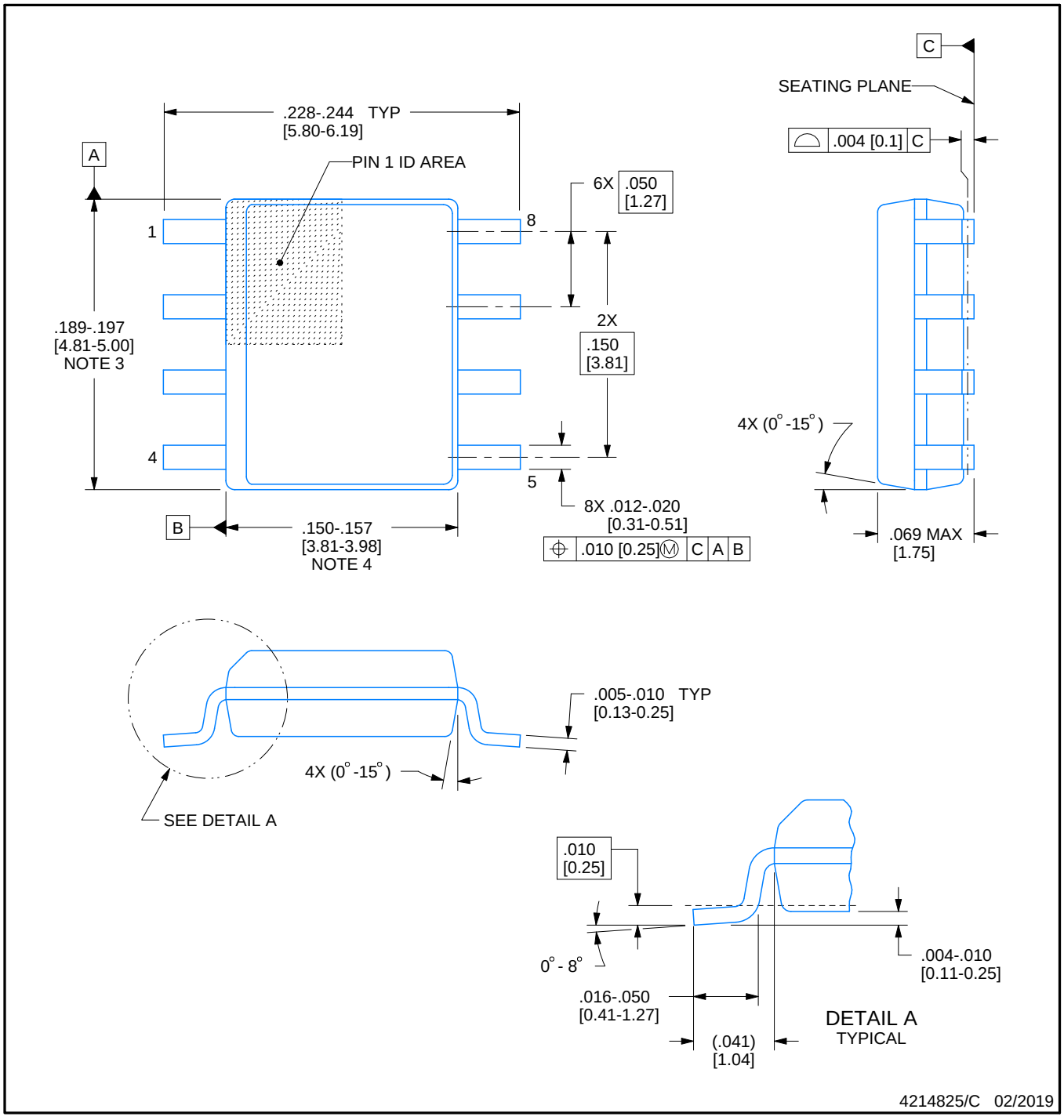


PACKAGE OUTLINE

D0008A

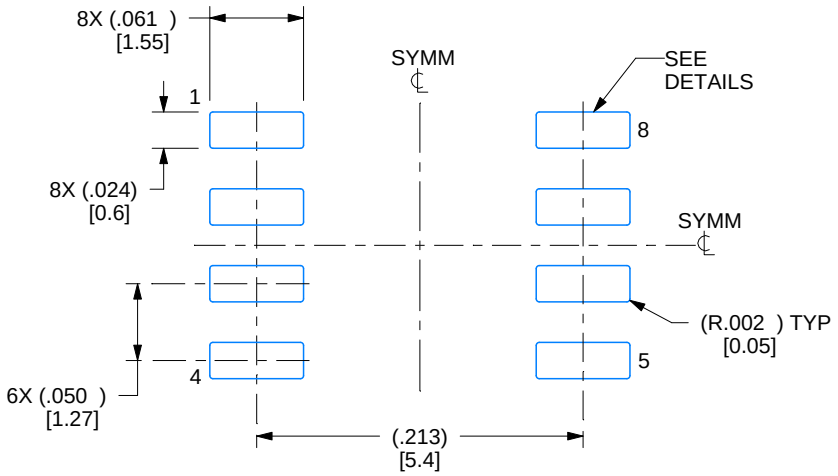
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

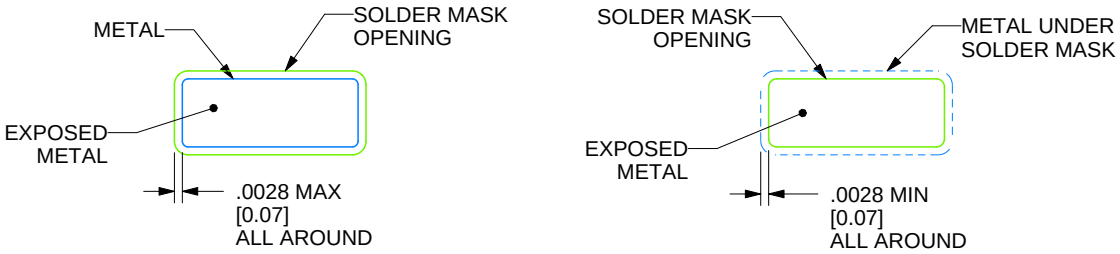


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

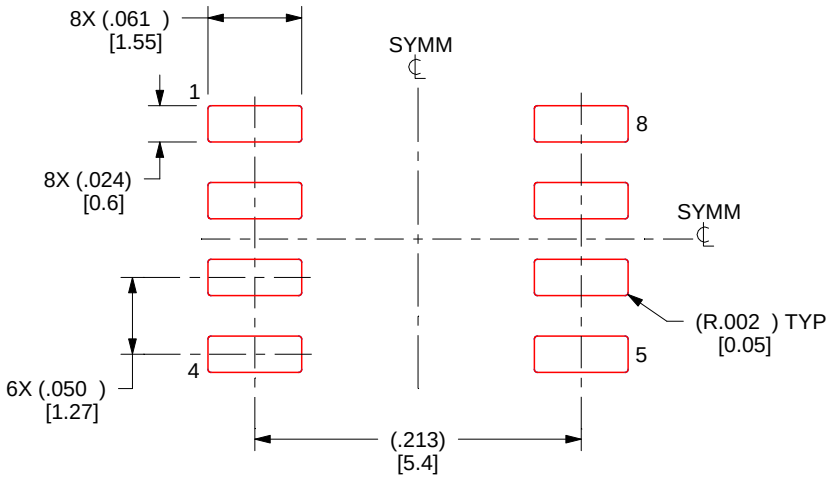
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



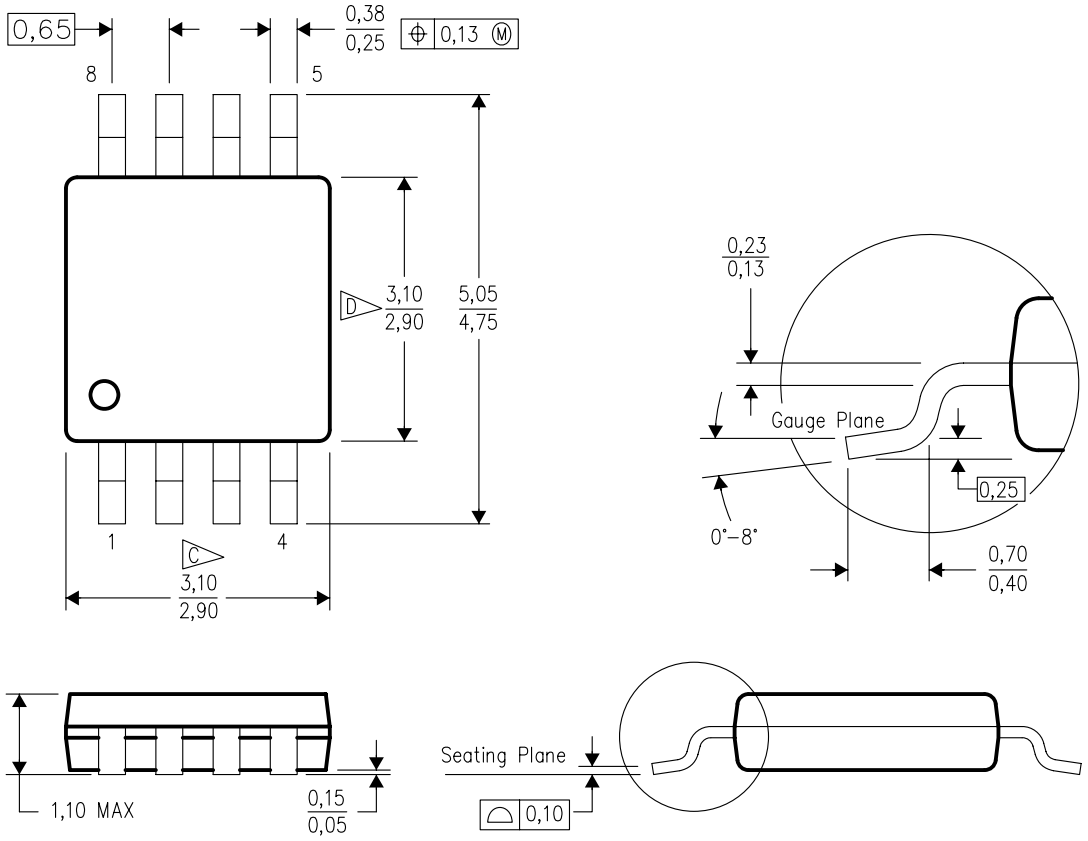
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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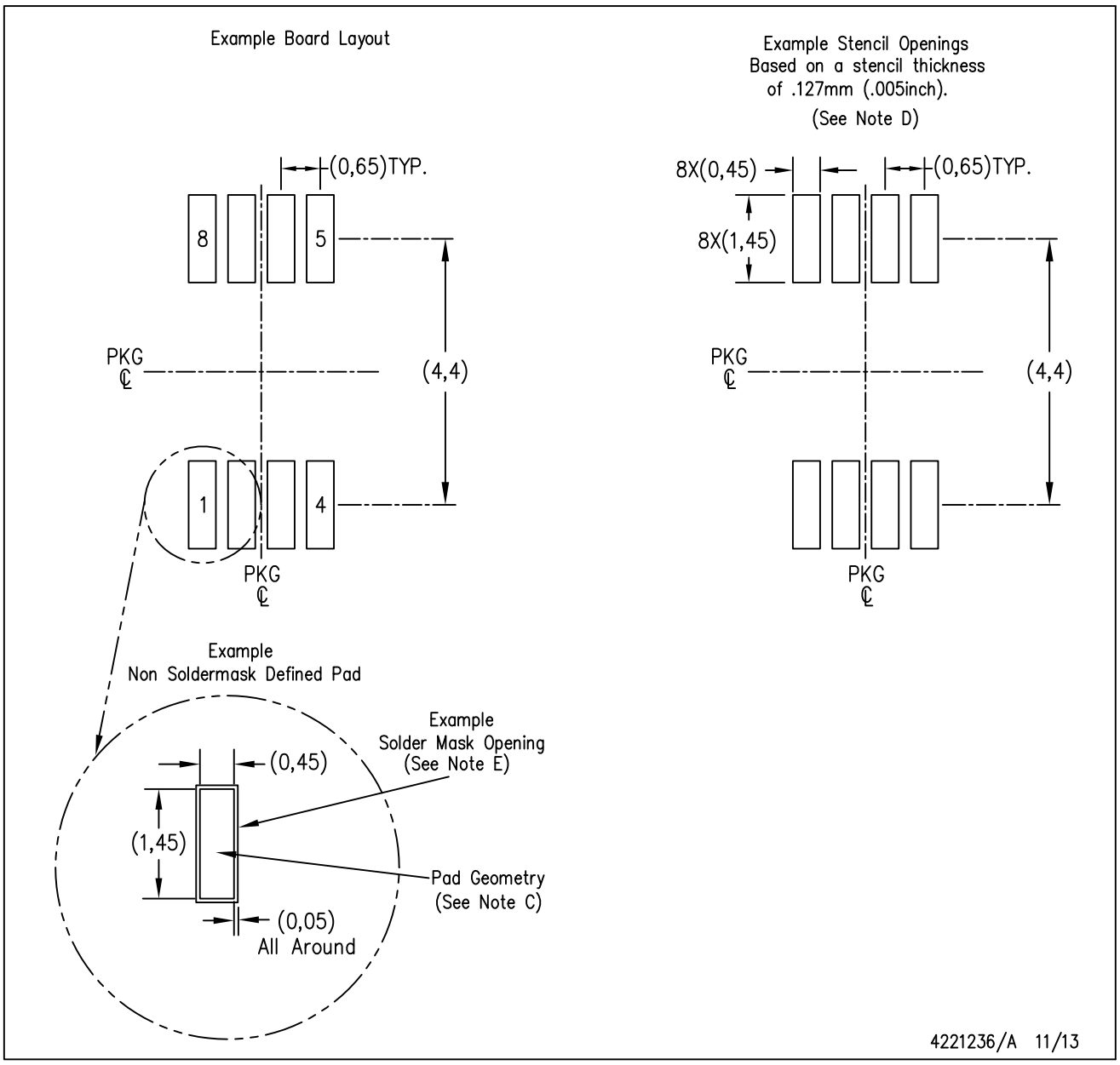
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265