AT34C02D

I²C-Compatible Serial Presence Detect (SPD) EEPROM with Permanent and Reversible Software Write Protection
2-Kbit (256 x 8)

DATASHEET

Features

- Single 1.7V to 5.5V V_{CC} Supply Voltage
- JEDEC EE1002 and EE1002A Serial Presence Detect (SPD) Compliant
  - EEPROM Specification for use in DDR, DDR2, and DDR3 DIMM Modules
- I²C-compatible (2-wire) Serial Interface
  - 400kHz (1.7V, 2.5V) and 1MHz (5.0V) Compatibility
- Multiple EEPROM Data Protection Schemes
  - Permanent and Reversible Software Write Protection for the Lower 128 bytes
  - Hardware Write Protection for the Entire Array
- Schmitt Trigger Filtered Inputs for Noise Suppression
- 16-byte Page Write Modes
  - Partial Page Writes are Allowed
- Self-timed Write Cycle (5ms maximum)
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- 8-pad 2x3mm UDFN, 8-lead TSSOP, 8-lead JEDEC SOIC, and 8-ball VFBGA Packages
- Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers are Available

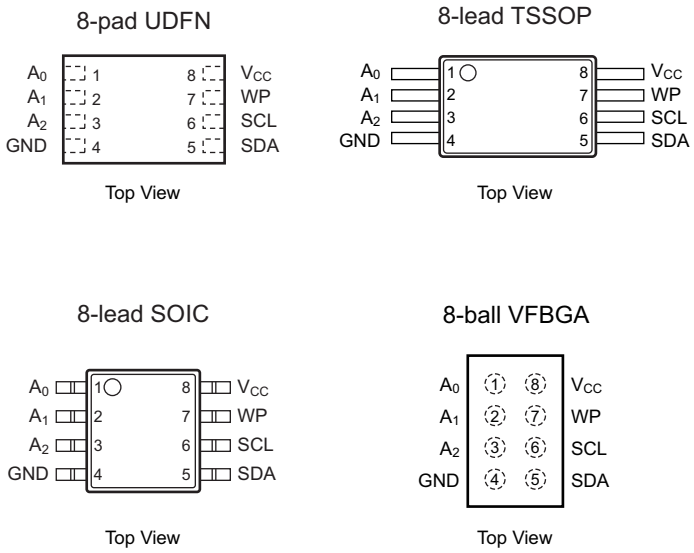
Description

The Atmel® AT34C02D is designed to support the JEDEC EE1002 and EE1002A Serial Presence Detect (SPD) function used in DDR, DDR2, and DDR3 Dual Inline Memory Modules (DIMM). The AT34C02D provides 2,048 bits of Serial Electrically-Erasable and Programmable Read Only Memory (EEPROM) organized as 256 words of 8 bits each. The device also incorporates a permanent and reversible software write protection feature for the lower 128 bytes of the EEPROM. Once the permanent software write protection is enabled, it cannot be reversed. However, the reversible software write protection can be enabled or disabled by sending a specific command and protocol sequence. A hardware write protection function is also available and is controlled by the WP pin state. It can be used to protect the entire EEPROM contents regardless of whether or not the software write protection has been enabled. The software and hardware write protection features allow the user the flexibility to protect none, lower-half, or the entire memory array depending on the specific needs of the application. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT34C02D is available in space saving 8-pad 2x3mm UDFN, 8-lead TSSOP, 8-lead JEDEC SOIC, and 8-ball VFBGA packages and is accessed via an I²C-compatible 2-wire serial interface. The AT34C02D operates over a wide V_{CC} range, from 1.7V to 5.5V.

1. Pin Configurations and Pinouts

Figure 1-1. Pin Configurations

Pin	Function
$A_0 – A_2$	Address Inputs
GND	Ground
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply



Note: Drawings are not to scale.

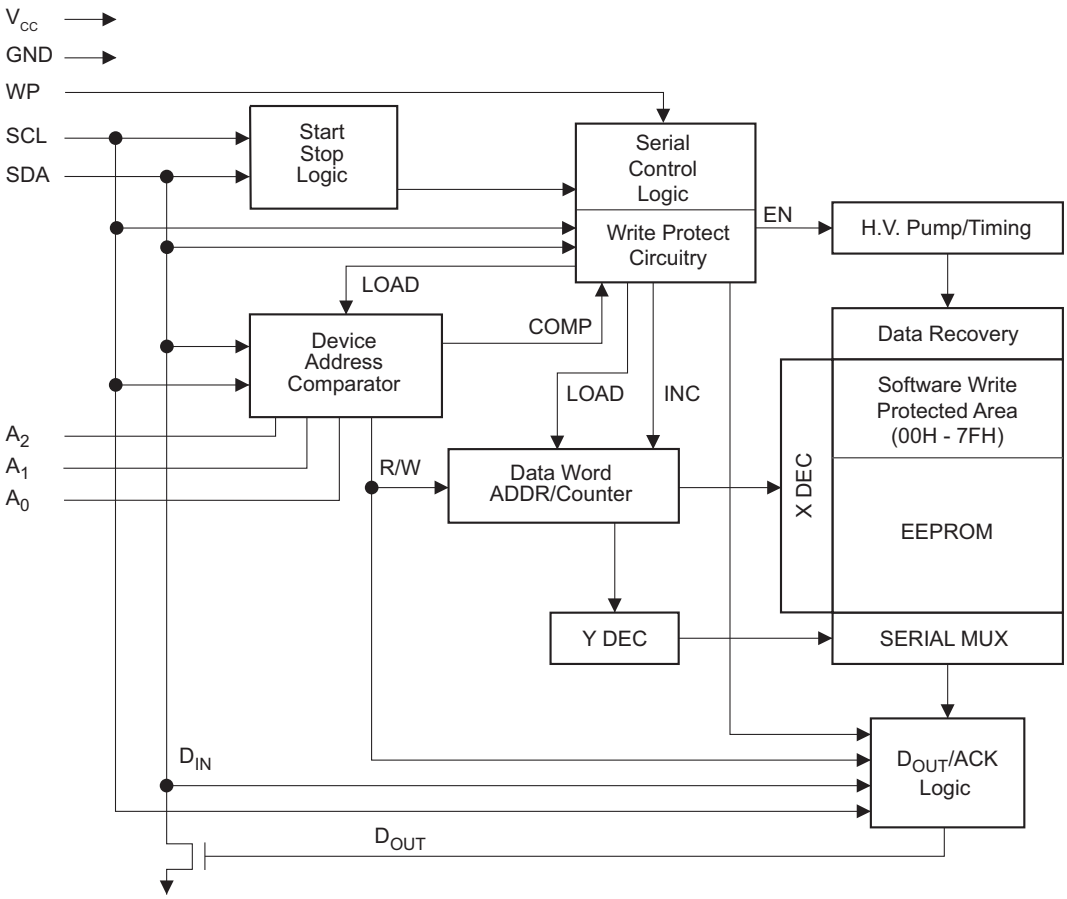
2. Memory Organization

2.1 AT34C02D, 2K Serial EEPROM:

The AT34C02D is internally organized with 16 pages of 16 bytes of EEPROM each. Random word addressing requires a 8-bit data word address.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

Device Addresses (A_2, A_1, and A_0): The A_2, A_1, and A_0 pins are device address inputs that are hardwired (directly to GND or to Vcc) for compatibility with other Atmel AT24Cxx devices. When the pins are hardwired, as many as eight 2K devices may be addressed on a single bus system. See Section 7. “Device Addressing” on page 9 for more details. A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Write Protect (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected directly to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Table 4-1. AT34C02D Write Protection Modes

WP Pin Status	Permanent Write Protect Register	Reversible Write Protect Register	Part of the Array Write Protected
V_{CC}	—	—	Full Array (00h – FFh)
GND or Floating	Programmed	—	Lower-half of Array (00h – 7Fh)
GND or Floating	—	Programmed	Lower-half of Array (00h – 7Fh)
GND or Floating	Not Programmed	Not Programmed	None, Normal Read/Write

5. Electrical Characteristics

5.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 400kHz, V_{CC} = 1.7V to 5.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$[1]	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}[1]	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

5.3 DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = 1.7V to 5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current V_{CC} = 5.0V	Read at 400kHz		1.0	2.0	mA
I_{CC2}	Supply Current V_{CC} = 5.0V	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}			3.0	µA
I_{SB3}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}, A_0 = V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

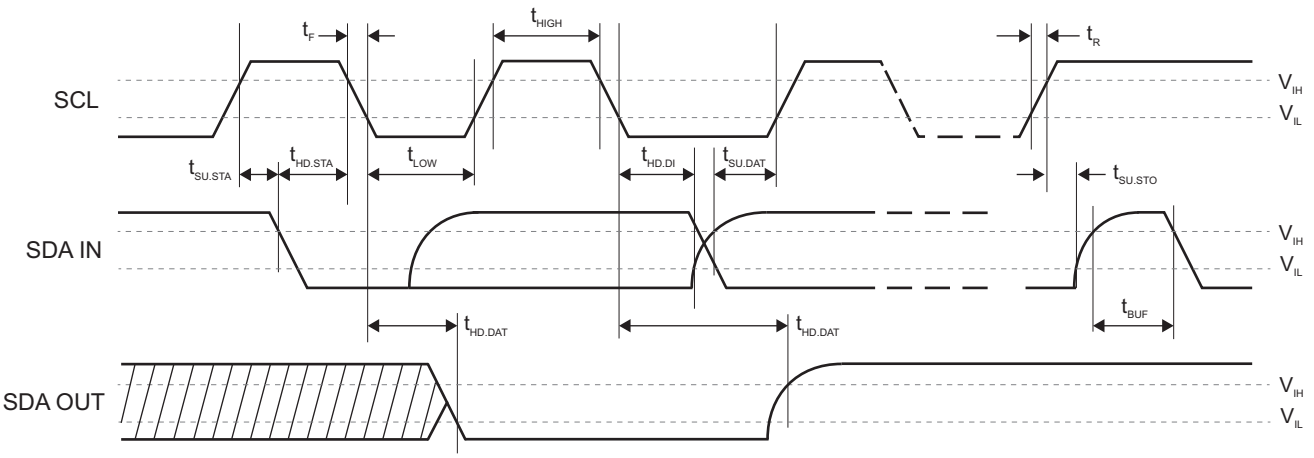
5.4 AC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C (unless otherwise noted).

		V_{CC} = 1.7 to 3.6V		V_{CC} = 1.7 to 3.6V		V_{CC} = 3.6V to 5.5V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{SCL}	Clock Frequency, SCL		100		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	4,700	—	1,300	—	400	—	ns
t_{HIGH}	Clock Pulse Width High	4,000	—	600	—	400	—	ns
t_R	Inputs Rise Time(1)	—	1000	—	300	—	100	ns
t_F	Inputs Fall Time(1)	—	300	—	300	—	100	ns
$t_{SU.DAT}$	Data in Set-up Time	250	—	100	—	100	—	ns
$t_{HD.DI}$	Data in Hold Time	0	—	0	—	0	—	ns
$t_{HD.DAT}$	Data Out Hold Time	200	3,450	200	900	50	550	ns
$t_{SU.STA}$	Start Condition Set-up Time	4,700	—	600	—	250	—	ns
$t_{HD.STA}$	Start Condition Hold Time	4,000	—	600	—	250	—	ns
$t_{SU.STO}$	Stop Condition Set-up Time	4,000	—	600	—	250	—	ns
t_I	Pulse Width of Spikes Suppressed, Single Glitch(1)	—	100	—	100	—	50	ns
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4,700	—	1,300	—	50	—	ns
t_{WR}	Write Cycle Time	—	5	—	5	—	5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1M	—	1M	—	1M	—	Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

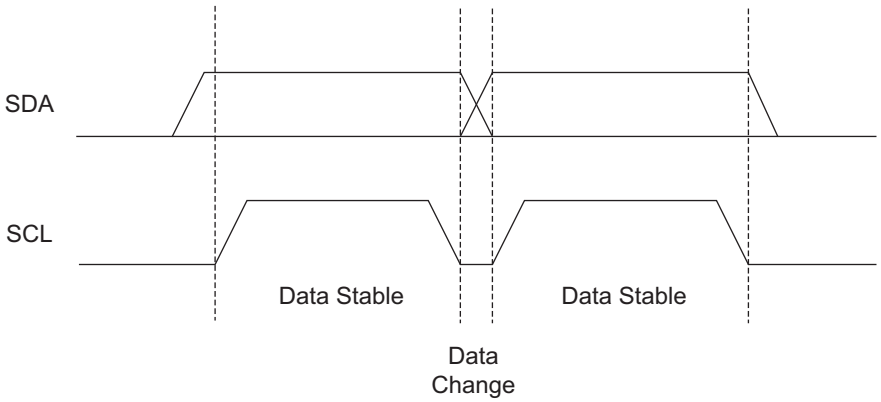
Figure 5-1. AC Timing Waveforms



6. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

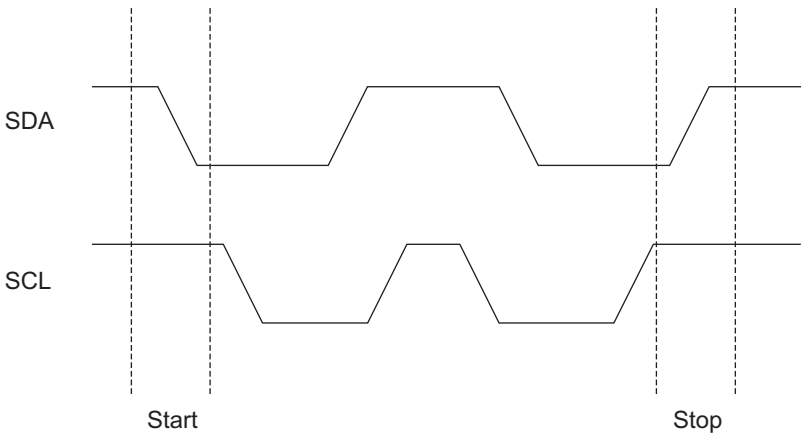
Figure 6-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

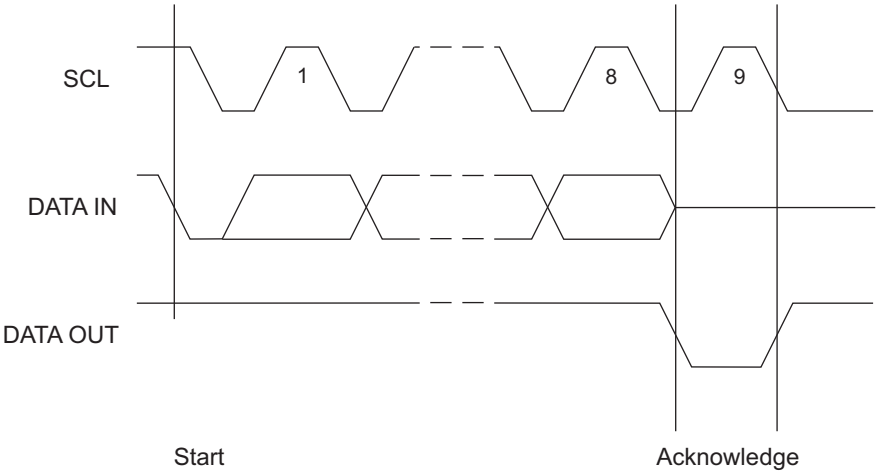
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode.

Figure 6-2. Start and Stop Condition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 6-3. Output Acknowledge



Standby Mode: The AT34C02D features a low-power standby mode which is enabled:

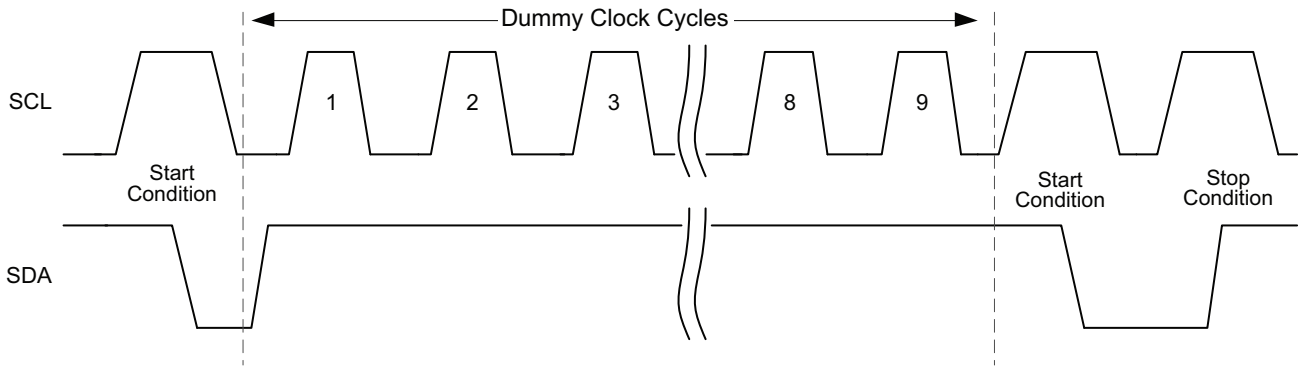
- Upon power-up or
- After the receipt of the Stop condition and the completion of any internal operations.

6.1 Memory Reset:

After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown below.

Figure 6-4. Software Reset



7. Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation.

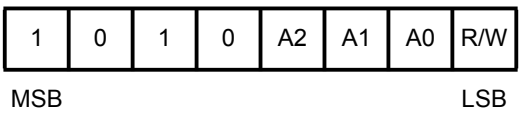
The device address word consists of a mandatory '1010' (Ah) sequence for the first four most-significant bits for normal read and write operations and '0110' (6h) for writing to the software write protect register.

The next three bits are the A_2, A_1, and A_0 device address bits. These three bits must match their corresponding hard-wired input pins in order for the part to acknowledge.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a successful compare of the device address, the EEPROM will acknowledge by outputting a zero. If a match is not made, the chip will return to a standby state. The device will not acknowledge if the write protect register has been programmed and the control code is '0110' (6h).

Figure 7-1. Device Address

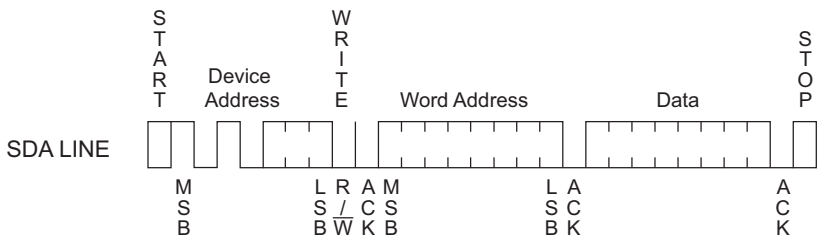


8. Write Operations

Byte Write: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again acknowledge or respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Figure 8-1. Byte Write



Page Write: The 2K device is capable of 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following data byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

Figure 8-2. Page Write

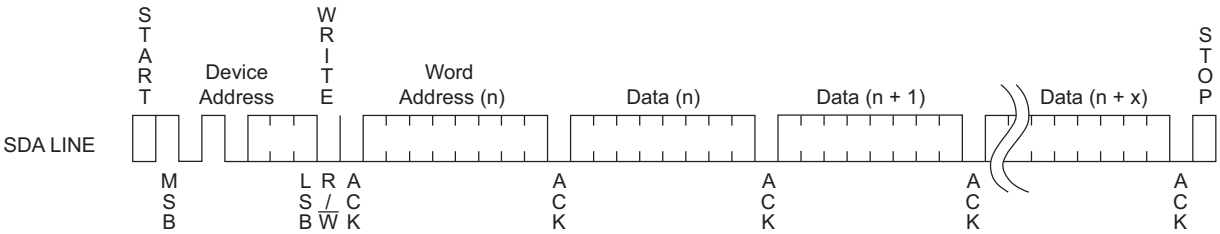
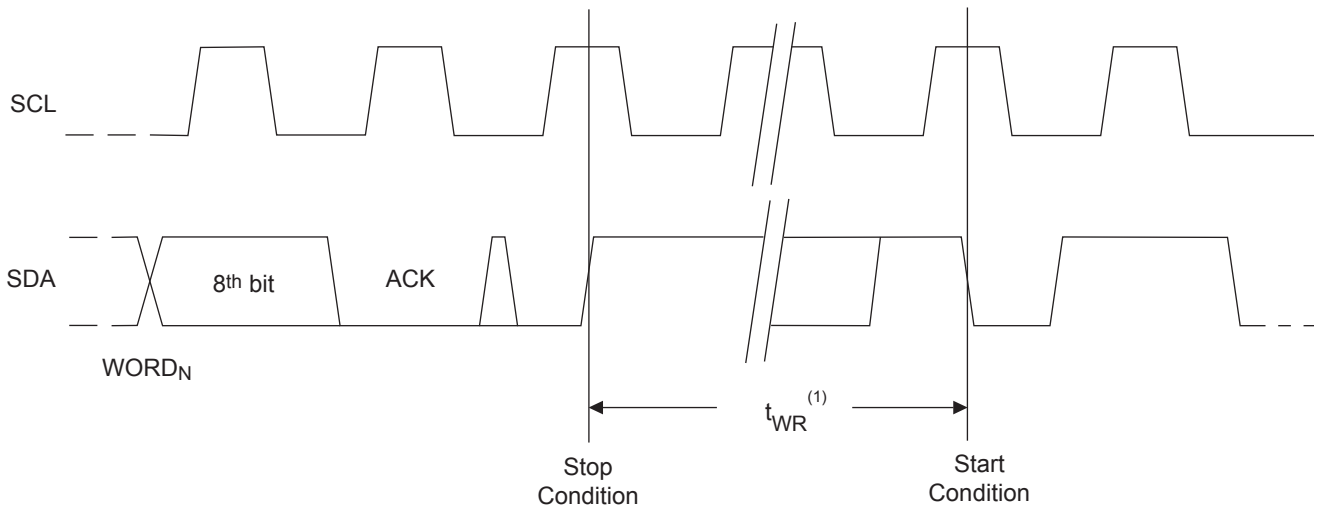


Figure 8-3. Write Cycle Timing



Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

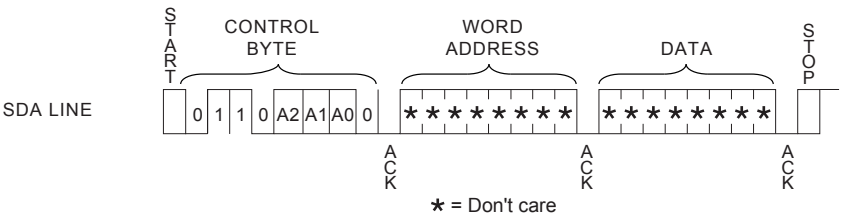
Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

8.1 Write Protection

The software write protection, once enabled, write protects only the lower-half of the array (addresses 0x00 – 0x7F) while the hardware write protection, via the WP pin, is used to protect the entire array.

Permanent Software Write Protection: The permanent software write protection is enabled by sending a command to the device, similar to a normal write command, which programs the permanent write protect register. This must be done with the WP pin low. The write protect register is programmed by sending a write command with the device address of '0110' (6h) instead of '1010' (Ah) with the address and data bit(s) being don't cares. Once the permanent software write protection has been enabled, the device will no longer acknowledge the '0110' (6h) control byte. The permanent software write protection cannot be reversed even if the device is powered down. The write cycle time must be observed.

Figure 8-4. Setting Permanent Write Protect Register (PSWP)



Reversible Software Write Protection: The reversible software write protection is enabled by sending a command to the device, similar to a normal write command, which programs the reversible write protect register. This must be done with the WP pin low. The reversible write protect register is programmed by sending a write command '01100010' (62h) with pins A_2 and A_1 tied to ground and pin A_0 connected to V_{HV} (see Figure 8-5). The reversible write protection can be reversed by sending a command '01100110' (66h) with pin A_2 tied to ground, pin A_1 tied to V_{CC} and pin A_0 tied to V_{HV} (see Figure 8-6).

Figure 8-5. Setting Reversible Write Protect Register (RSWP)

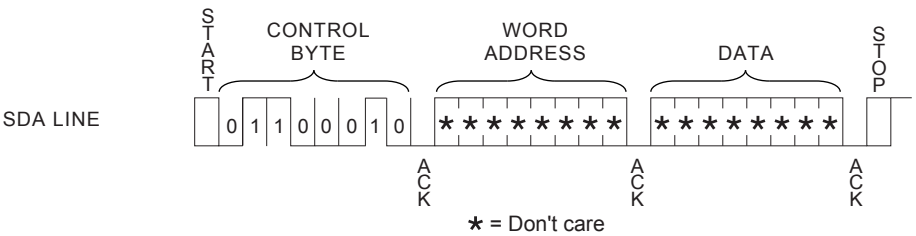
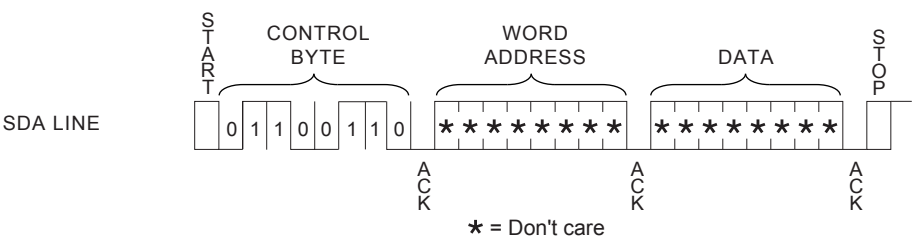


Figure 8-6. Clearing Reversible Write Protect Register (RSWP)



Hardware Write Protection: The WP pin can be connected to V_{CC}, GND, or left floating. Connecting the WP pin to V_{CC} will write protect the entire array, regardless of whether or not the software write protection has been enabled or invoked. The software write protection register cannot be programmed when the WP pin is connected to V_{CC}. If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the software write protect register.

Table 8-1. Write Protection

	Pin State/Voltage			Preamble							R/W
Command	**A_2**	**A_1**	**A_0**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Set PSWP	A_2	A_1	A_0	0	1	1	0	A_2	A1	A_0	0
Set RSWP	0	0	V_{HV}	0	1	1	0	0	0	1	0
Clear RSWP	0	V_{CC}	V_{HV}	0	1	1	0	0	1	1	0

Table 8-2. V_{HV}

	Min	Max	Units
V_{HV}	7	10	V

Note: $V_{HV} - V_{CC} > 4.8V$

Table 8-3. Device Response, WP Connected to GND or Floating

WP Connected to GND or Floating						
				Device Acknowledgement		
Command	Operation	Permanent Write Protect Register PSWP	Reversible Write Protect Register RSWP	Command/ Address Byte	Data Byte	Action from Device
1010	Read	X	X	ACK	X	Read Array
1010	Write to Upper 128 Bytes	Programmed	X	ACK	ACK	Can write to upper-half (80h – FFh) only.
1010	Write to Upper 128 Bytes	X	Programmed	ACK	ACK	Can write to upper-half (80h – FFh) only.
1010	Write to Lower 128 Bytes	Programmed	X	ACK	No ACK	Lower half is permanently write protected. No writing occurs.
1010	Write to Lower 128 Bytes	X	Programmed	ACK	No ACK	Lower half is write protected with the reversible protection features. No writing occurs.
1010	Write	Not Programmed	Not Programmed	ACK	ACK	Can write to Full Array.
Read PSWP	Read	Programmed	X	No ACK	X	STOP — Indicates permanent write protect register is programmed.
Read PSWP	Read	Not Programmed	X	ACK	X	Read out data undefined. Indicates PSWP register is not programmed
Set PSWP	Write	Programmed	X	No ACK	No ACK	STOP — Indicates permanent write protect register is programmed.
Set PSWP	Write	Not Programmed	X	ACK	ACK	Program permanent write protect register (irreversible).
Read RSWP	Read	X	Programmed	No ACK	X	STOP — Indicates reversible write protect register is programmed.
Read RSWP	Read	X	Not Programmed	ACK	X	Read out data undefined. Indicates RSWP register is not programmed
Set RSWP	Write	Not Programmed	Programmed	No ACK	No ACK	STOP — Indicates reversible write protect register is programmed.
Set RSWP	Write	Not Programmed	Not Programmed	ACK	ACK	Program reversible write protect register (reversible).
Set RSWP	Write	Programmed	X	No ACK	No ACK	STOP — Indicates permanent write protect register is programmed.
Clear RSWP	Write	Programmed	X	No ACK	No ACK	STOP — Indicates permanent write protect register is programmed.
Clear RSWP	Write	Not Programmed	X	ACK	ACK	Clear (unprogram) reversible write protect register (reversible).

Table 8-4. Device Response, WP Connected to V_{CC}

WP connected to V_{CC}						
				Device Acknowledgement		
Command	Read / Write Bit	Permanent Write Protect Register PSWP	Reversible Write Protect Register RSWP	Command/ Address Byte	Data Byte	Action from Device
1010	Read	X	X	ACK	X	Read Array
1010	Write	X	X	ACK	No ACK	Device is Write Protected, No writing occurs.
Read PSWP	Read	Programmed	X	No ACK	X	STOP — Indicates permanent write protect register is programmed.
Read PSWP	Read	Not Programmed	X	ACK	X	Read out data undefined. Indicates PSWP register is not programmed.
Set PSWP	Write	Programmed	X	No ACK	No ACK	STOP — Indicates permanent write protect register is programmed.
Set PSWP	Write	Not Programmed	X	ACK	No ACK	Cannot program write protect registers.
Read RSWP	Read	X	Programmed	No ACK	X	STOP — Indicates reversible write protect register is programmed.
Read RSWP	Read	X	Not Programmed	ACK	X	Read out data undefined. Indicates RSWP register is not programmed.
Set RSWP	Write	Not Programmed	Programmed	No ACK	No ACK	STOP — Indicates reversible write protect register is programmed.
Set RSWP	Write	Not Programmed	Not Programmed	ACK	No ACK	Cannot program write protect registers.
Set RSWP	Write	Programmed	X	No ACK	No ACK	STOP — Indicates permanent write protect register is programmed.
Clear RSWP	Write	Programmed	X	No ACK	No ACK	STOP — Indicates permanent write protect register is programmed.
Clear RSWP	Write	Not Programmed	X	ACK	No ACK	Cannot write to write protect registers.

9. Read Operations

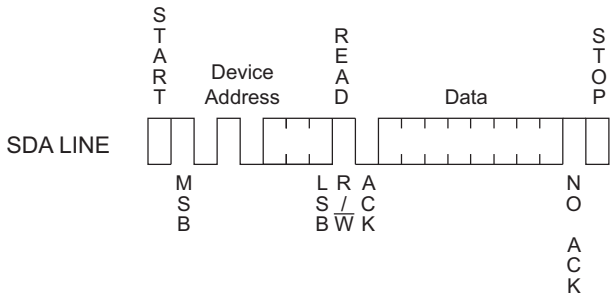
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page.

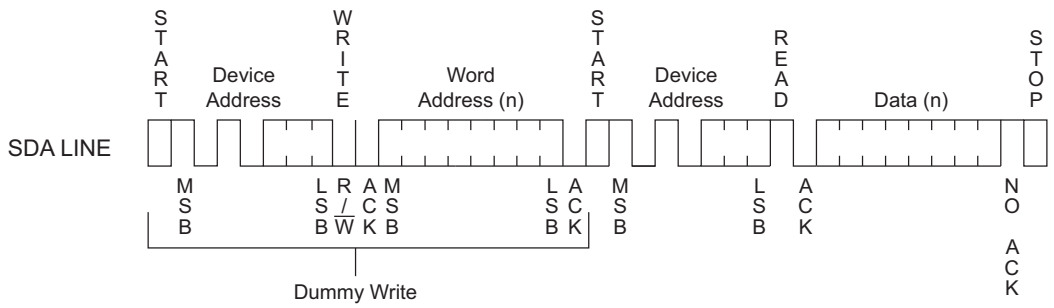
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end the command, the microcontroller does not respond with a zero but does generate a stop condition in the subsequent clock cycle.

Figure 9-1. Current Address Read



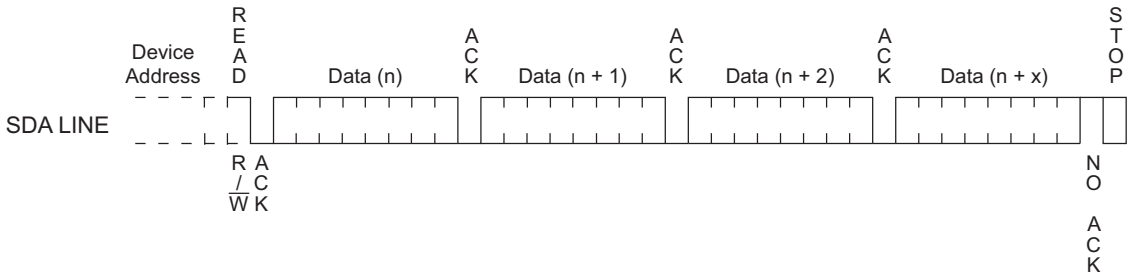
Random Read: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the command, the microcontroller does not respond with a zero but does generate a stop condition in the subsequent clock cycle.

Figure 9-2. Random Read



Sequential Read: Sequential Reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll-over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a stop condition in the subsequent clock cycle.

Figure 9-3. Sequential Read



Permanent Write Protect Register (PSWP) Status: Determining the status of the permanent write protect register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/W bit must now be set to a one. If the device returns an acknowledge, the permanent write protect register has not been programmed. Otherwise, it has been programmed and the lower-half of the array is permanently write protected.

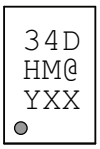
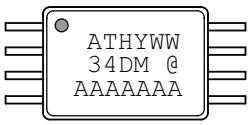
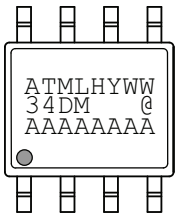
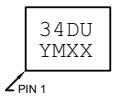
Reversible Write Protect Register (RSWP) Status: Determining the status of the reversible write protect register can be accomplished by sending a similar command to the device as was used when programming the register, except the R/W bit must be set to one. If the device returns an acknowledge, then the reversible write protect register has been programmed. The lower-half of the array is write protected, but remains reversible.

Table 9-1. PSWP and RSWP Status

	Pin State/Voltage			Preamble							R/W
Command	**A_2**	**A_1**	**A_0**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Read PSWP	A_2	A_1	A_0	0	1	1	0	A_2	A_1	A_0	1
Read RSWP	0	0	A_0	0	1	1	0	0	0	1	1

10. Part Markings

AT34C02D: Package Marking Information

8-lead UDFN	8-lead TSSOP
2.0 x 3.0 mm Body 	
8-lead SOIC	**8-ball VFBGA**
	1.5 x 2.0 mm Body 

Note 1: ● designates pin 1

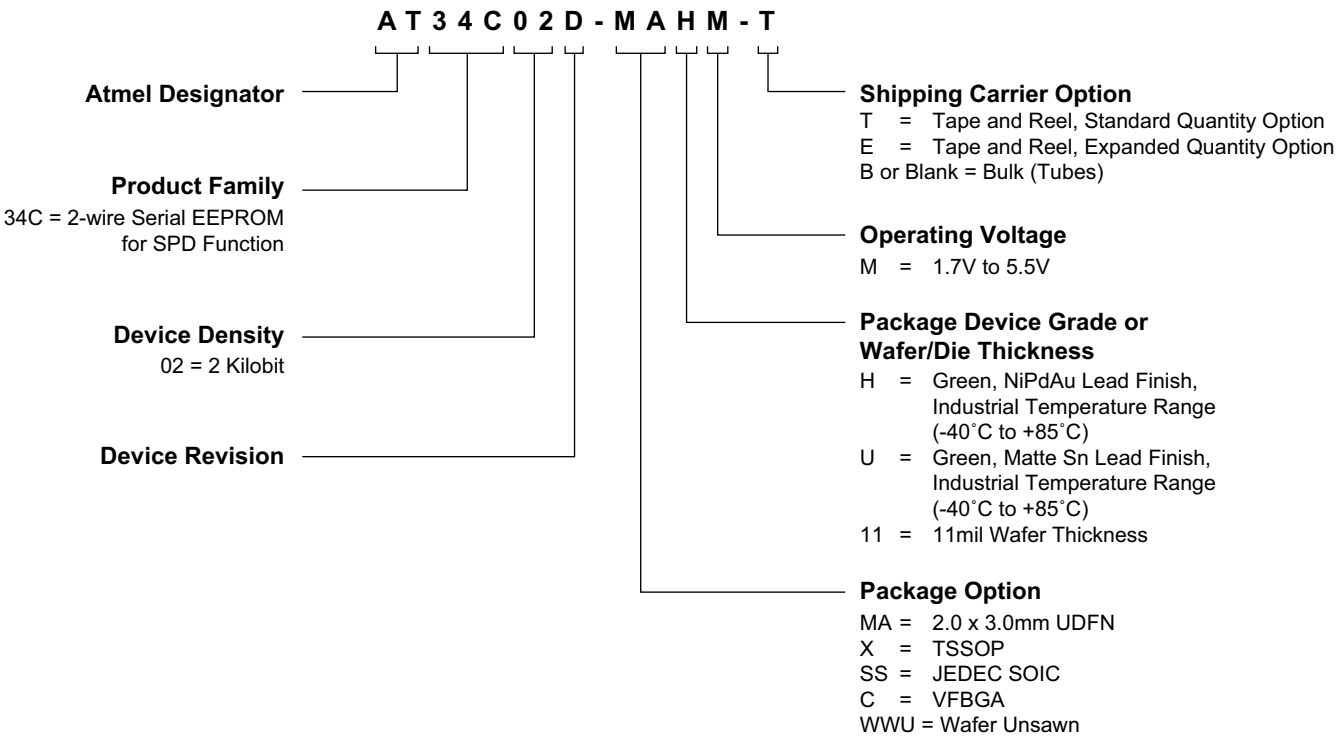
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT34C02D		Truncation Code ###: 34D	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	M: 1.7V min
4: 2014 8: 2018 5: 2015 9: 2019 6: 2016 0: 2020 7: 2017 1: 2021	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		H: Industrial/NiPdAu U: Industrial/Matte Tin
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

5/12/14

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	34C02DSM, AT34C02D Package Marking Information	34C02DSM	D

11. Ordering Code Detail



12. Ordering Information

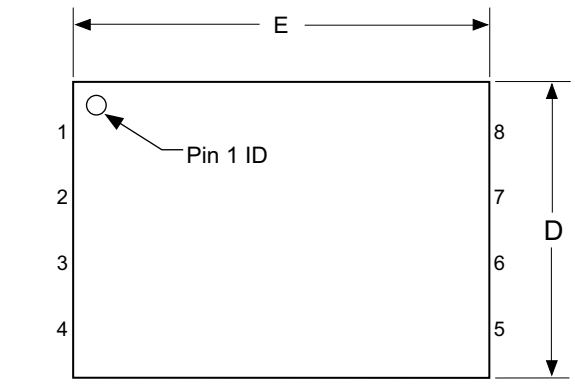
Atmel Ordering Code	Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT34C02D-MAHM-T	NiPdAu (Lead-free/Halogen-free)	8MA2	Tape and Reel	5,000 per Reel	Industrial Temperature (-40°C to +85°C)
AT34C02D-MAHM-E			Tape and Reel	15,000 per Reel	
AT34C02D-XHM-T		8X	Tape and Reel	5,000 per Reel	
AT34C02D-XHM-B			Bulk (Tubes)	100 per Tube	
AT34C02D-SSHM-T		8S1	Tape and Reel	4,000 per Reel	
AT34C02D-SSHM-B			Bulk (Tubes)	100 per Tube	
AT34C02D-CUM-T	Matte Tin (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT34C02D-WWU11M(1)	N/A	Wafer Sale	Note 1		

Note: 1. For Wafer sales, please contact Atmel Sales.

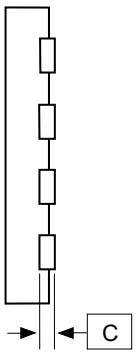
Package Type	
8MA2	8-pad, 2.0mm x 3.0mm, 0.6mm body, Ultra Thin Dual Flat No Lead (UDFN)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8S1	8-lead, 0.150" wide body, Plastic Gull Wing Small Outline (JEDEC SOIC)
8U3-1	8-ball, 1.5mm x 2.0mm body, 0.5mm pitch, die Ball Grid Array (VFBGA)

13. Packaging Information

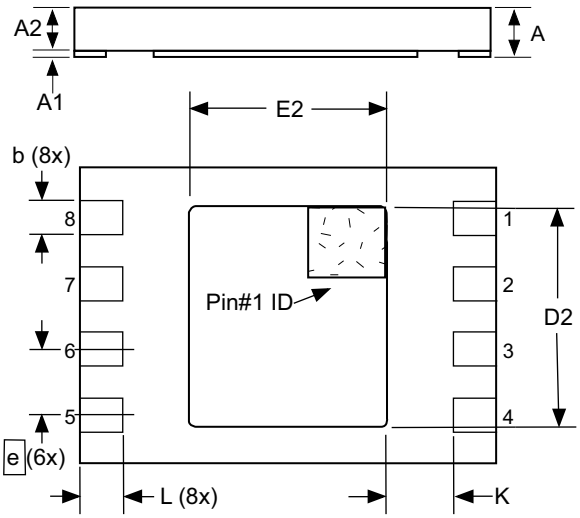
13.1 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

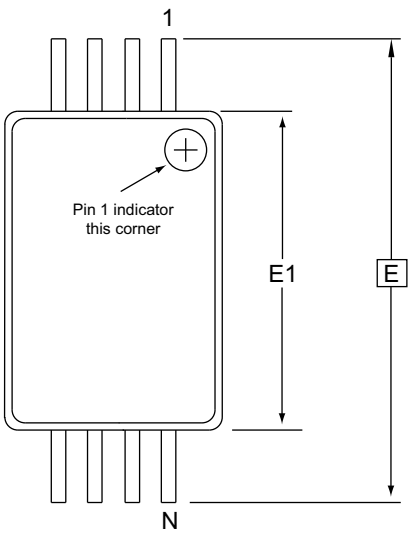
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
K	0.20	-	-	

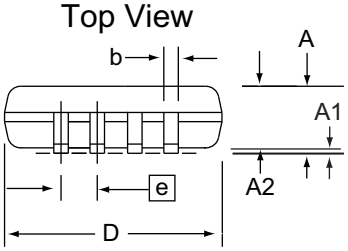
11/26/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** G

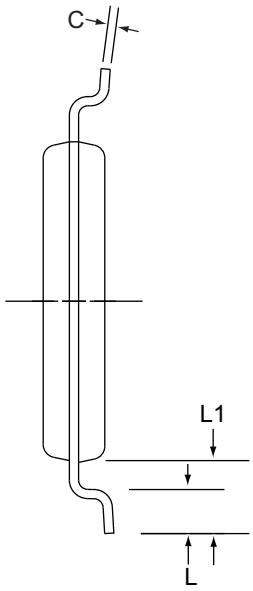
13.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

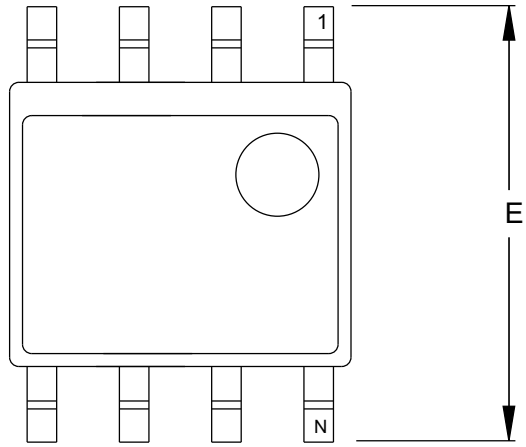
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

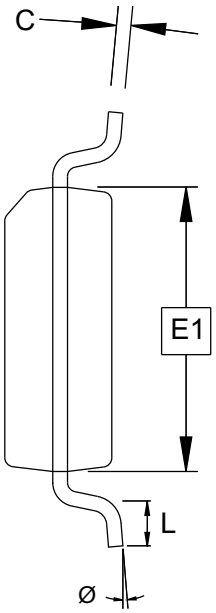
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

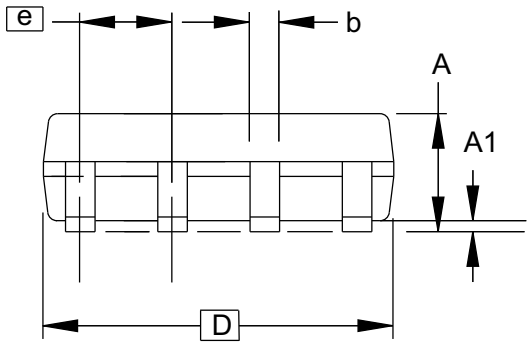
13.3 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

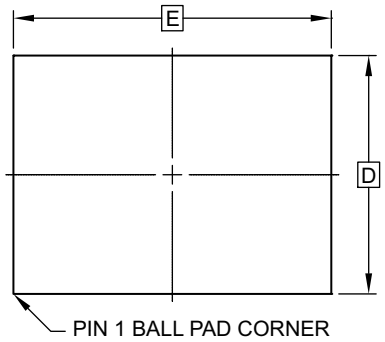
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

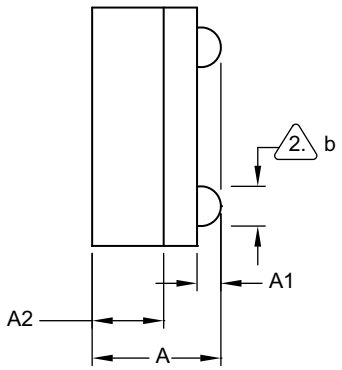
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

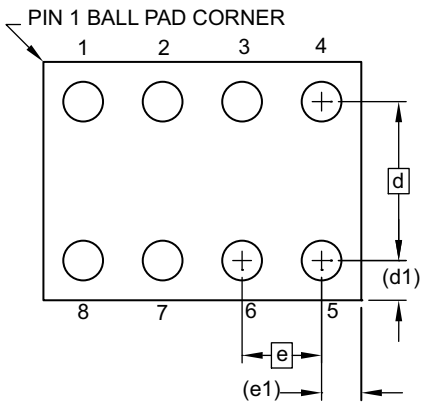
13.4 8U3-1 — 8-ball VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

6/11/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GPC GXU	DRAWING NO. 8U3-1	REV. F

14. Revision History

Doc. Rev.	Date	Comments
8781D	01/2015	Added the UDFN extended quantity option. Updated the ordering information section and the 8MA2 package outline drawing.
8781C	07/2014	Updated various language elements for consistency with JEDEC EE1002/1002A. Updated AC timing terminology for consistency with JEDEC EE1002/1002A. Added 100kHz timing information for SPD applications using < 2.2V V_{CC} supply. Miscellaneous formatting changes and text corrections. Update package drawings.
8781B	06/2012	Correct ordering code: - AT34C02D-WWU11, Die Sale to AT34C02D-WWU11M, Wafer Sale. Update template.
8781A	03/2012	Initial document release.

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