MCP616/617/618/619

2.3V to 5.5V Micropower Bi-CMOS Op Amps

FEATURES

- Low Power: I_{DD} = 25 µA, max
- Low Offset Voltage: 150 µV, max
- Rail-to-Rail Swing at Output
- Low Input Offset Current: 0.3 nA, typical
- Specifications rated for 2.3V to 5.5V Supplies
- Unity Gain Stable
- Chip Select ($\overline{CS}$) Capability with MCP618
- Industrial Temperature range supported
- No Phase Reversal
- Available in Single, Dual, and Quad

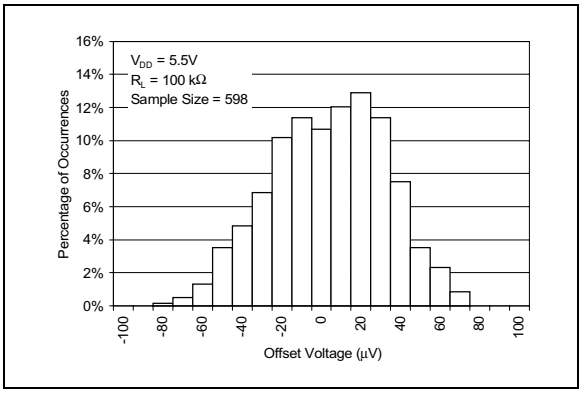
APPLICATIONS

- Battery Powered Instruments
- Strain Gauges
- Medical Instruments
- Test Equipment

AVAILABLE TOOLS

- Spice Macromodels (at www.microchip.com)
- FilterLab™ Software (at www.microchip.com)

HISTOGRAM OF INPUT OFFSET VOLTAGE



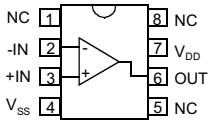
DESCRIPTION

The MCP616, MCP617, MCP618 and MCP619 from Microchip Technology, Inc. are unity gain stable, low offset voltage operational amplifiers capable of precision low power single supply operation. Performance characteristics include ultra low offset voltage (150 µV, max.), rail-to-rail output swing capability, and low input offset current (0.3 nA typ.). These features make this family of amplifiers well suited for single supply precision, high impedance, battery powered applications.

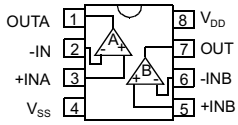
The single MCP616 is available in standard 8-lead PDIP, SOIC, and MSOP packages. Another version of the single op amp, MCP618 is offered with a Chip Select ($\overline{CS}$) option in standard 8-lead PDIP, SOIC, and MSOP packages. The dual MCP617 is offered in standard 8-lead PDIP, SOIC, as well as the MSOP package. Finally, the quad MCP619 is offered in 14-lead PDIP, SOIC and TSSOP packages. All devices are fully specified from -40°C to +85°C with power supplies from 2.3V to 5.5V.

PACKAGES

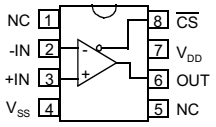
MCP616
PDIP, SOIC, MSOP



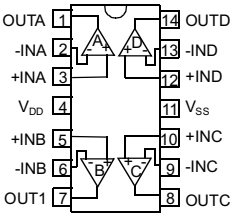
MCP617
PDIP, SOIC, MSOP



MCP618
PDIP, SOIC, MSOP



MCP619
PDIP, SOIC,TSSOP



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings†

V_{DD}.....7.0V
All inputs and outputs w.r.t. .. V_{SS} –0.3V to V_{DD} +0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-55°C to +125°C
ESD protection on all pins (HBM)..... ≥ 4 kV

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
+IN/+INA/+INB/+INC/+IND	Non-inverting Input Terminals
-IN/-INA/-INB/-INC/-IND	Inverting Input Terminals
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
OUT/OUTA/OUTB/OUTC/OUTD	Output Terminals
$\overline{CS}$	Chip Select
NC	No internal connection to IC

DC CHARACTERISTICS

Unless otherwise specified, all limits are specified for V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25 °C, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2

PARAMETERS	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
INPUT OFFSET						
Input Offset Voltage	V_{OS}	-150	—	+150	µV	
Drift with Temperature	dV_{OS}/dT	—	±2	—	µV/°C	T_A= -40°C to +85°C
Power Supply Rejection	PSRR	86	105	—	dB	
INPUT BIAS CURRENT AND IMPEDANCE						
Input Bias Current	I_B	-35	-15	-5	nA	
Over Temperature	I_B	-70	—	—	nA	T_A= -40°C to +85°C
Input Offset Bias Current	I_{OS}	—	±0.3	—	nA	
Common Mode Input Impedance	Z_{CM}	—	600||4	—	MΩ||pF	
Differential Input Impedance	Z_{DIFF}	—	3||2	—	MΩ||pF	
COMMON MODE						
Common-Mode Input Range	CMR	V_{SS}		V_{DD}–0.9	V	
Common-Mode Rejection Ratio	CMRR	80	100	—	dB	V_{DD} = 5V, V_{CM} = 0.0 to 4.1V
OPEN LOOP GAIN						
DC Open Loop Gain	A_{OL}	100	120	—	dB	R_L = 25 kΩ to V_{DD}/2, 50 mV < V_{OUT} < (V_{DD} – 50 mV)
DC Open Loop Gain	A_{OL}	95	115	—	dB	R_L = 5 kΩ to V_{DD}/2, 100 mV < V_{OUT} < (V_{DD} – 100 mV)
OUTPUT						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 0.015	—	V_{DD} – 0.020	V	R_L = 25 kΩ to V_{DD}/2
	V_{OL}, V_{OH}	V_{SS} + 0.045	—	V_{DD} – 0.060	V	R_L = 5 kΩ to V_{DD}/2
Linear Region Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 0.050	—	V_{DD} – 0.050	V	R_L = 25 kΩ to V_{DD}/2, A_{OL} ≥ 100 dB
	V_{OL}, V_{OH}	V_{SS} + 0.100	—	V_{DD} – 0.100	V	R_L = 5 kΩ to V_{DD}/2, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_{SC}		±17		mA	V_{OUT} = 2.75V, V_{DD} = 5.5V
POWER SUPPLY						
Supply Voltage	V_S	2.3	—	5.5	V	
Quiescent Current Per Amplifier	I_Q	12	19	25	µA	I_O = 0

AC CHARACTERISTICS

Unless otherwise specified, all limits are specified for V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, and V_{OUT} ~ V_{DD}/2

PARAMETERS	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Gain Bandwidth Product	GBWP	—	190	—	kHz	G = 1, V_{DD} = 5V, C_L = 60 pF
Phase Margin at Unity Crossing	θ	—	57	—	degrees	G = 1, V_{DD} = 5V, C_L = 60 pF
Slew Rate	SR	—	0.08	—	V/µs	G = 1, V_{DD} = 5V, C_L = 60 pF
Input Voltage Noise	E_n	—	2.2	—	µVp-p	f = 0.1 Hz to 10 Hz
Noise Density	e_n	—	32	—	nV/√Hz	f ≥ 1 kHz
Input Current Noise Density	i_n	—	70	—	fA/√Hz	f ≥ 1 kHz

SPECIFICATIONS FOR MCP618 CHIP SELECT ($\overline{CS}$) FEATURE

Unless otherwise specified, all limits are specified for V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, R_L = 100 kΩ, and V_{OUT} ~ V_{DD}/2

PARAMETERS	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$\overline{CS}$ LOW SPECIFICATIONS						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	For entire V_{DD} range
$\overline{CS}$ Input Current, Low	I_{CSL}	-1.0	0.01	—	µA	$\overline{CS}$ = 0.2V_{DD}
$\overline{CS}$ HIGH SPECIFICATIONS						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	For entire V_{DD} range
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.01	2	µA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current	I_Q	—	0.05	2	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage, $\overline{CS}$ High		—	0.01	—	µA	$\overline{CS}$ = 0.8V_{DD}
DYNAMIC SPECIFICATIONS						
$\overline{CS}$ Low to Amplifier Output High Turn-on Time	t_{ON}	—	9	100	µs	$\overline{CS}$ low = 0.2V_{DD}, V_{OUT} = 0.9 *V_{DD}/2, G = +1V/V
$\overline{CS}$ High to Amplifier Output High Z	t_{OFF}	—	0.1	—	µs	$\overline{CS}$ high = 0.8V_{DD}, V_{OUT} = 0.1 *V_{DD}/2, G = +1V/V
Hysteresis		—	0.6	—	V	V_{DD} = 5V

TEMPERATURE SPECIFICATIONS

Unless otherwise specified, all limits are specified for V_{DD} = +2.3V to +5.5V, V_{SS} = GND

PARAMETERS	SYM.	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TEMPERATURE RANGES						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
THERMAL PACKAGE RESISTANCE						
Thermal Resistance, 8L-PDIP	$θ_{JA}$	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	$θ_{JA}$	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	$θ_{JA}$	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	$θ_{JA}$	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	$θ_{JA}$	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	$θ_{JA}$	—	100	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: Unless otherwise indicated, $T_A = 25^\circ C$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, V_{SS} = GND

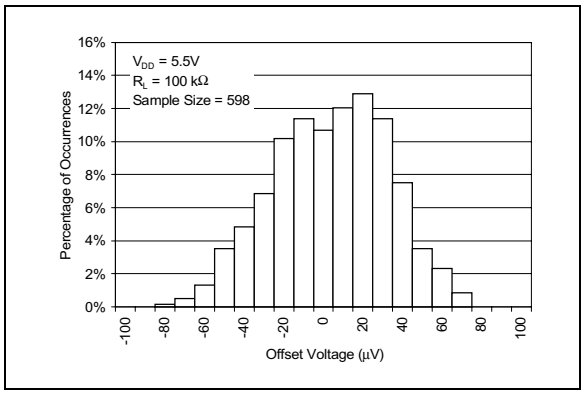


FIGURE 2-1: *Histogram of Offset Voltage with V_{DD} = 5.5V.*

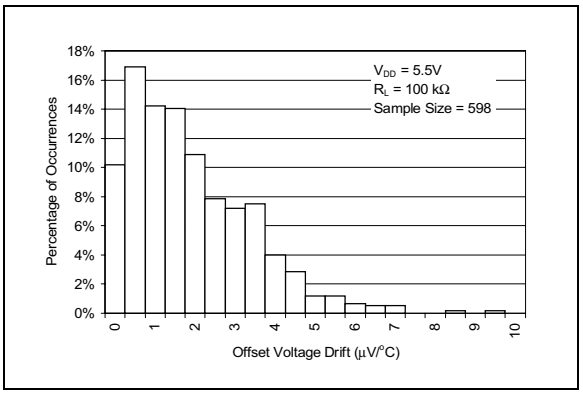


FIGURE 2-4: *Histogram of Offset Voltage Drift with V_{DD} = 5.5V.*

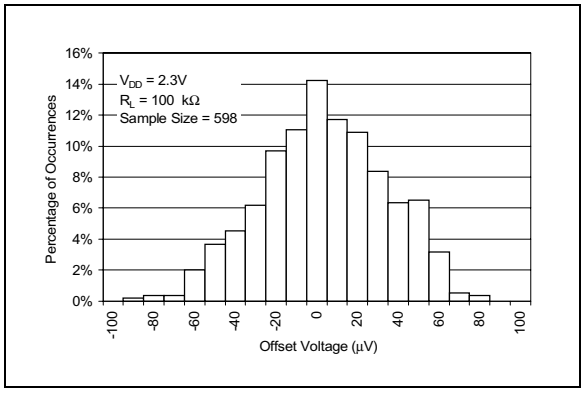


FIGURE 2-2: *Histogram of Offset Voltage with V_{DD} = 2.3V.*

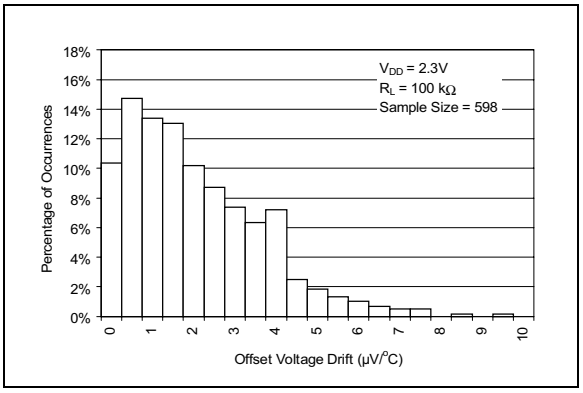


FIGURE 2-5: *Histogram of Offset Voltage Drift with V_{DD} = 2.3V.*

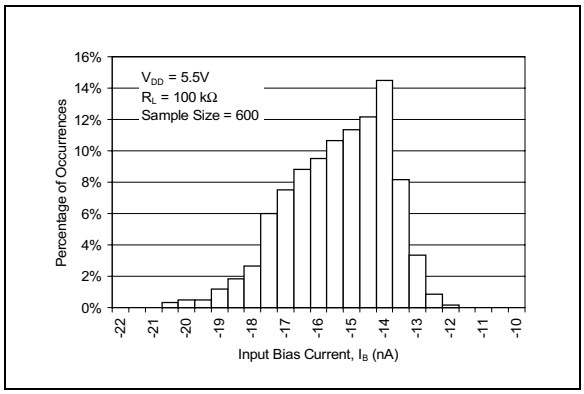


FIGURE 2-3: *Histogram of Input Bias Current with V_{DD} = 5.5V.*

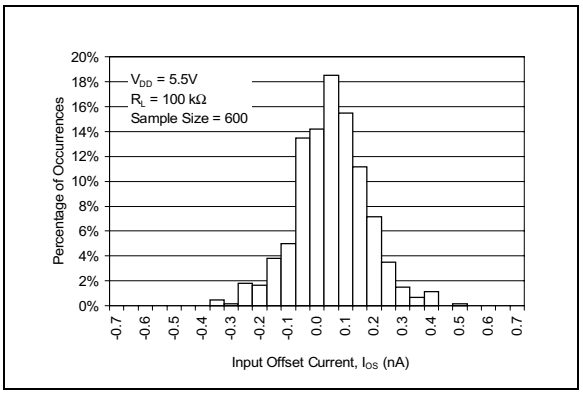


FIGURE 2-6: *Histogram of Input Offset Current with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, $T_A = 25°C$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, V_{SS} = GND

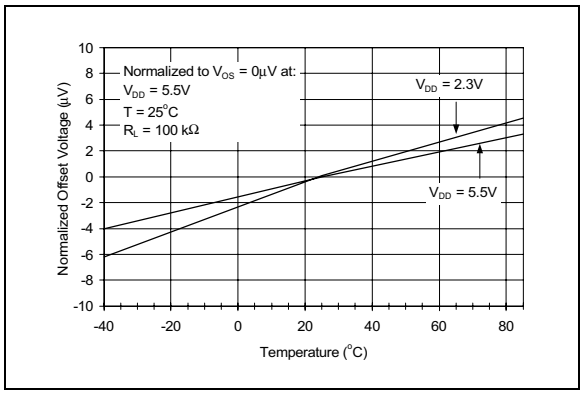


FIGURE 2-7: *Normalized Offset Voltage vs. Temperature.*

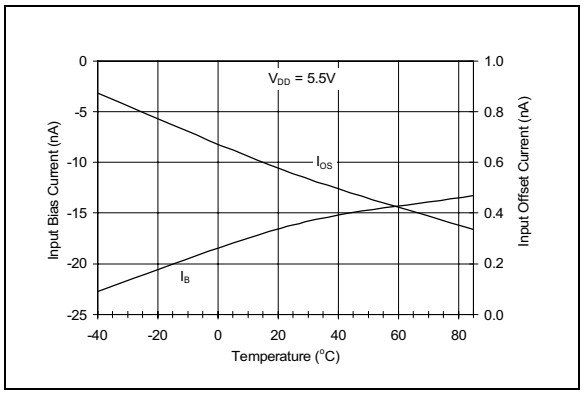


FIGURE 2-10: *Input Bias Current, Input Offset Current vs. Temperature.*

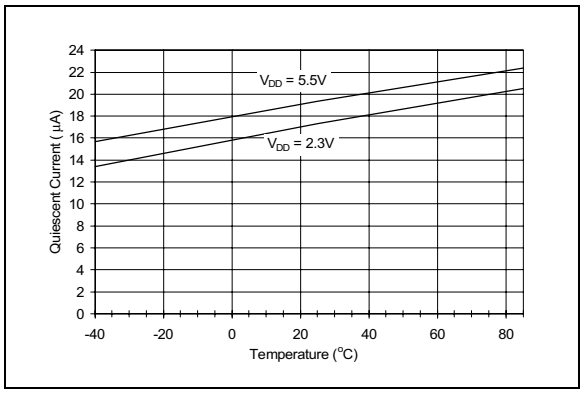


FIGURE 2-8: *Quiescent Current vs. Temperature vs. Power Supply Voltage.*

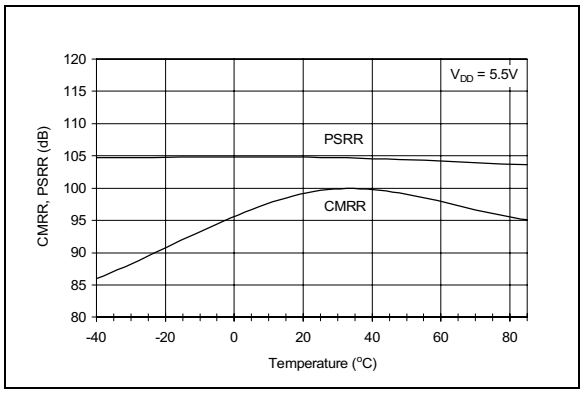


FIGURE 2-11: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.*

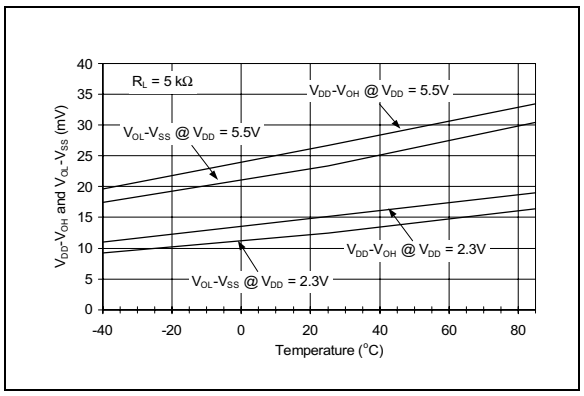


FIGURE 2-9: *Maximum Output Voltage Swing vs. Temperature with R_L = 5 kΩ.*

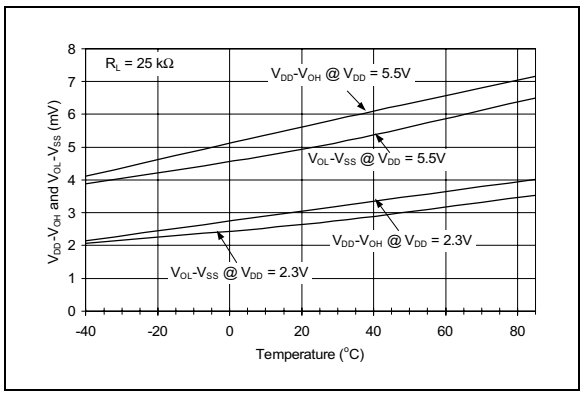


FIGURE 2-12: *Maximum Output Voltage Swing vs. Temperature with R_L = 25 kΩ.*

Note: Unless otherwise indicated, $T_A = 25^\circ C$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, V_{SS} = GND

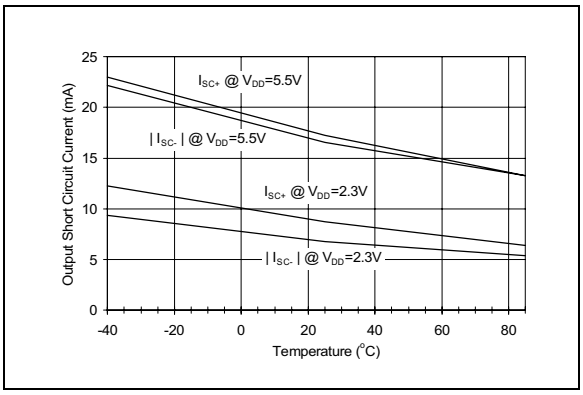


FIGURE 2-13: *Output Short Circuit Current vs. Temperature vs. Power Supply Voltage.*

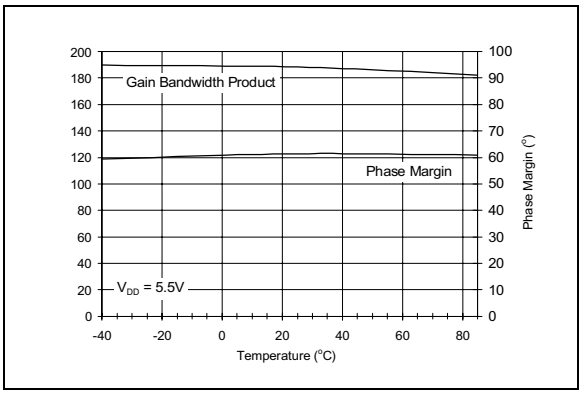


FIGURE 2-16: *Gain Bandwidth Product, Phase Margin vs. Temperature.*

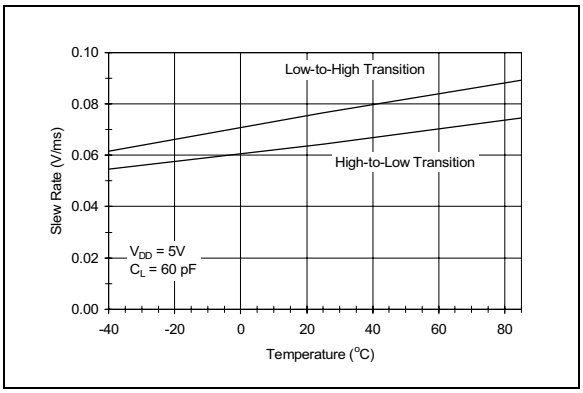


FIGURE 2-14: *Slew Rate vs. Temperature.*

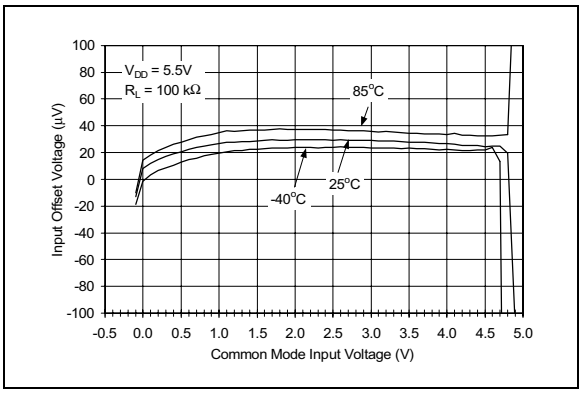


FIGURE 2-17: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature.*

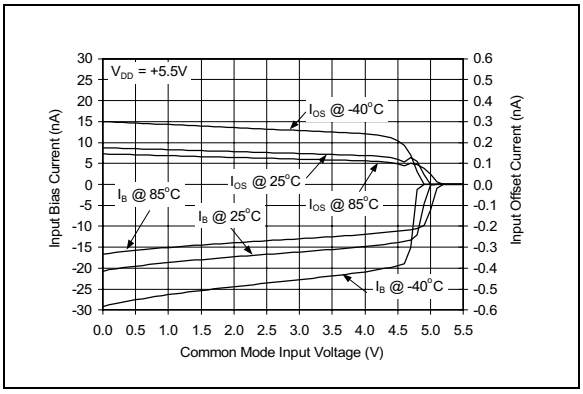


FIGURE 2-15: *Input Bias and Offset Current vs. Common Mode Input Voltage vs. Temperature.*

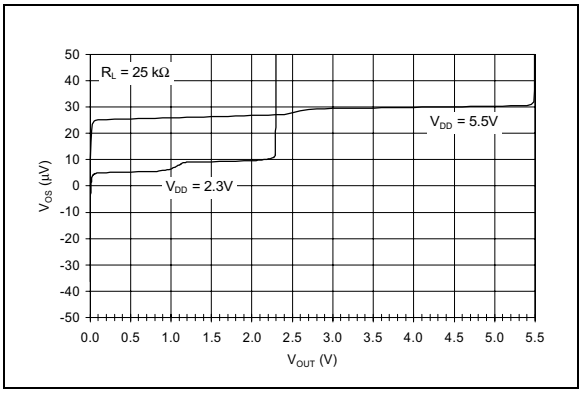


FIGURE 2-18: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, $T_A = 25°C$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, V_{SS} = GND

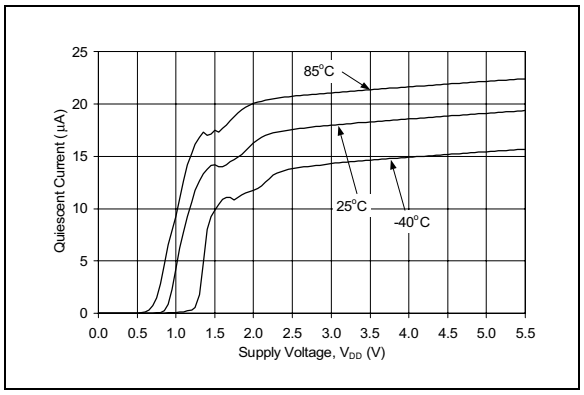


FIGURE 2-19: *Quiescent Current vs. Power Supply Voltage vs. Temperature.*

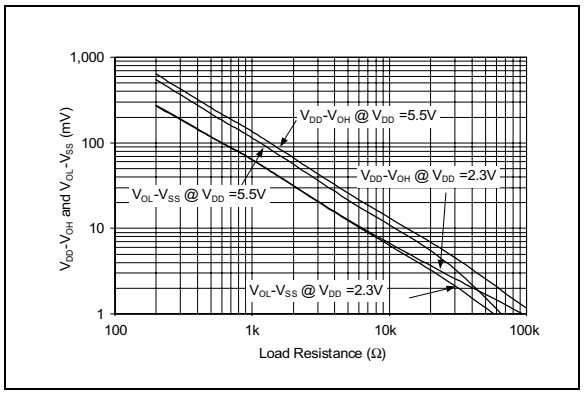


FIGURE 2-22: *Maximum Output Voltage Swing vs. Load Resistance.*

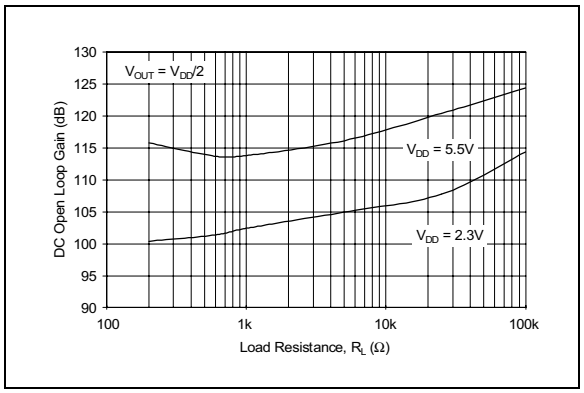


FIGURE 2-20: *DC Open Loop Gain vs. Load Resistance vs. Power Supply Voltage.*

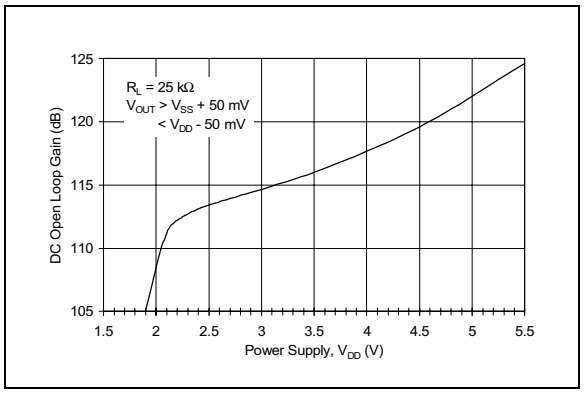


FIGURE 2-23: *DC Open Loop Gain vs. Power Supply Voltage.*

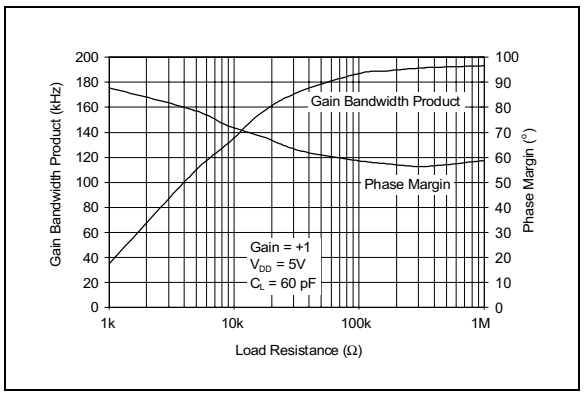


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Load Resistance.*

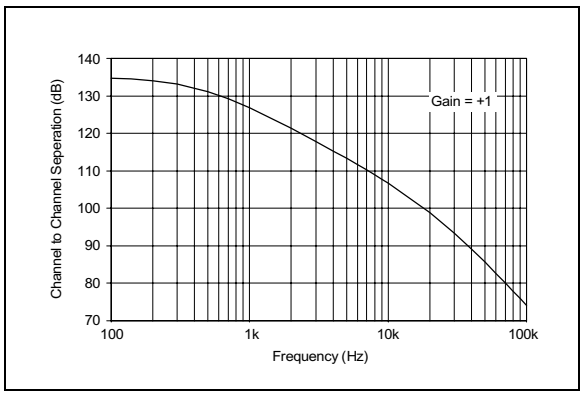


FIGURE 2-24: *Channel to Channel Separation vs. Frequency (MCP617 and MCP619 only).*

Note: Unless otherwise indicated, $T_A = 25^\circ C$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, V_{SS} = GND

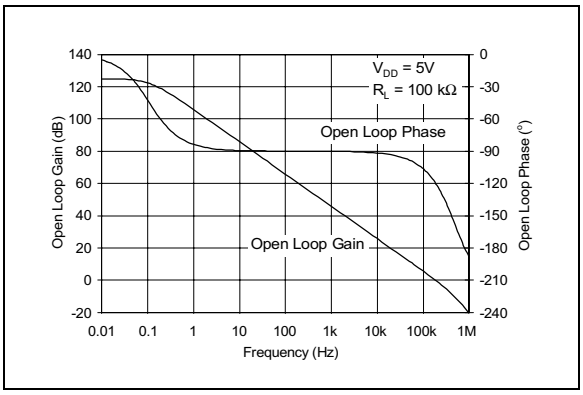


FIGURE 2-25: *Open Loop Gain, Phase vs. Frequency.*

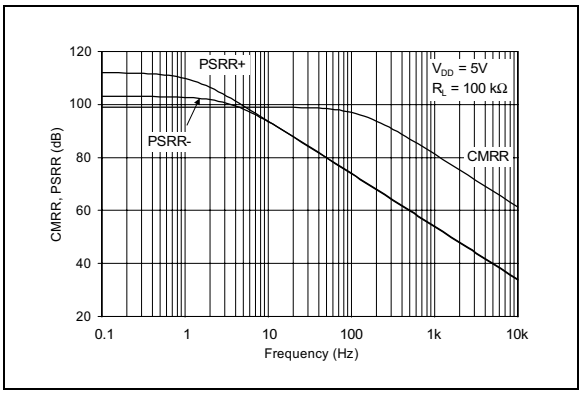


FIGURE 2-28: *Common-Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.*

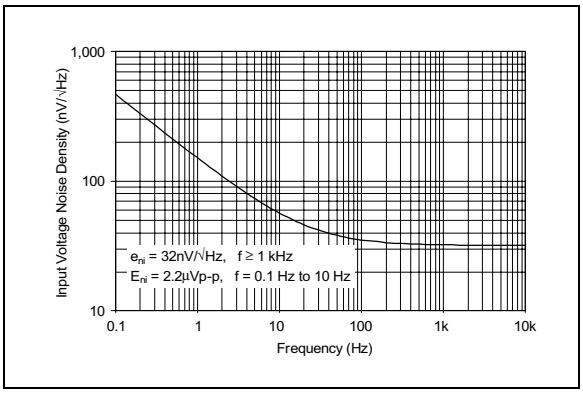


FIGURE 2-26: *Input Voltage Noise Density vs. Frequency.*

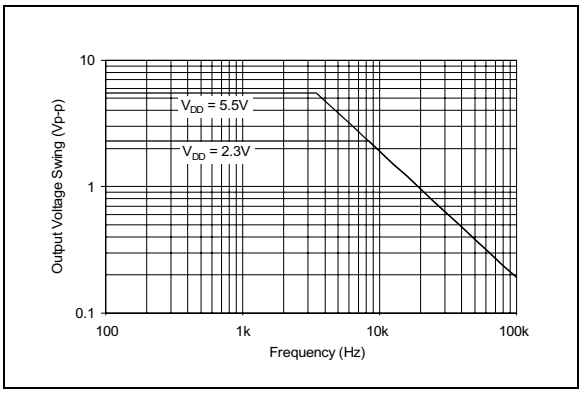


FIGURE 2-29: *Maximum Output Voltage Swing vs. Frequency.*

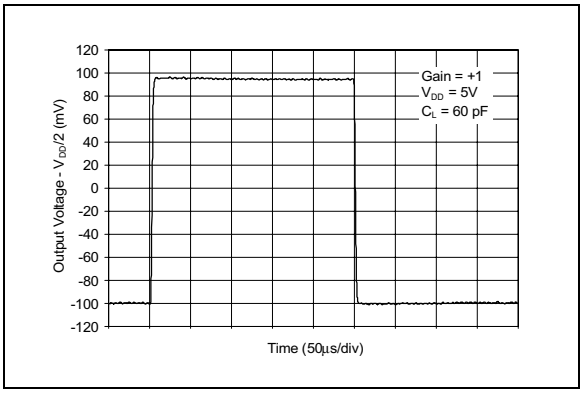


FIGURE 2-27: *Small Signal Non-Inverting Pulse Response.*

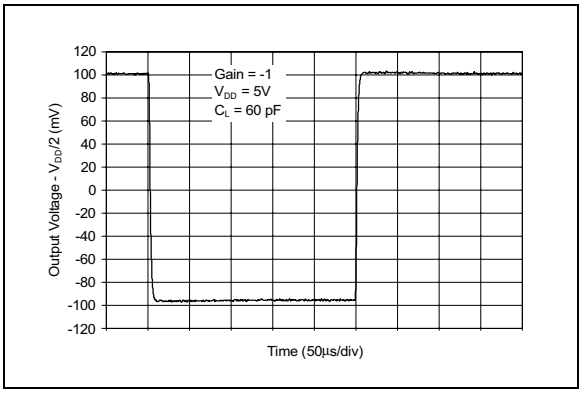


FIGURE 2-30: *Small Signal Inverting Pulse Response.*

Note: Unless otherwise indicated, $T_A = 25^\circ C$, $V_{CM} = V_{DD} / 2$ and $V_{OUT} \sim V_{DD}/2$, V_{SS} = GND

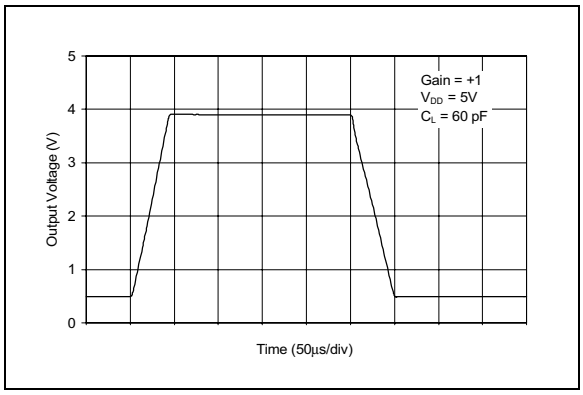


FIGURE 2-31: *Large Signal Non-Inverting Pulse Response.*

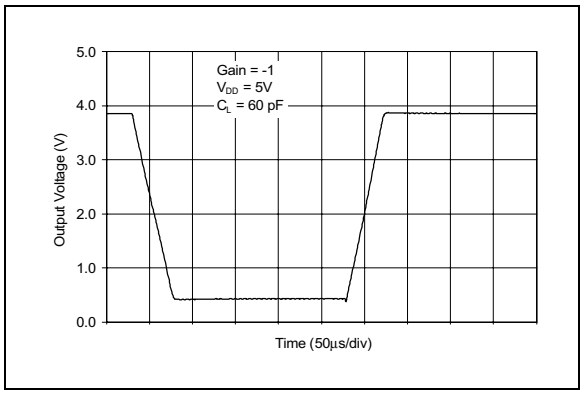


FIGURE 2-33: *Large Signal Inverting Pulse Response.*

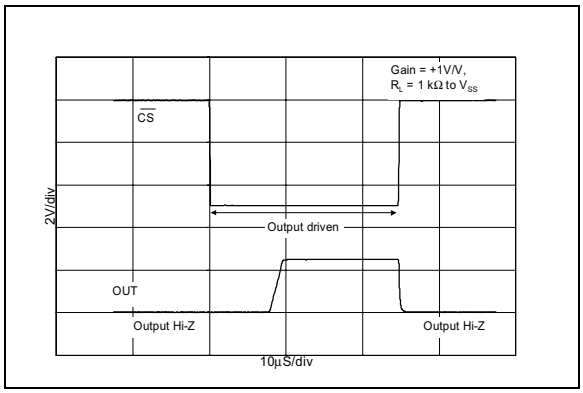


FIGURE 2-32: *$\overline{\text{Chip Select}}$ to Amplifier Output Response Time (MCP618 only).*

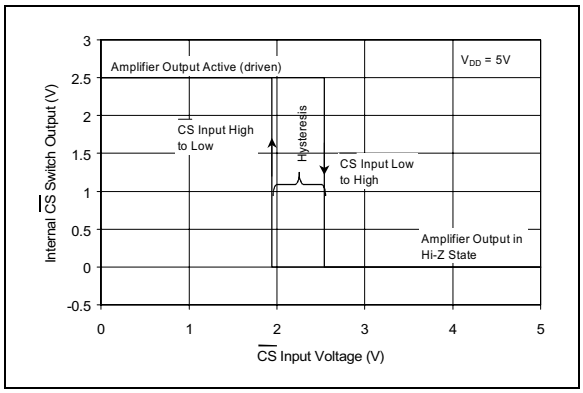


FIGURE 2-34: *$\overline{CS}$ Hysteresis (MCP618 only).*

3.0 APPLICATIONS INFORMATION

The MCP616/617/618/619 family of operational amplifiers are fabricated on Microchip's state-of-the-art CMOS process. They are unity gain stable and suitable for a wide range of general purpose applications. With this family of operational amplifiers, the power supply pin should be by-passed with a 0.1 µF capacitor.

3.1 Rail-to-Rail Output Swing

There are two specifications that describe the output swing capability of the MCP616/617/618/619 family of operational amplifiers. The first specification, Maximum Output Voltage Swing, defines the absolute maximum swing that can be achieved under specified loaded conditions. For instance, the MCP616/617/618/619 family is specified to be able to swing at least to 15 mV from the negative rail with a 25 kΩ load to $V_{DD}/2$. This output swing performance is shown in Figure 3-1, where the output of an MCP616 is configured in a gain of +2V/V and overdriven with a 4 kHz triangle wave.

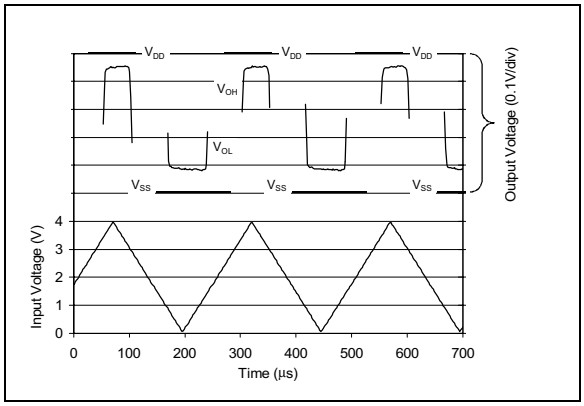


FIGURE 3-1: *Maximum Output Voltage Swing.*

The second specification that describes the output swing capability of these amplifiers is the Linear Region Output Voltage Swing. This specification defines the maximum output swing that can be achieved while the amplifier is still operating in its linear region. For instance, the open loop gain is ≥ 100 dB for a 25 kΩ load over the specified range of V_{SS} +0.050V and V_{DD} - 0.050V.

The classical definition of the DC open loop gain of an amplifier is:

$$A_{OL} = 20 \log_{10}\left(\frac{\Delta V_{OUT}}{\Delta V_{OS}}\right)$$

where:

A_{OL} is the DC open loop gain of the amplifier

ΔV_{OUT} is the change in V_{OUT} while in the Linear Region Output Voltage swing spec

ΔV_{OS} is the change in input offset voltage with the change in V_{OUT}

3.2 Input Voltage and Phase Reversal

The MCP616/617/618/619 amplifier family is designed with CMOS devices and PNP input transistors. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 3-2 shows an input voltage exceeding both supplies with no resulting phase inversion.

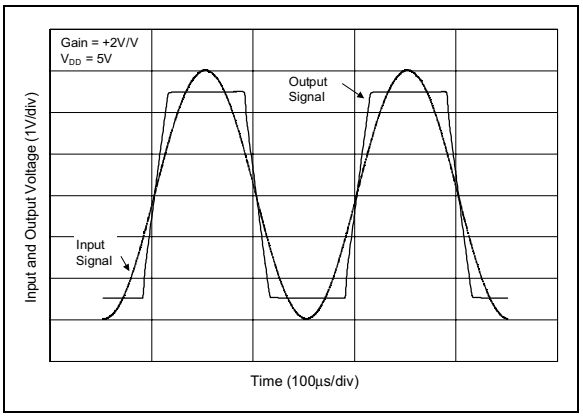


FIGURE 3-2: *The MCP616/617/618/619 family of op amps do not have phase reversal issues. For this graph, the amplifier is in a gain of +2V/V.*

The maximum operating common-mode voltage that can be applied to the inputs is V_{SS} to V_{DD} -0.9V. In contrast, the absolute maximum input voltage is V_{SS} - 0.3V and V_{DD} + 0.3V. Voltages on the input that exceed this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor as shown in Figure 3-3.

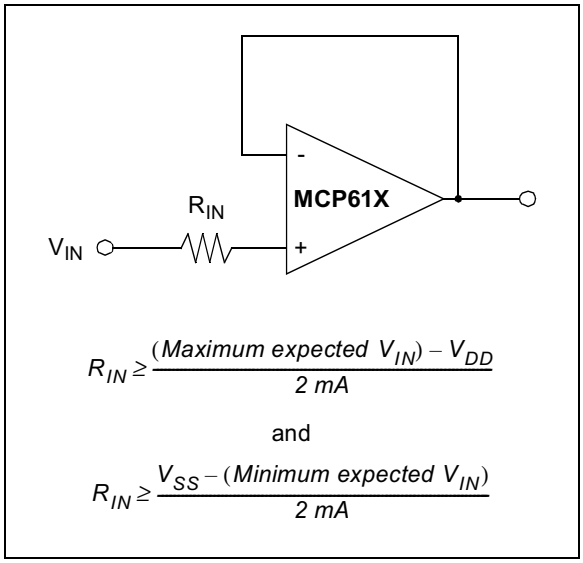


FIGURE 3-3: *If the inputs of the amplifier exceed the Absolute Maximum Specifications, an input resistor, R_{IN}, should be used to limit the current flow into that pin.*

3.3 Capacitive Load and Stability

Driving capacitive loads can cause stability problems with many of the higher speed amplifiers.

For any closed loop amplifier circuit, a good rule of thumb is to design for a phase margin that is no less than 45°. This is a conservative theoretical value, however, if the phase margin is lower, layout parasitics can degrade the phase margin further causing a truly unstable circuit. A system with 45° phase margin will have an overshoot in its step response of approximately 25%.

A buffer configuration with a capacitive load is the most difficult configuration for an amplifier to maintain stability. The Phase versus Capacitive Load of the amplifier is shown in Figure 3-4. In this figure, it can be seen that the amplifier has a phase margin above 45°, while driving capacitance loads up to 150 pF. This figure also shows that higher capacitive loads reduce the bandwidth of the amplifier.

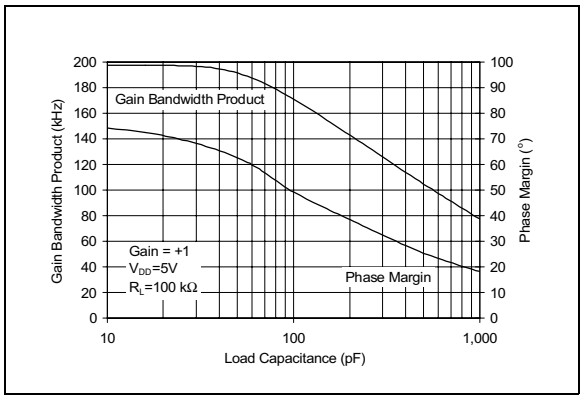


FIGURE 3-4: *Gain Bandwidth Product, Phase Margin vs. Capacitive Load.*

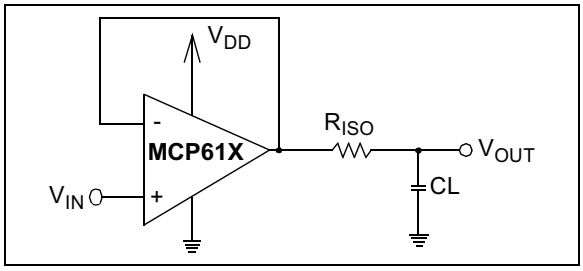


FIGURE 3-5: *Amplifier circuits that can be used when driving heavy capacitive loads.*

If the amplifier is required to drive larger capacitive loads, the circuit shown in Figure 3-5 can be used. A small series resistor (R_{ISO}) at the output of the amplifier improves the phase margin when driving large capacitive loads. This resistor decouples the capacitive load from the amplifier by introducing a zero in the transfer function. It will not, however, significantly improve the bandwidth for larger capacitive loads.

This zero adjusts the phase margin by approximately:

$$\Delta\theta_m = \tan^{-1}(2\pi GBWP \times R_{ISO} \times C_L)$$

where:

$\Delta\theta_m$ is the improvement in phase margin,

GBWP is the gain bandwidth product of the amplifier,

R_{ISO} is the capacitive decoupling resistor, and

C_L is the load capacitance

3.4 DC Offsets

The MCP616/617/618/619 amplifier family has very low offset voltage (150 µV max at T_A = 25°C). These amplifiers use a PNP transistor input stage with a typical bias currents of -15 nA, which must have a DC path to ground or the op amp will not bias properly. The DC resistances seen by the op amp inputs (R_2 and $R_F||R_1$ in Figure 3-6) need to be equal to minimize DC offsets. Also keep these resistance ≤100 kΩ for low DC offset.

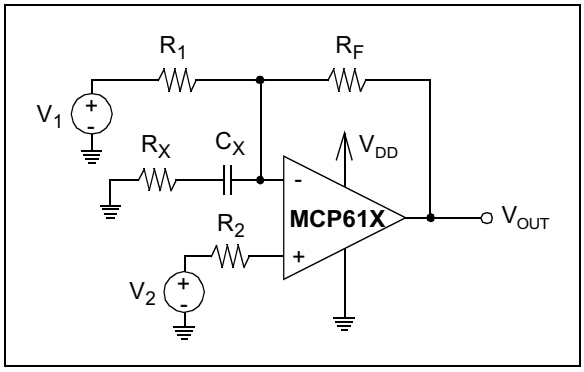


FIGURE 3-6: *Circuit for calculating DC Offset.*

To calculate the DC offset (ΔV_{OUT}), first simplify the circuit to its DC equivalent.

- Replace capacitors with open circuits
- Replace inductors with short circuits
- Replace AC voltage sources with short circuits
- Replace AC current sources with open circuits
- Convert DC sources and resistances into Thieving equivalent form

Second, calculate the nominal DC bias point. Note that current is positive going into the op amp, so the bias current spec shows current sourced out of the inputs.

$$V_{CM} = V_2 - I_B R_2$$
$$G_N = 1 + R_F / R_1$$
$$V_{OUT} = V_2(G_N) - V_1(G_N - 1)$$

Where:

V_{CM} is the common mode voltage at the op amp inputs

G_N is the DC gain from the non-inverting input to V_{OUT}

Third, calculate the DC error voltage caused by the op amp.

$$\Delta V_{OUT} = G_N V_{OS} + G_N I_B (R_F \| R_1 - R_2) - G_N I_{OS} \frac{R_F \| R_1 + R_2}{2}$$

Last, use the values in the DC Characteristics table to determine the worst case V_{OUT} + ΔV_{OUT} for your design. Make sure that the output voltage range is not exceeded.

Note that with very high input DC resistances, the output may exceed the linear region output voltage swing specification, and the op amp will saturate. Keep the input resistances below 100 kΩ to help prevent this from happening.

3.5 The Chip Select Option of the MCP618

The MCP618 is a single amplifier with a Chip Select ($\overline{CS}$) option. When $\overline{CS}$ is pulled high the supply current drops to 50 nA (typ). In this state, the amplifier is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier will not operate properly. Figure 3-7 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

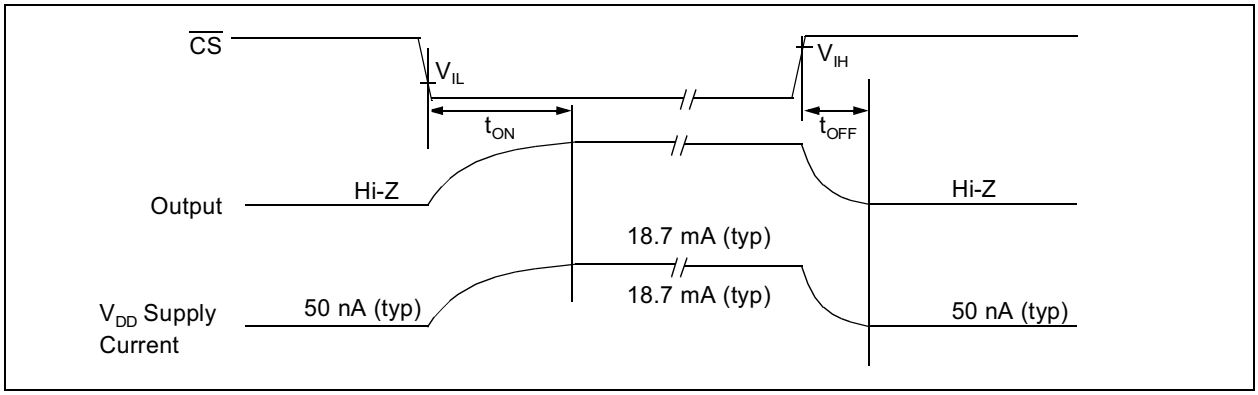


FIGURE 3-7: *Timing Diagram for the $\overline{CS}$ Function of the MCP618 Amplifier.*

3.6 Layout Considerations

Good PC board layout techniques will help you achieve the performance shown in the specs and Typical Performance Curves. It will also help you minimize EMC (Electro-Magnetic Compatibility) issues.

3.6.1 COMPONENT PLACEMENT

Partition the board layout into different sections to minimize crosstalk. Digital and analog functions should be separated from each other. High speed and low speed parts should be kept apart whenever possible.

Keep important signal traces as short as possible, especially high frequency (low rise time) signals. This reduces the signal's exposure to interference. Other traces, such as supply lines, can be longer. Place analog parts in the signal path close together.

Use a 0.1 µF supply bypass capacitor within 0.1" (2.5 mm) of the V_{DD} pin. It should connect directly to the ground plane, in order to minimize ground loops.

3.6.2 SIGNAL COUPLING

The input pins of the MCP616/617/618/619 amplifiers are high impedance, which allows noise injection if good layout techniques are not followed. Current can be injected into the inputs from another trace with fast changing voltages, such as digital clock. This current is coupled capacitively between the traces.

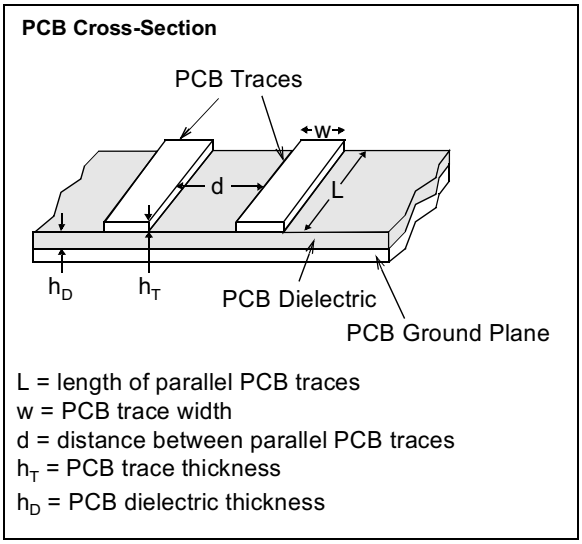


FIGURE 3-8: *Capacitors can be built with PCB traces, allowing signals to couple from one trace to another.*

The PCB layout shown in Figure 3-8 produces parasitic capacitances as shown in Figure 3-9. The resistor R_{T2} includes the op amp input resistance, and any additional resistance the designer ties from the trace to ground.

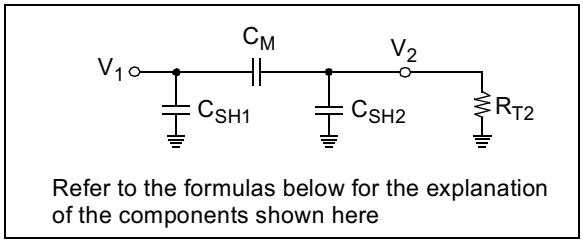


FIGURE 3-9: *Equivalent circuit for Figure 3-8.*

The signal, V_1 is coupled to the sensitive trace through the mutual capacitance, C_M. The terminating resistor, R_{T2} attenuates the coupled signal at low frequencies, and the shunt capacitor, C_{SH2} at high frequencies. Without the ground plane (C_{SH2} = 0), V_1 would appear without attenuation on the sensitive trace at high frequencies. The capacitances C_M, C_{SH1} and C_{SH2} can be approximated with these formulas:

$$C_M \approx \frac{h_T L \varepsilon_0 \varepsilon_r}{d}$$

$$C_{SH1} = C_{SH2} \approx \frac{L w \varepsilon_0 \varepsilon_r}{h_d}$$

Where:

V_1 = interfering voltage signal

C_M = mutual capacitance

C_{SH1} = shunt capacitance at V_1

C_{SH2} = shunt capacitance at sensitive trace

R_{T2} = optional terminating resistance attached to sensitive trace

To reduce this capacitively coupled signal,

1. Always use ground plane.
   a. Put ground plane and sensitive traces in adjacent PCB layers.
   b. Inject large currents into the ground plane far away from sensitive traces.
2. Minimize interfering signal strength.
   a. Keep the edge rates on digital signals low.
   b. Limit the bandwidth of analog signals.
   c. Keep interfering traces far apart.
   d. Minimize distance interfering traces are in parallel.
3. Dissipate interfering signals at sensitive traces.
   a. Make sensitive traces as wide and short as possible.
   b. Connect a low-valued shunt resistor from sensitive trace to ground.

3.7 Typical Applications

3.7.1 HIGH GAIN PRE-AMPLIFIER

The MCP616/617/618/619 amplifiers are well suited to amplifying small signals produced by low impedance sources/sensors. The low offset voltage, low offset current, and low noise fit well in this role. Figure 3-10 shows a typical pre-amplifier connected to a low impedance source (V_S and R_S).

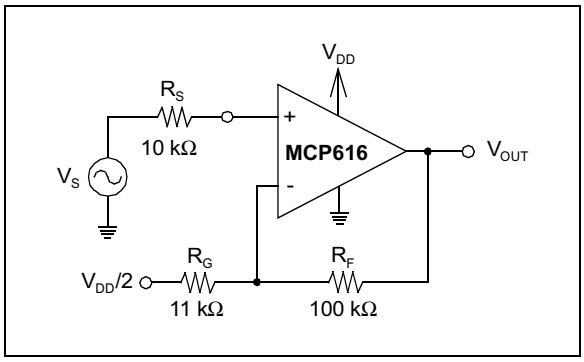


FIGURE 3-10: *High gain pre-amplifier for low resistance sources.*

For the best noise and offset performance, the source resistance R_S needs to be ≤15 kΩ. The DC resistances at the inputs are equal to minimize the offset voltage caused by the input bias currents. In this circuitry, the DC gain is 10V/V, which will give a typical bandwidth of 16 kHz.

3.7.2 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two op amp instrumentation amplifier shown in Figure 3-11 serves the function of taking the difference of two input voltages, level shifting then and providing a single output. This configuration is best suited for higher gains. The key specifications that make the MCP616/617/618/619 family appropriate for this application circuit is low offset voltage and high common-mode rejection. The reference voltage (V_{REF}) of this circuit is supplied to the first op amp in the signal chain. Typically, this voltaged is half of the supply voltage in a single supply environment.

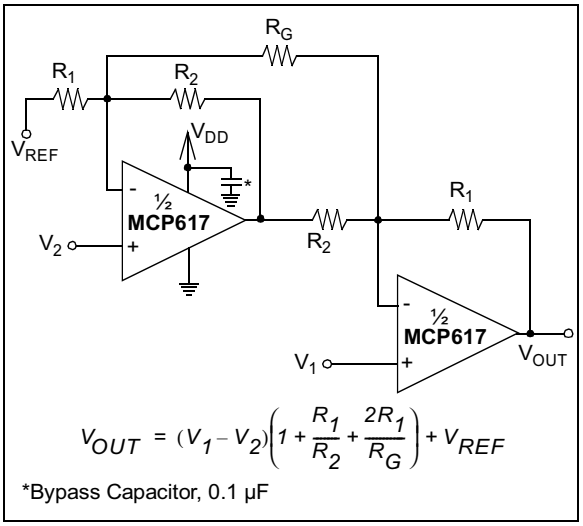


FIGURE 3-11: *Two Op Amp Instrumentation Amplifiers.*

3.7.3 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three op amp instrumentation amplifier is illustrated in Figure 3-12. The input operational amplifiers in this circuit provide signal gain. The output operational amplifier converts the signal from two inputs to a single ended output with a difference amplifier. The gain of this circuit is simply adjusted with one resistor, R_G. The reference voltage (V_{REF}) of the difference stage of this instrumentation amplifier is capable of spanning a wide range. Most typically, this node is referenced to half of the supply voltage in a signal supply application.

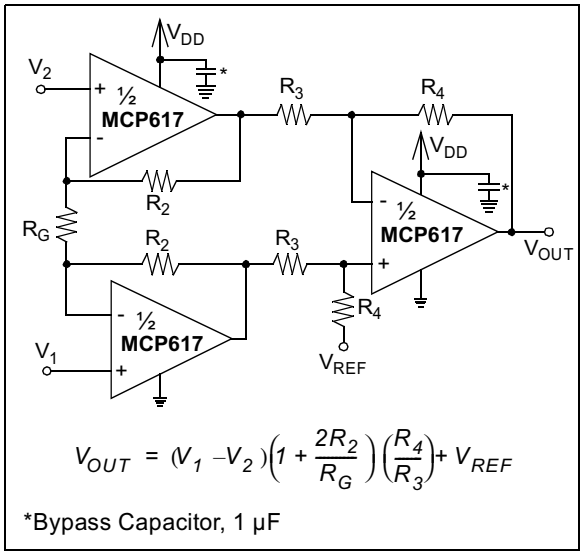


FIGURE 3-12: *Three Op Amp Instrumentation Amplifiers.*

3.7.4 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 3-13, the low input offset voltage of the MCP616 is used to implement a circuit with a high gain. This precision measurement can easily be disrupted by changing the output current drive of the device that is doing the amplification work. Consequently, the precision amplifier configuration is followed by a MCP601 amplifier which is capable of driving higher currents. Since the two amplifiers are housed in separate packages, there is minimal change in offset voltage of the MCP616 due to loading effects.

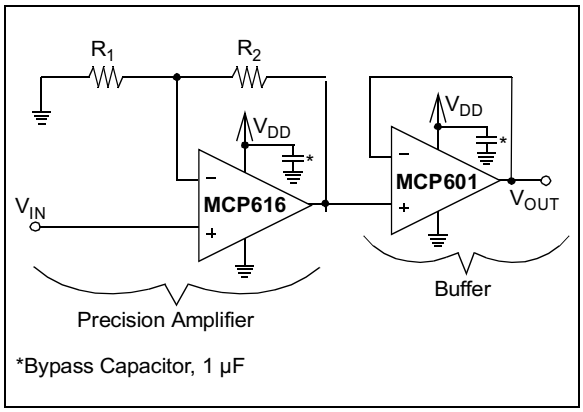


FIGURE 3-13: *Precision Gain with Good Load Isolation.*

4.0 SPICE MACROMODEL

The Spice macromodel for the MCP616, MCP617, MCP618 and MCP619 simulates the typical amplifier performance of offset voltage, DC power supply rejection, input capacitance, DC common mode rejection ratio, open loop gain over frequency, phase margin with no capacitive load, output swing, DC power supply current, power supply current change with supply voltage, input common mode range and input voltage noise.

The characteristics of the MCP616, MCP617, MCP618, and MCP619 amplifiers are similar in terms of performance and behavior. This single op amp macromodel supports all four devices with the exception of the chip select ($\overline{CS}$) function of the MCP618, which is not modeled.

The listing for this macromodel is shown on the next page. The most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

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```
.SUBCKT MCP616 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*              Non-inverting Input
*
* Macromodel for MCP616 (single), MCP617 (dual), MCP618 (single w/CS),and MCP619 (quad)
*
* The characteristics of the MCP616, MCP617, MCP618, and MCP619 have the same fundamental
* performance and behavior. Consequently, this single op amp macromodel supports all four
* devices. However, the chip select function of the MCP618 is not modeled.
*
* Revision History:
*   REV A : 2-23-01  created  KEB
*
* This macromodel models typical amplifier offset voltage, DC power supply rejection, input
* capacitance, open loop gain over frequency, phase margin with 60pF load, output swing,
* power supply current, input voltage noise, slew rate.
*
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* AT ANY TIME WITHOUT NOTICE.
*
*Input Stage, pole at 300kHz
*
Q1      9 64   7   PQ
Q2      8  2   7   PQ
CDM     1  2   2P
IOS     1  2   400P
CCM1    1  4   4P
CCM2    2  4   4P
IDD     3  7   13.3U
DCT    20  3   DX
VCT    20  7   1.10
RA      8  6   5.53K
RB      9  6   5.53K
CA      8  9   48.0P
VCMM    4  6   0.45
ICOMP   4  3   195U
*
```
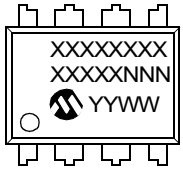

```
* Input Stage Common-Mode Clamping
*
ECM   55  4  3 64 1

RCM   57 56  1K
DCMP  56 55  DY
VCMP  57  4  1.2

RST   58 59  1K
DST   59 55  DX
VST   58  4  1.6

GCMP2 23  4  POLY(2) 57 56 58 59   0 0 0;0 -500U 500U
*
* Input Errors (vos, en, psr)
*
ERR   64  1  poly(2) 67 4 3 4   -50U 2.3 6U
*
* Second Stage, pole at 0.19Hz
*
GS    23  4  8  9  181U
R1    23  4  5.53G
C2    23  4  166P

VSOM   3 24  4.784
VSOP  25  4  -3.98
DSOM  23 24  DY
DSOP  25 23  DY

*HCM   23  3  VCMP

FS     3  4  POLY(11) VO3 VO5 VO4 VO6 VO1 VO2 VO9 VO10 VMID1 VSOP VSOM
+ 200U -1 -1 -1 1 -1 -1 1 1 -1 -1 -1
*
* Mid-supply Reference
*
RMID1   3 35  61.62K
VMID1  35 34  0
RMID2   4 34  61.62K
ELEVEL 34  4 23  4 -1
*
* Output Stage
*
DO3    34 43  DY
DO4    44 34  DY
DO5     3 45  DY
DO6     3 46  DY
DO7     4 45  DY
DO8     4 46  DY
VO3    43  5  0.1
VO4     5 44  30M

GO5     3 47  3 34  10M
VO5    47  5  0
GO6     4 48 34  4  10M
VO6    48  5  0
GO1    49  4  5 34  10M
VO1    49 45  0

GO2    50  4 34  5  10M
VO2    50 46  0
RO9     3 51  100
VO9    51  5  0
RO10   52  4  100
VO10   52  5  0
```

```
*
* Input Voltage Noise
VN1    65  4  0.6
DN1    65 67  DX
RN1    67  4  10K
*
* Models
*
.model PQ PNP (IS=0.1F BF=440 VAF=70 RB=1K)
.model DY D (IS=1F BV=50)
.model DX D (IS=0.001F AF=1.0 KF=55F)
*
.ENDS MCP616
```

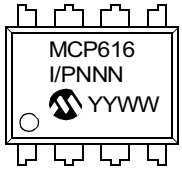
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

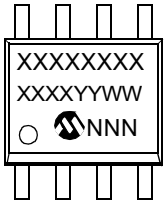
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (150 mil)



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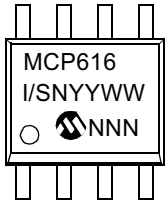
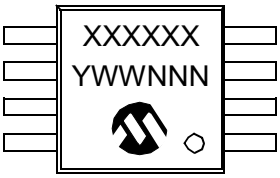


8-Lead MSOP



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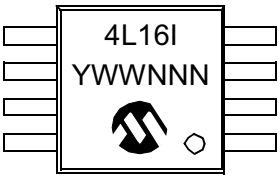

Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

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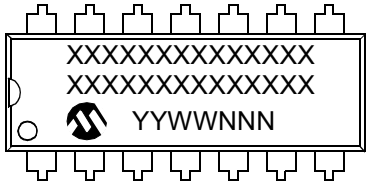
Package Marking Information (Continued)

14-Lead PDIP (300 mil)(MCP619)



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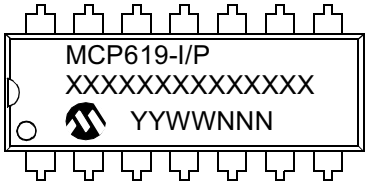
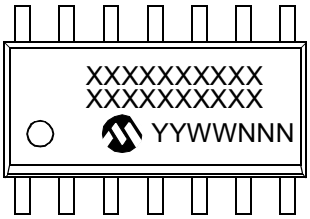


14-Lead SOIC (150 mil)(MCP619)



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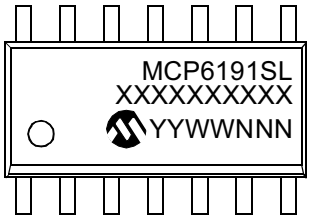
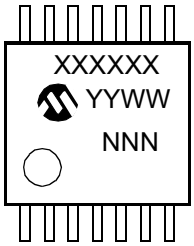
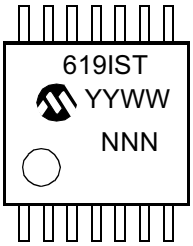


14-Lead TSSOP(MCP619)



Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

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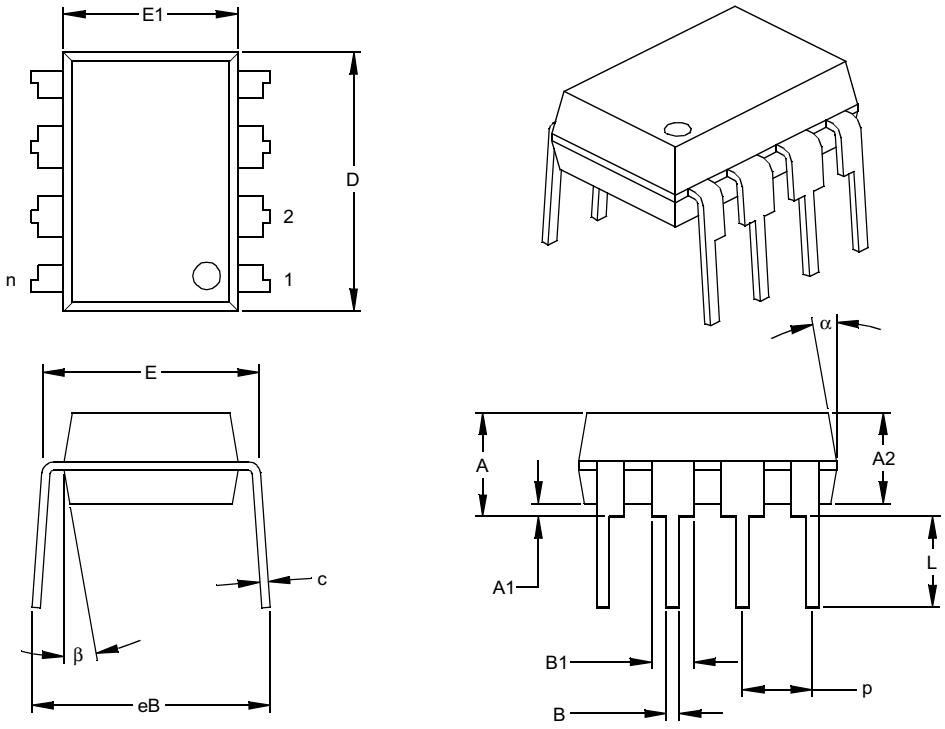
8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

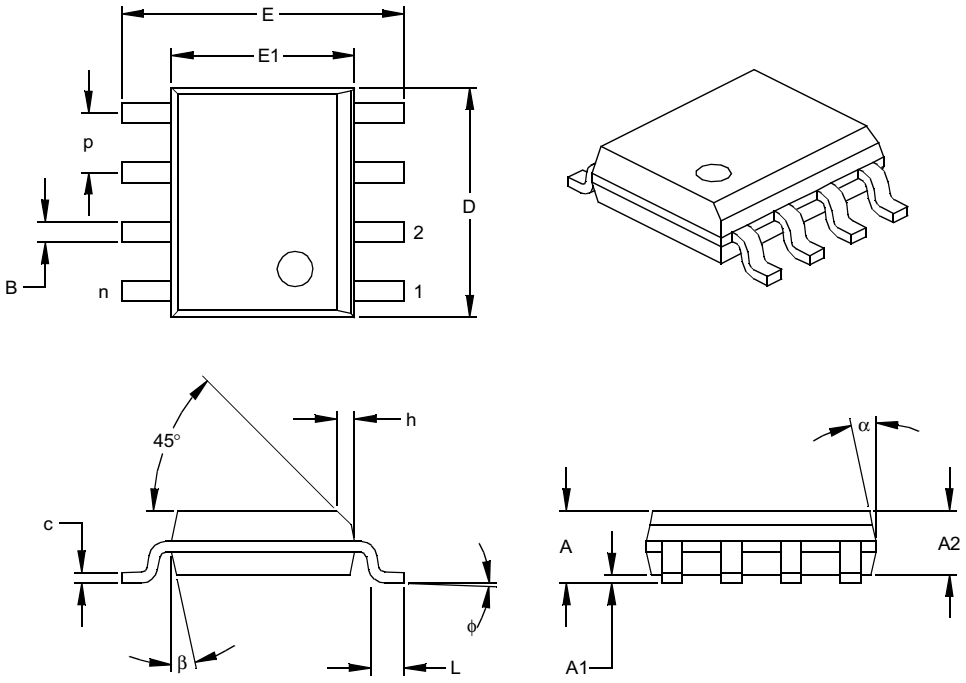


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

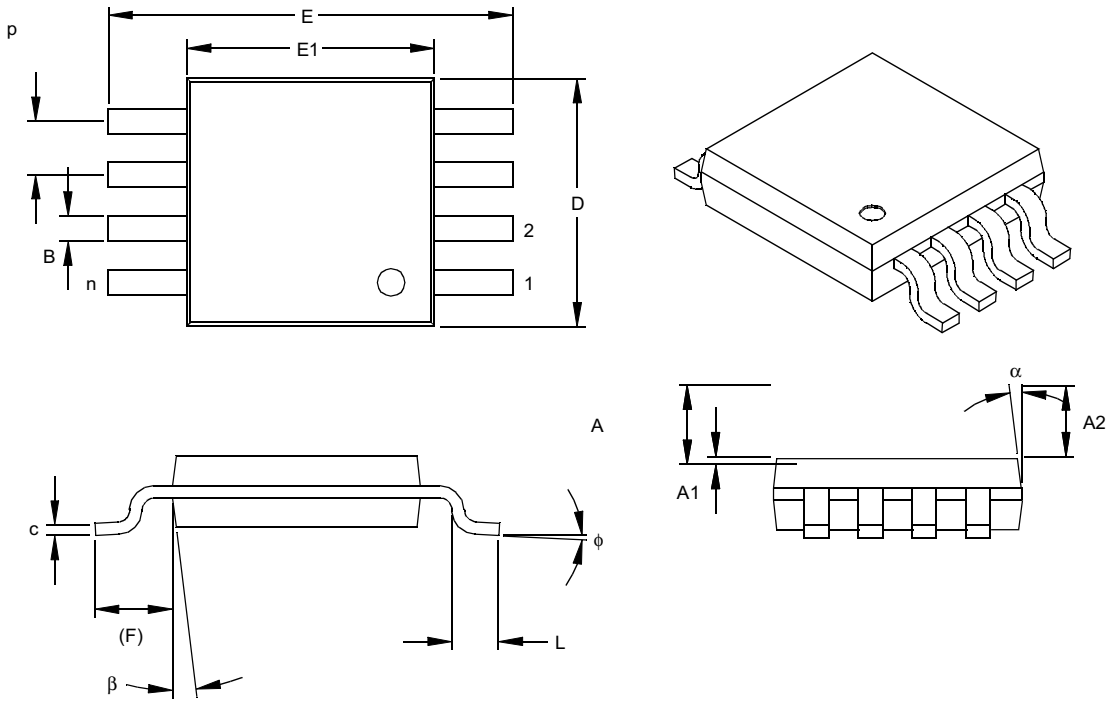


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8				8
Pitch	p		.026			0.65	
Overall Height	A			.044			1.18
Molded Package Thickness	A2	.030	.034	.038	0.76	0.86	0.97
Standoff §	A1	.002		.006	0.05		0.15
Overall Width	E	.184	.193	.200	4.67	4.90	.5.08
Molded Package Width	E1	.114	.118	.122	2.90	3.00	3.10
Overall Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.016	.022	.028	0.40	0.55	0.70
Footprint (Reference)	F	.035	.037	.039	0.90	0.95	1.00
Foot Angle	φ	0		6	0		6
Lead Thickness	c	.004	.006	.008	0.10	0.15	0.20
Lead Width	B	.010	.012	.016	0.25	0.30	0.40
Mold Draft Angle Top	α		7			7	
Mold Draft Angle Bottom	β		7			7	

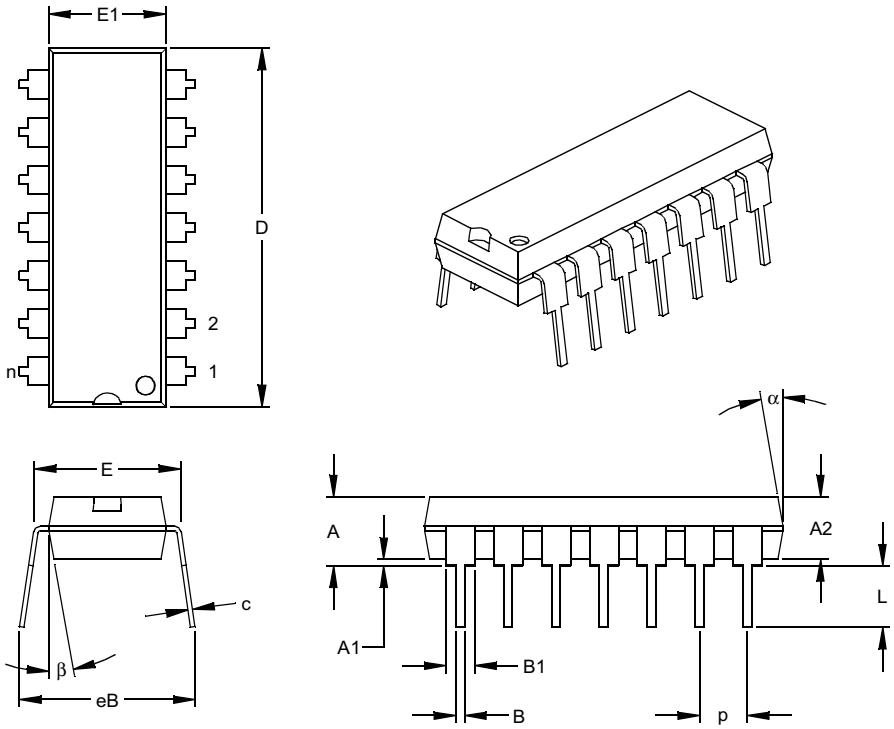
*Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-111

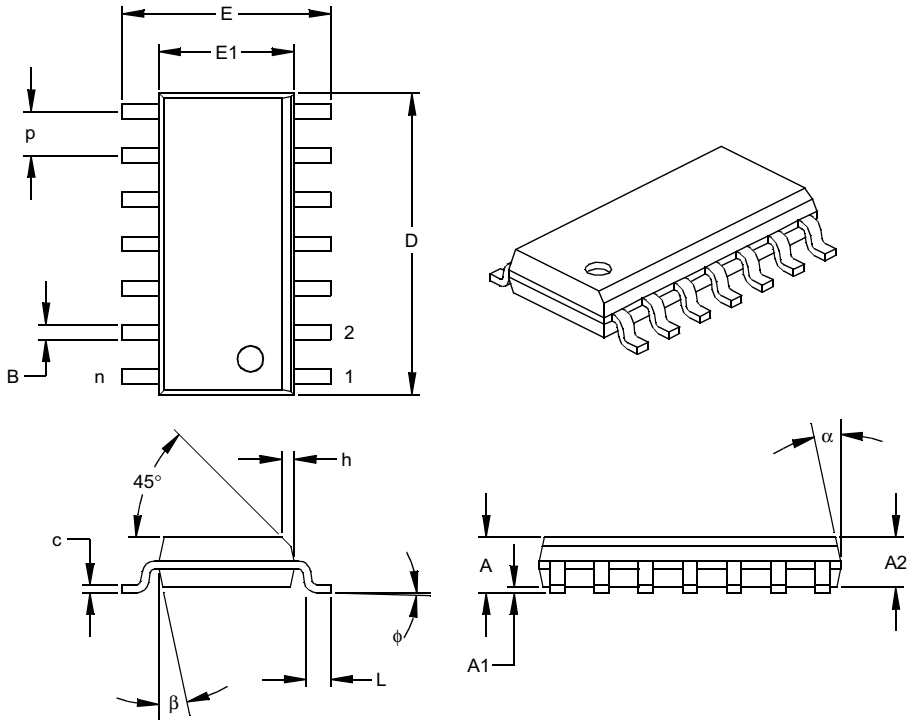
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

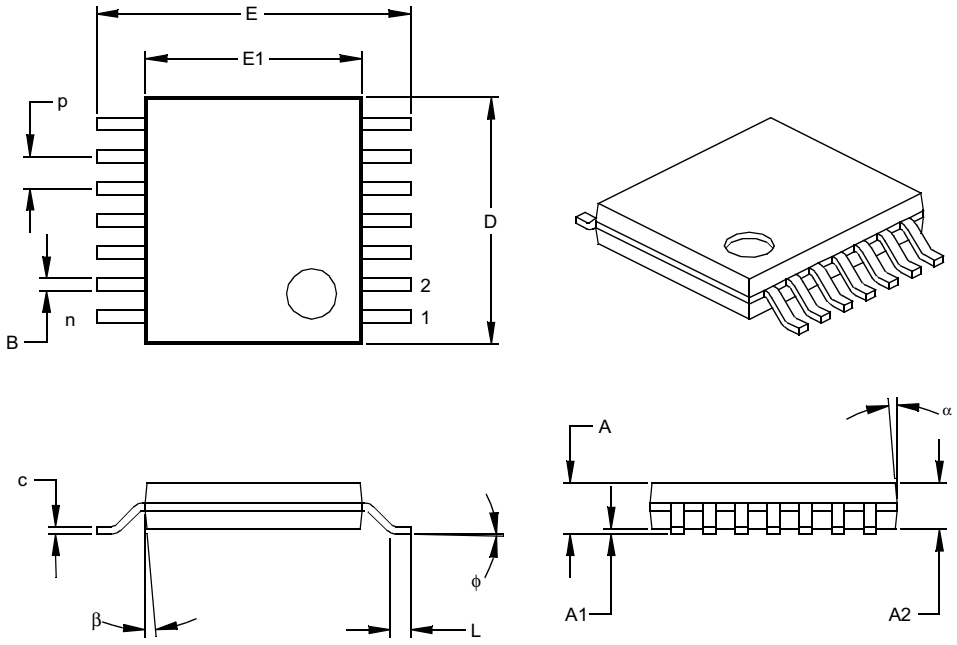


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

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013001

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Device: **MCP616/617/618/619** Literature Number: **DS21613A**

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	MCP616	= Single Operational Amplifier
	MCP616T	= Single Operational Amplifier (Tape and Reel-SOIC/MSOP)
	MCP617	= Dual Operational Amplifier
	MCP617T	= Dual Operational Amplifier (Tape and Reel-SOIC/MSOP)
	MCP618	= Single Operational Amplifier w/$\overline{CS}$ Function
	MCP618T	= Single Operational Amplifier w/$\overline{CS}$ Function (Tape and Reel-SOIC/MSOP)
	MCP619	= Quad Operational Amplifier
	MCP619T	= Quad Operational Amplifier (Tape and Reel-SOIC/TSSOP)
Temperature Range	I	= -40°C to +85°C
Package	P	= Plastic DIP (300 mil Body), 8-lead & 14-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead
	ST	= Plastic TSSOP, 14-lead
	MS	= Plastic MSOP, 8-lead

Examples:

a) MCP616-I/P Industrial Temp., PDIP package
b) MCP616-I/SN Industrial Temp., SOIC package
c) MCP616T-I/SN Tape and Reel, Industrial Temp., SOIC package
d) MCP616-I/MS Industrial Temp., MSOP package
e) MCP616T-I/MS Tape and Reel, Industrial Temp., MSOP package
f) MCP617-I/P Industrial Temp., PDIP package
g) MCP618-I/SN Industrial Temp., SOIC package
h) MCP618T-I/SN Tape and Reel, Industrial Temp., SOIC package
i) MCP619-I/P Industrial Temp., PDIP package

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