LM49250 Boomer® Audio Power Amplifier Series Enhanced Emissions Suppression Stereo Class D Audio Sub-System with Ground Referenced Headphone Amplifier and Mono Earpiece

Check for Samples: LM49250

FEATURES

- **Output Short Circuit Protection**
- **Thermal Overload Protection**
- **Stereo Filterless Class D Operation**
- **Spread Spectrum Modulation**
- **Ground Referenced Headphone Drivers**
- **I^2C Control Interface**
- **32-Step Input Volume Control**
- **Output Volume Control**
- **Minimum External Components**
- **Click and Pop Suppression**
- **Micro-Power Shutdown**
- **Available in Space-Saving 36–Bump DSBGA Package**
- **Single Supply Operation**
- **RF Suppression**

APPLICATIONS

- **Mobile Phones**
- **Portable Navigation Devices**
- **Portable Media Players**

KEY SPECIFICATIONS

- **Power Output at V_{DD} = 5V Speaker:**
  - **R_L = 4Ω, THD+N ≤ 1%: 1.97W/Ch**
  - **R_L = 4Ω, THD+N ≤ 10%: 2.4W/Ch**
  - **R_L =8Ω, THD+N ≤ 1%: 1.2W/Ch**
- **Headphone:**
  - **R_L = 16Ω, THD+N ≤ 1%: 41mW/Ch**
  - **R_L = 32Ω, THD+N ≤ 1%: 45mW/Ch**
- **Earpiece:**
  - **R_L = 16Ω, THD+N ≤ 1%: 170mW**
  - **R_L = 32Ω, THD+N ≤ 1%: 90mW**
- **Shutdown Current: 0.1µA**
- **Efficiency at 5V, 1W into 8Ω: 87%**
- **Efficiency at 3.6V, 500mW into 8Ω: 85%**

DESCRIPTION

The LM49250 is a fully integrated audio subsystem designed for stereo cell phone applications. The LM49250 combines a 2.4W/Ch stereo class D speaker amplifiers with a 45mW/Ch stereo ground referenced headphone amplifier, a class AB earpiece amplifier, TI 3D enhancement, volume control, and an input mixer into a single device. The filterless class D amplifiers deliver 1.2W/Ch into an 8Ω load with <1% THD+N from a 5V supply.

The LM49250 features a new circuit technology that utilizes a charge pump to generate a negative supply voltage. This allows the headphone outputs to be biased about ground, thereby eliminating the output-coupling capacitors.

For improved noise immunity, the LM49250 features fully differential left, right and mono inputs. The three inputs can be mixed/multiplexed to any output combination of the loudspeaker, headphone or earpiece amplifiers. The left and right differential inputs can be used as separate single-ended inputs, mixing multiple stereo audio sources. The mixer, volume control, and device mode select are controlled through an I^2C compatible interface.

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Output short circuit and thermal overload protection prevent the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

Typical Application

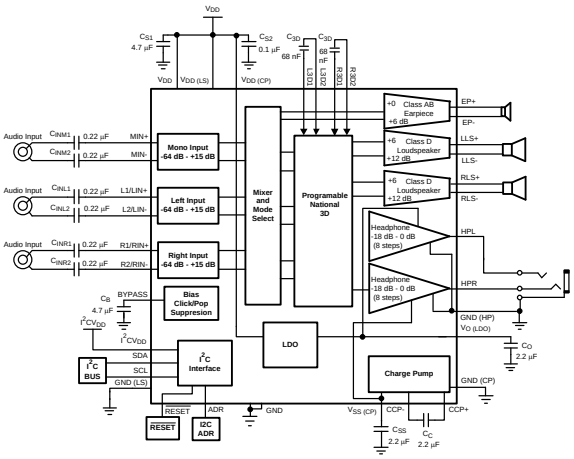

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Top View

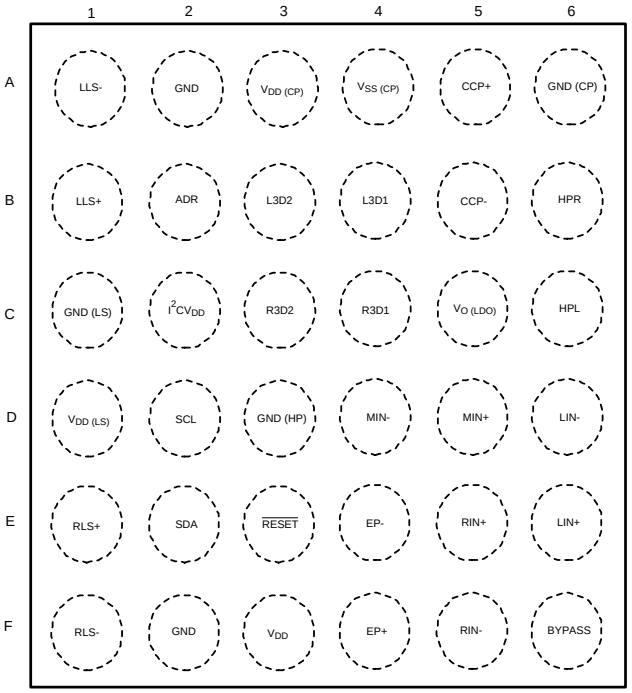

Figure 2. DSBGA Package
See Package Number YPG0036CCA

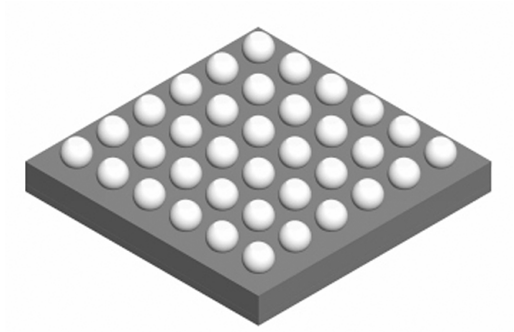

Figure 3. Package View (Top View)
Package Number YPG0036CCA

Table 1. Bump Description

BUMP	NAME	DESCRIPTION
A1	LLS-	Negative left differential loudspeaker output
A2	GND	Ground
A3	$V_{DD(CP)}$	Charge pump supply voltage
A4	$V_{SS(CP)}$	Negative supply voltage (charge pump output)
A5	CCP+	Charge pump flying capacitor positive terminal
A6	GND(CP)	Charge pump ground
B1	LLS+	Positive left differential loudspeaker output

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Table 1. Bump Description (continued)

BUMP	NAME	DESCRIPTION
B2	ADR	I^2C address select
B3	L3D2	Left 3D input
B4	L3D1	Left 3D output
B5	CCP-	Charge pump flying capacitor negative terminal
B6	HPR	Right ground referenced headphone output
C1	GND(LS)	Loudspeaker ground
C2	$I^2C\_V_{DD}$	I^2C supply voltage
C3	R3D2	Right 3D input
C4	R3D1	Right 3D output
C5	$V_{O(LDO)}$	LDO output voltage
C6	HPL	Left ground referenced headphone output
D1	$V_{DD(LS)}$	Loudspeaker supply voltage
D2	SCL	I^2C clock
D3	GND(HP)	Headphone ground
D4	MIN-	Negative mono audio input
D5	MIN+	Positive mono audio input
D6	LIN-	Negative left audio input
E1	RLS+	Positive right differential loudspeaker output
E2	SDA	I^2C data
E3	$\overline{\text{RESET}}$	I^2C reset
E4	EP-	Negative differential earpiece output
E5	RIN+	Positive right audio input
E6	LIN+	Positive left audio input
F1	RLS-	Negative right differential loudspeaker output
F2	GND	Ground
F3	V_{DD}	Power supply voltage
F4	EP+	Positive differential earpiece output
F5	RIN-	Negative right audio input
F6	BYPASS	Amplifier bypass

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)(2)(3)

Supply Voltage (1)	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (4)	Internally Limited
ESD Rating (5)	2000V
ESD Rating (6)	200V
Junction Temperature	150°C
Thermal Resistance, θ_{JA} (YPG0036CCA)	44.4°C/W

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range, $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage (V_{DD}, $V_{DD(LS)}$, $V_{DD(CP)}$)	$2.7V \le V_{DD} \le 5.5V$
I^2C Voltage (I^2CV_{DD})	$1.7V \le I^2CV_{DD} \le 5.5V$
	$V_{DD} = V_{DD(CP)} = V_{DD(LS)}$
	$I^2CV_{DD} \le V_{DD}$

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Electrical Characteristics (1)(2)

The following specifications apply for V_{DD} = $V_{DD(LS)}$ = $V_{DD(CP)}$ = 3.6V, all selectable gains = 0dB, $R_{L(LS)}$ = 8Ω (Note 8), $R_{L(HP)}$ = 32Ω, $R_{L(EP)}$ = 32Ω, f = 1kHz and the conditions shown in the " Typical Application Circuit" unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Tests Conditions	LM49250		Units (Limits)
			Typ(3)	Limit(4)	
I_{DD}	Supply Current	V_{DD} = 3.0V, No Load, Spread Spectrum on			
		Loudspeaker (LS) Mode Stereo Mono	 5.6 3.9		 mA mA
		Headphone (HP) Mode Stereo Mono	 5.5 4.0		 mA mA
		Earpiece (EP) Mode	2.5		mA
		Stereo LS + Stereo HP Mode	9.0		mA
		V_{DD} = 3.6V, No Load, Spread Spectrum on			
		Loudspeaker (LS) Mode Stereo Mono	 6.1 4.1	 8.0	 mA (max) mA
		Headphone (HP) Mode Stereo Mono	 5.6 4.1	 7.5	 mA (max) mA
		Earpiece (EP) Mode	2.6	3.4	mA (max)
		Stereo LS + Stereo HP Mode	9.4	12.5	mA (max)
		V_{DD} = 5.0V, No Load, Spread Spectrum on			
		Loudspeaker (LS) Mode Stereo Mono	 7.1 4.8	 8.8	 mA (max) mA
		Headphone (HP) Mode Stereo Mono	 6.0 4.4	 7.7	 mA (max) mA
		Earpiece (EP) Mode	3.0	3.9	mA (max)
		Stereo LS + HP Mode	10.5	13.8	mA (max)
I_{SD}	Shutdown Supply Current		0.1	2	µA (max)
V_{OS}	Output Offset Voltage	Differential inputs Headphone (output mode 2) Speaker (output mode 2) Earpiece (output mode 1)	 3.8 10 1.5	 5.0 45 6.0	 mV (max) mV (max) mV (max)

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

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Electrical Characteristics [1][2] (continued)

The following specifications apply for V_{DD} = $V_{DD(LS)}$ = $V_{DD(CP)}$ = 3.6V, all selectable gains = 0dB, $R_{L(LS)}$ = 8Ω (Note 8), $R_{L(HP)}$ = 32Ω, $R_{L(EP)}$ = 32Ω, f = 1kHz and the conditions shown in the "Typical Application Circuit" unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Tests Conditions	LM49250		Units (Limits)
			Typ[3]	Limit[4]	
P_{OUT}	Output Power	V_{DD} = 3.0V, f = 1kHz			
		Loudspeaker Mode (stereo) R_L = 4Ω, THD+N = 10% R_L = 4Ω, THD+N = 1% R_L = 8Ω, THD+N = 10% R_L = 8Ω, THD+N = 1%	 800 650 515 420		 mW mW mW mW
		Headphone Mode (stereo) R_L = 16Ω, THD+N = 1% R_L = 32Ω, THD+N = 1%	 32 33		 mW mW
		Earpiece Mode (mono) R_L = 16Ω, THD+N = 1% R_L = 32Ω, THD+N = 1%	 35 35		 mW mW
P_{OUT}	Output Power	V_{DD} = 3.6V, f = 1kHz			
		Loudspeaker Mode (stereo) R_L = 4Ω, THD+N = 10% R_L = 4Ω, THD+N = 1% R_L = 8Ω, THD+N = 10% R_L = 8Ω, THD+N = 1%	 1210 985 775 625	 540	 mW mW mW mW (min)
		Headphone Mode (stereo) R_L = 16Ω, THD+N = 1% R_L = 32Ω, THD+N = 1%	 41 45	 38	 mW mW (min)
		Earpiece Mode (mono), 0dB R_L = 16Ω, THD+N = 1% R_L = 32Ω, THD+N = 1%	 70 50	 45	 mW mW (min)
P_{OUT}	Output Power	V_{DD} = 5.0V, f = 1kHz			
		Loudspeaker Mode (stereo) R_L = 4Ω, THD+N = 10% R_L = 4Ω, THD+N = 1% R_L = 8Ω, THD+N = 10% R_L = 8Ω, THD+N = 1%	 2.43 1.97 1.54 1.23		 W W W W
		Headphone Mode (stereo), 0dB R_L = 16Ω, THD+N = 1% R_L = 32Ω, THD+N = 1%	 41 45		 mW mW
		Earpiece Mode (mono) R_L = 16Ω, THD+N = 1% R_L = 32Ω, THD+N = 1%	 170 90		 mW mW
THD+N	Total Harmonic Distortion + Noise	HP Mode (output mode 2) R_L = 16Ω, P_{OUT} = 20mW R_L = 32Ω, P_{OUT} = 20mW	 0.015 0.01		 % %
		LS Mode (output mode 2) R_L = 4Ω, P_{OUT} = 600mW/Ch R_L = 8Ω, P_{OUT} = 300mW/Ch	 0.03 0.02		 % %
		Earpiece Mode (output mode 1) Differential Input R_L = 16Ω, P_{OUT} = 50mW R_L = 32Ω, P_{OUT} = 30mW	 0.05 0.03		 % %

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Electrical Characteristics [1][2] (continued)

The following specifications apply for V_{DD} = $V_{DD(LS)}$ = $V_{DD(CP)}$ = 3.6V, all selectable gains = 0dB, $R_{L(LS)}$ = 8Ω (Note 8), $R_{L(HP)}$ = 32Ω, $R_{L(EP)}$ = 32Ω, f = 1kHz and the conditions shown in the "Typical Application Circuit" unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Tests Conditions	LM49250		Units (Limits)
			Typ[3]	Limit[4]	
e_N	Noise	Differential Inputs, A-weighted, A_V = 0dB			
		Headphone, A_V = 0dB HP Mode 2 HP Mode 7	 11 18		 µV µV
		Earpiece, A_V = 6dB EP Mode 1 EP Mode 3	 12 14		 µV µV
		Loudspeaker, A_V = 0dB LS Mode 2 LS Mode 7	 45 50		 µV µV
η	Efficiency	LS Mode, P_{OUT} = 500mW, V_{DD} = 3.6V	85		%
Xtalk	Crosstalk	LS Mode, f = 1kHz, R_L = 8Ω, V_{IN} = $1V_{P-P}$			
		Differential Input Mode	106		dB
		Single-Ended Input Mode	100		dB
		HP Mode, f = 1kHz, R_L = 32Ω, V_{IN} = $1V_{P-P}$			
		Differential Input Mode	94		dB
		Single-Ended Input Mode	91		dB
T_{ON}	Turn on Time	T_ON = 0 T_ON = 1	35 20		ms ms
Z_{IN}	Input Impedance	Maximum Gain Minimum Gain	17 200	±3.4 ±40	kΩ (max) kΩ (max)
Mute	Mute Attenuation	V_{IN} = $1V_{P-P}$			
		LS Mode	–94		dB
		HP Mode	–109		dB
		Earpiece Mode	–109		dB
CMRR	Common Mode Rejection Ratio	Differential Inputs,V_{IN} = $500mV_{PP}$, f = 217Hz, LS Mode (output mode 2) HP Mode (output mode 2) EP Mode (output mode 1)	 57 65 65		 dB dB dB
PSRR	Power Supply Rejection Ratio	Differential Inputs, V_{RIPPLE} = $200mV_{P-P}$			
		HP (output mode 1, 2, 3)			
		f = 217Hz	95		dB
		f = 1kHz	92		dB
		EP (output mode 1)			
		f = 217Hz	96		dB
		f = 1kHz	94		dB
		LS (output mode 1, 2)			
		f = 217Hz	70		dB
		f = 1kHz	70		dB
PSRR	Power Supply Rejection Ratio	Differential Inputs, V_{RIPPLE} = $200mV_{P-P}$			
		EP Mode = 3			
		f = 217Hz	92		dB
		f = 1kHz	89		dB
		LS Mode = 3			
		f = 217Hz	70		dB
		f = 1kHz	70		dB

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Electrical Characteristics [1][2] (continued)

The following specifications apply for V_{DD} = $V_{DD(LS)}$ = $V_{DD(CP)}$ = 3.6V, all selectable gains = 0dB, $R_{L(LS)}$ = 8Ω (Note 8), $R_{L(HP)}$ = 32Ω, $R_{L(EP)}$ = 32Ω, f = 1kHz and the conditions shown in the "Typical Application Circuit" unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Tests Conditions	LM49250		Units (Limits)
			Typ[3]	Limit[4]	
PSRR	Power Supply Rejection Ratio	Single-Ended Inputs, V_{RIPPLE} = 200mV_{P-P}			
		HP (output mode 2, 3)			
		f = 217Hz	84		dB
		f = 1kHz	81		dB
		LS (output mode 2)			
		f = 217Hz	69.1		dB
		f = 1kHz	68.1		dB
		EP (output mode 2)			
		f = 217Hz	78		dB
		f = 1kHz	76		dB

Control Interface Electrical Characteristics [1][2]

The following specifications apply for 2.7V ≤ V_{DD} ≤ 5.5V, and 1.7V ≤ I^2CV_{DD} ≤ 2.2V, unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM49250		Units (Limits)
			Typ[3]	Limit[4]	
t_1	SCL Period			2.5	µs (min)
t_2	SDA Set-up Time			250	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	SDA Hold time			250	ns (min)
V_{IH}	Digital Input High Voltage			0.7*I^2CV_{DD}	V (min)
V_{IL}	Digital Input Low Voltage			0.3*I^2CV_{DD}	V (max)
$\overline{RESET}_{IH}$	Reset Input High Voltage			1.6	V (min)
$\overline{RESET}_{IL}$	Reset Input Low Voltage			0.6	V (max)

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

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(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are ensured by test or statistical analysis.

The following specifications apply for 2.7V ≤ V_{DD} ≤ 5.5V, and 2.2V ≤ I^2CV_{DD} ≤ 5.5V, unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM49250		Units (Limits)
			Typ[1]	Limit[2]	
t_1	SCL Period			2.5	µs (min)
t_2	SDA Set-up Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)

(1) Typical values represent most likely parametric norms at T_A = +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(2) Datasheet min/max specification limits are ensured by test or statistical analysis.

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The following specifications apply for 2.7V ≤ V_{DD} ≤ 5.5V, and 2.2V ≤ I^2CV_{DD} ≤ 5.5V, unless otherwise specified. Limits apply for T_A = 25°C.

Parameter		Test Conditions	LM49250		Units (Limits)
			Typ(1)	Limit(2)	
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	SDA Hold Time			100	ns (min)
V_{IH}	Digital Input High Voltage			$0.7*I^2CV_{DD}$	V (min)
V_{IL}	Digital Input Low Voltage			$0.3*I^2CV_{DD}$	V (max)
$\overline{RESET}_{IH}$	Reset Input High Voltage			1.6	V (min)
$\overline{RESET}_{IL}$	Reset Input Low Voltage			0.6	V (max)

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Typical Performance Characteristics

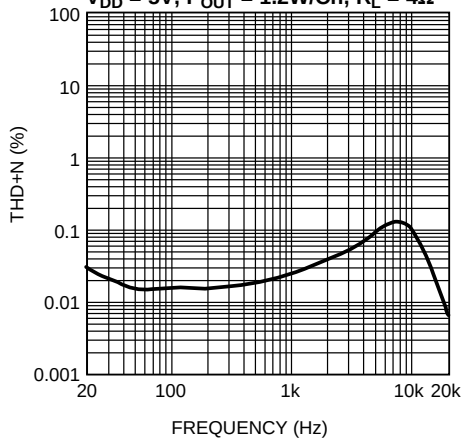


Figure 4.

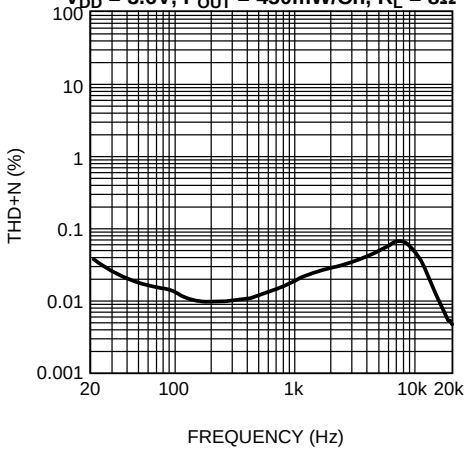


Figure 5.

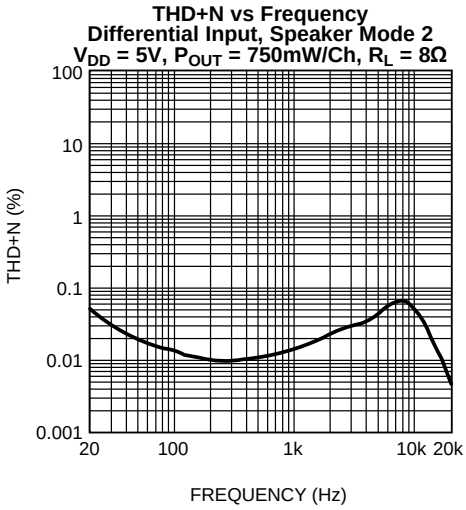
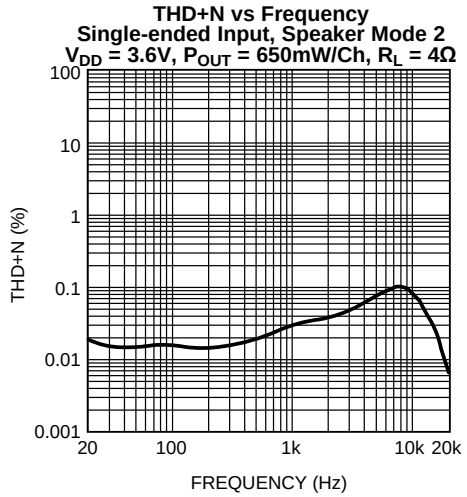


Figure 6.



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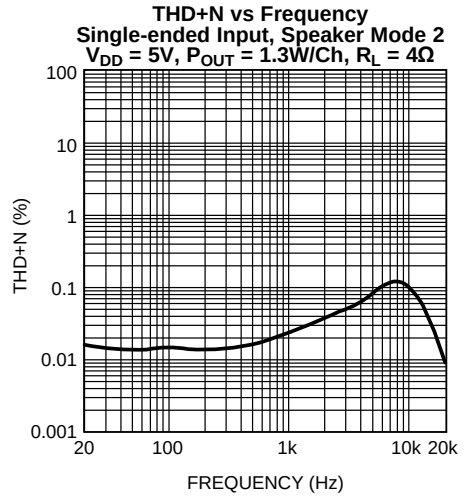

Figure 8.

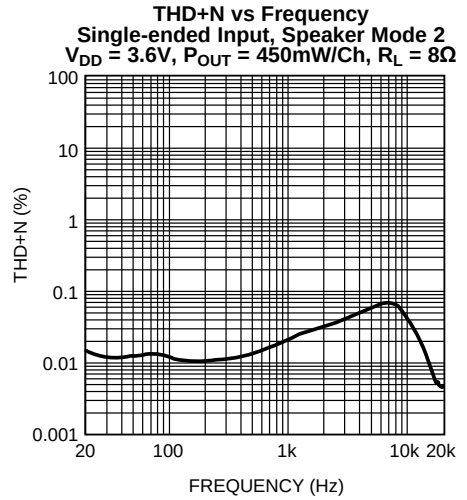

Figure 9.

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Typical Performance Characteristics (continued)

THD+N vs Frequency
Single-ended Input, Speaker Mode 2
V_{DD} = 5V, P_{OUT} = 800mW/Ch, R_L = 8Ω

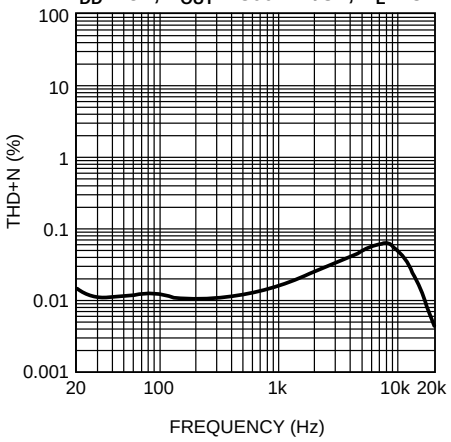

Figure 10.

THD+N vs Frequency
Differential Input, Headphone Mode 2
V_{DD} = 3.6V, P_{OUT} = 30mW/Ch, R_L = 16Ω

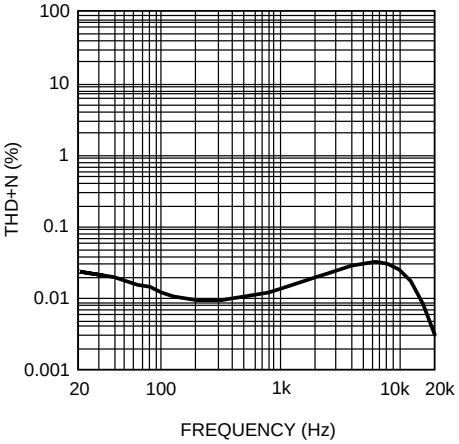

Figure 11.

THD+N vs Frequency
Differential Input, Headphone Mode 2
V_{DD} = 3.6V, P_{OUT} = 30mW/Ch, R_L = 32Ω

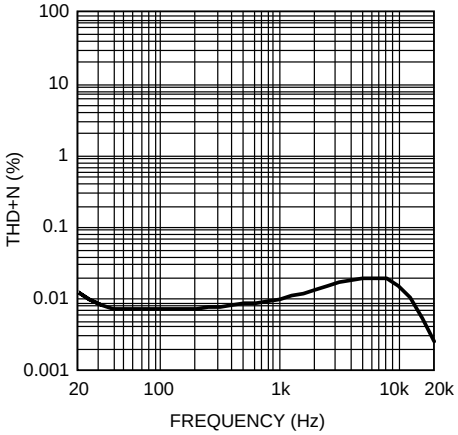

Figure 12.

THD+N vs Frequency
Single-ended Input, Headphone Mode 2
V_{DD} = 3.6V, P_{OUT} = 30mW, R_L = 16Ω

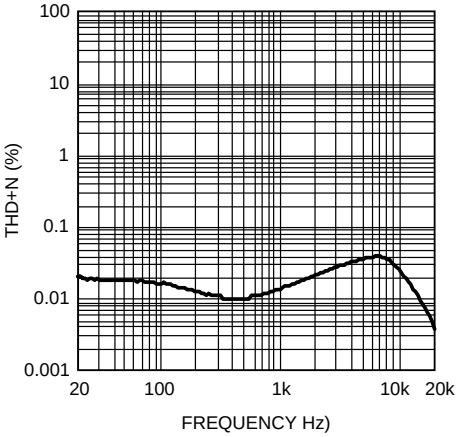

Figure 13.

THD+N vs Frequency
Single-ended Input, Headphone Mode 2
V_{DD} = 3.6V, P_{OUT} = 30mW, R_L = 32Ω

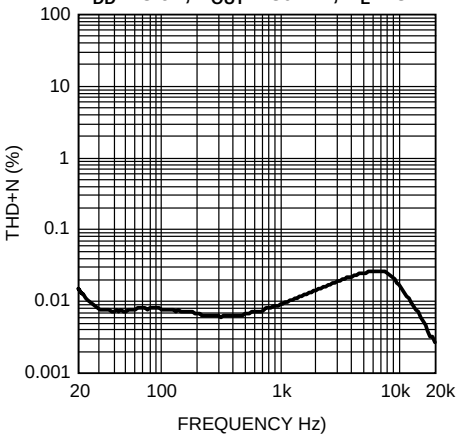

Figure 14.

THD+N vs Output Power
Differential Input, Speaker Mode 2
A_V = 0dB, R_L = 4Ω, f = 1kHz

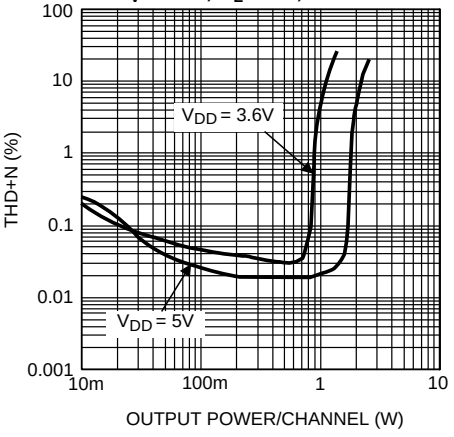

Figure 15.

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Typical Performance Characteristics (continued)

THD+N vs Output Power
Differential Input, Speaker Mode 2
A_V = 0dB, R_L = 8Ω, f = 1kHz

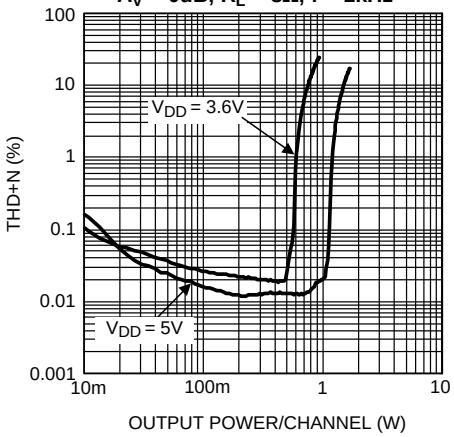

Figure 16.

THD+N vs Output Power
Single-ended Input, Speaker Mode 2
A_V = 6dB, R_L = 4Ω, f = 1kHz

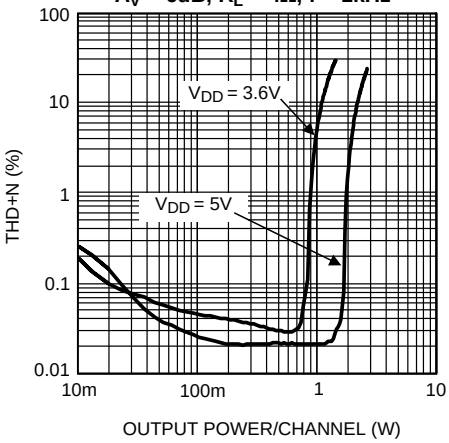

Figure 17.

THD+N vs Output Power
Single-ended Input, Speaker Mode 2
A_V = 6dB, R_L = 8Ω, f = 1kHz

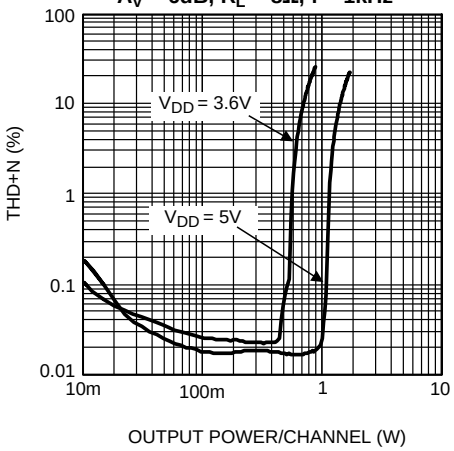

Figure 18.

THD+N vs Output Power
Differential Input, Headphone Mode 2
V_{DD} = 3.6V, A_V = 0dB, R_L = 16Ω, f = 1kHz

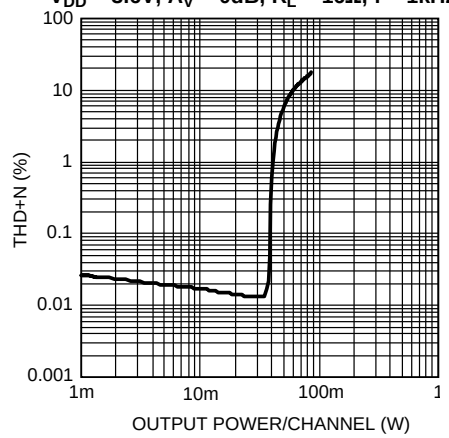

Figure 19.

THD+N vs Output Power
Differential Input, Headphone Mode 2
V_{DD} = 3.6V, A_V = 0dB, R_L = 32Ω, f = 1kHz

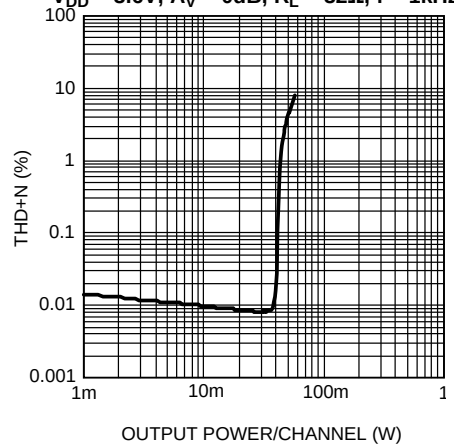

Figure 20.

THD+N vs Output Power
Single-ended Input, Headphone Mode 2
V_{DD} = 3.6V, A_V = 0dB, R_L = 16Ω, f = 1kHz

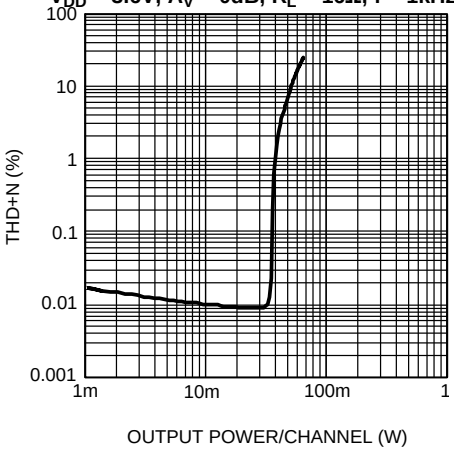

Figure 21.

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Typical Performance Characteristics (continued)

THD+N vs Output Power
Single-ended Input, Headphone Mode 2
V_{DD} = 3.6V, A_V = 0dB, R_L = 32Ω, f = 1kHz

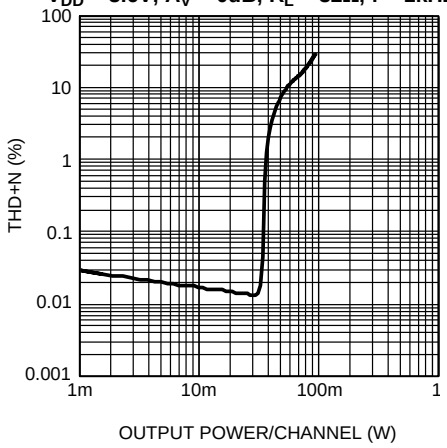

Figure 22.

THD+N vs Frequency
Differential Input, Earpiece Mode 1
V_{DD} = 3.6V, P_{OUT} = 40mW, R_L = 16Ω

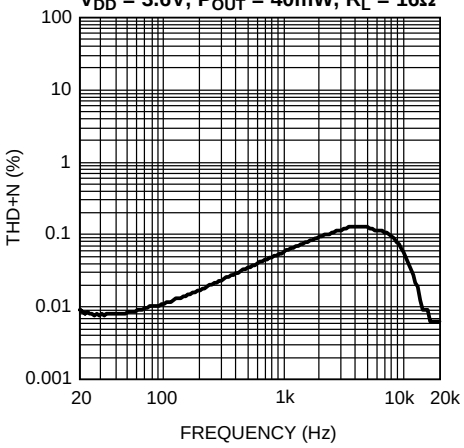

Figure 23.

THD+N vs Frequency
Differential Input, Earpiece Mode 1
V_{DD} = 5V, P_{OUT} = 140mW, R_L = 16 Ω

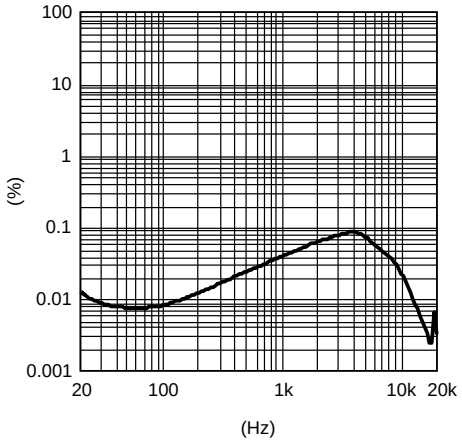

Figure 24.

THD+N vs Frequency
Differential Input, Earpiece Mode 1
V_{DD} = 3.6V, P_{OUT} = 65mW, R_L = 32Ω

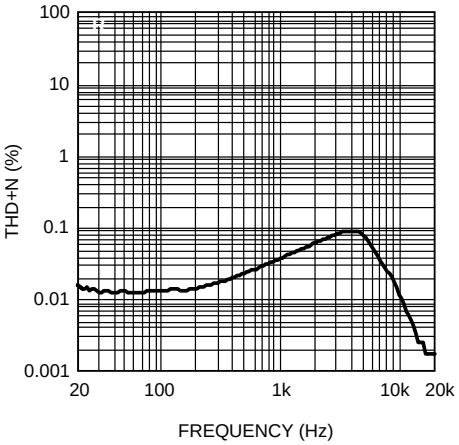

Figure 25.

THD+N vs Frequency
Differential Input, Earpiece Mode 1
V_{DD} = 5V, P_{OUT} = 160mW, R_L = 32Ω

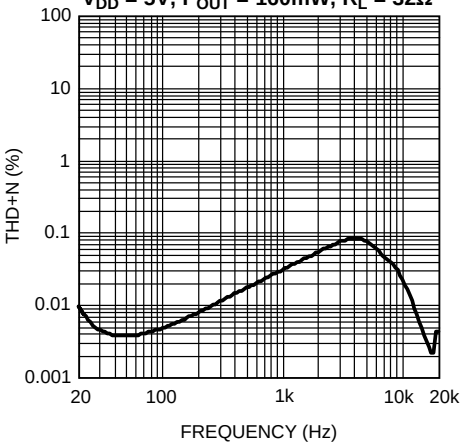

Figure 26.

THD+N vs Output Power
Differential Input, Earpiece Mode 1
A_V = 6dB, R_L = 16Ω, f = 1kHz

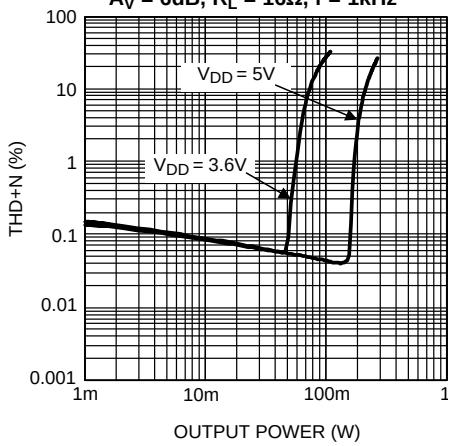

Figure 27.

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Typical Performance Characteristics (continued)

THD+N vs Output Power
Differential Input, Earpiece Mode 1
A_V = 6dB, R_L = 32Ω, f = 1kHz

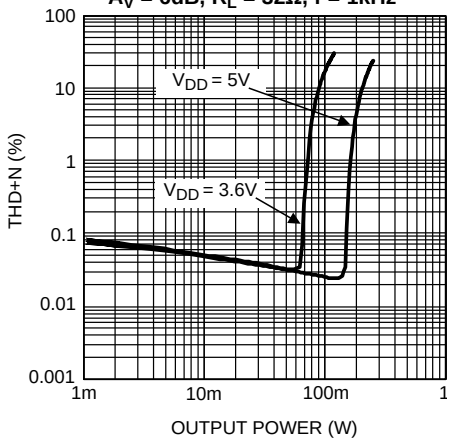

Figure 28.

Efficiency vs Output Power
Speaker Mode 2, R_L = 4Ω, f = 1kHz

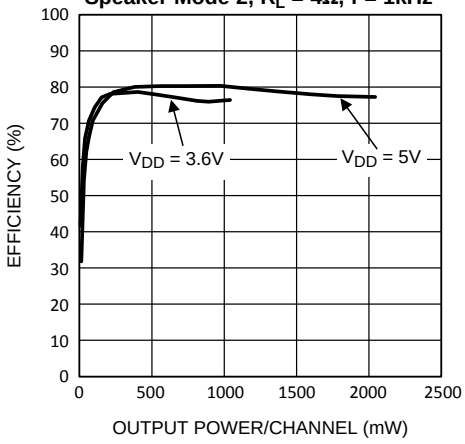

Figure 29.

Efficiency vs Output Power
Speaker Mode 2, R_L = 8Ω, f = 1kHz

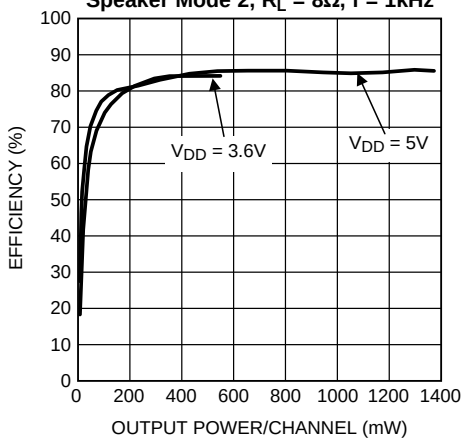

Figure 30.

Power Dissipation vs Output Power
Speaker Mode 2, R_L = 4Ω, f = 1kHz

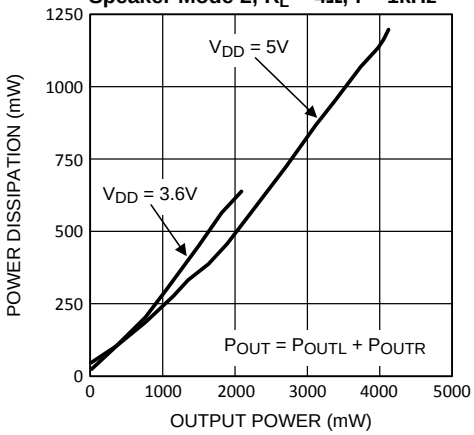

Figure 31.

Power Dissipation vs Output Power
Speaker Mode 2, R_L = 8Ω, f = 1kHz

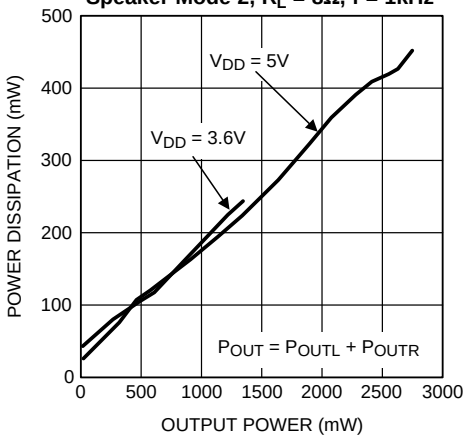

Figure 32.

Power Dissipation vs Output Power
Headphone Mode 2, V_{DD} = 3.6V
R_L = 16Ω, f = 1kHz

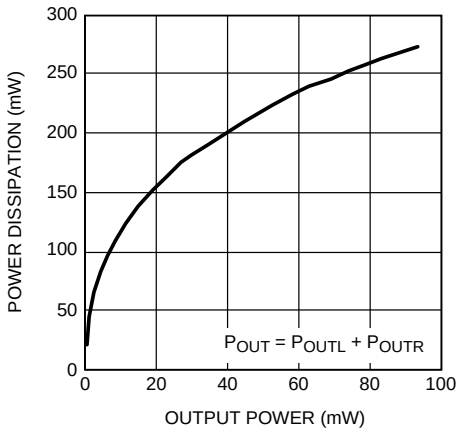

Figure 33.

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Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
Headphone Mode 2, V_{DD} = 3.6V
R_L = 32Ω, f = 1kHz

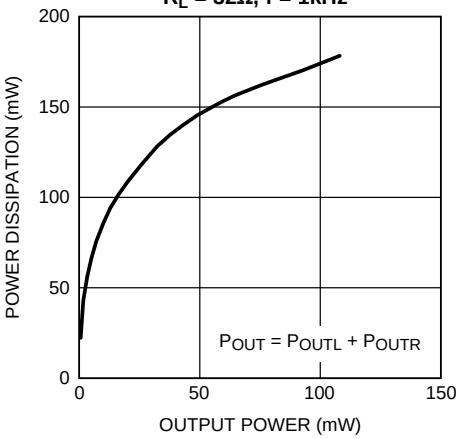

Figure 34.

Power Dissipation vs Output Power
Earpiece Mode 1, V_{DD} = 3.6V
R_L = 16Ω, f = 1kHz

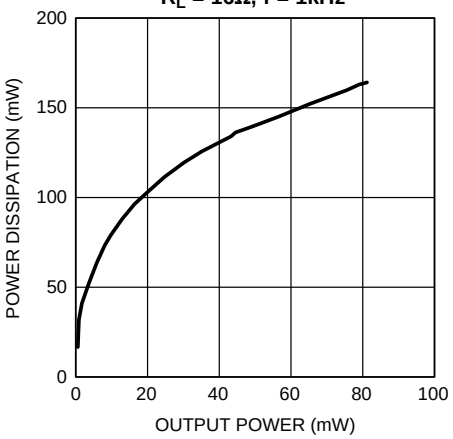

Figure 35.

Power Dissipation vs Output Power
Earpiece Mode 1, V_{DD} = 3.6V
R_L = 32Ω, f = 1kHz

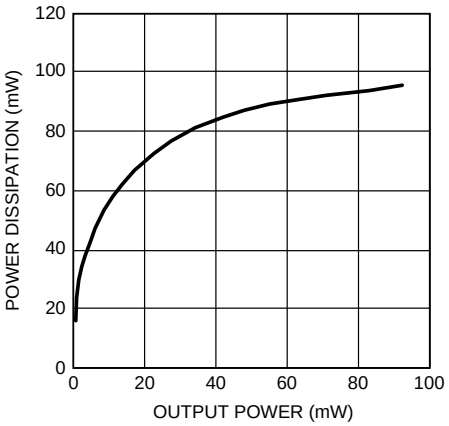

Figure 36.

PSRR vs Frequency
Differential Input, Speaker Mode 2
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω

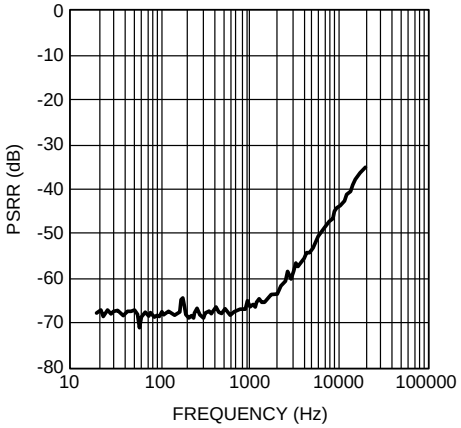

Figure 37.

PSRR vs Frequency
Differential Input, Speaker Output Mode 2
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω

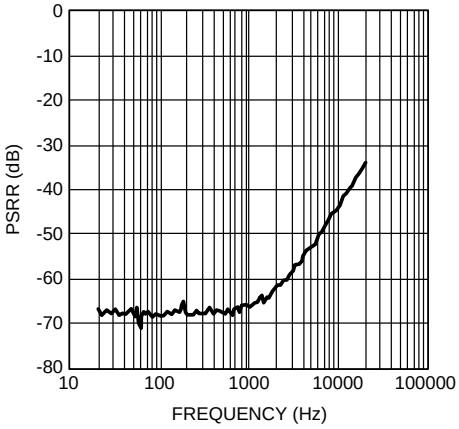

Figure 38.

PSRR vs Frequency
Differential Input, Earpiece Mode 1
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω

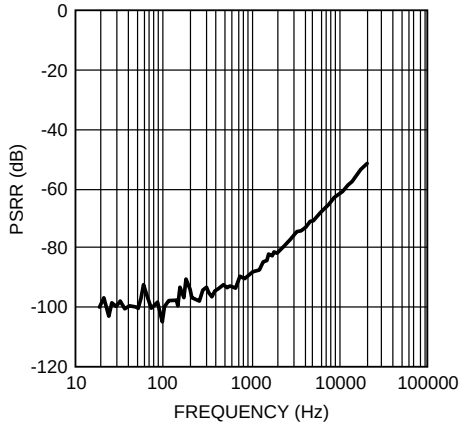

Figure 39.

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Typical Performance Characteristics (continued)

PSRR vs Frequency
Differential Input, Earpiece Output Mode 3
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω

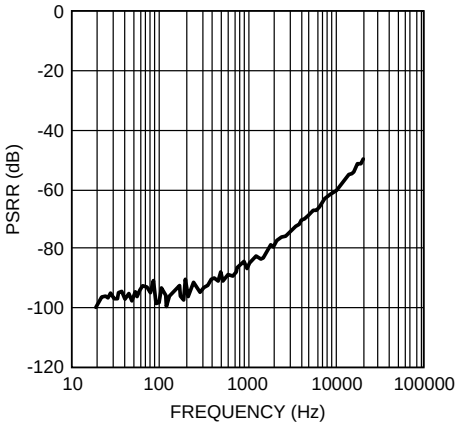

Figure 40.

PSRR vs Frequency
Single-Ended Input, Earpiece Mode 2, 3
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω

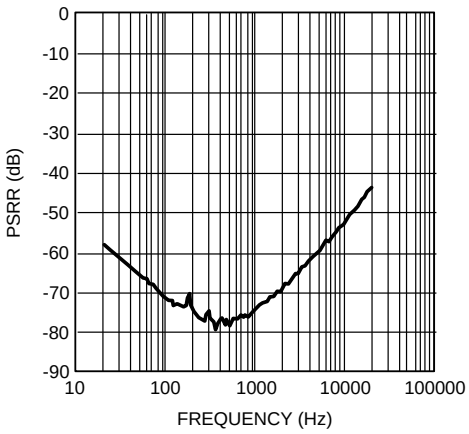

Figure 41.

PSRR vs Frequency
Single-Ended Input, Speaker Mode 3
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω

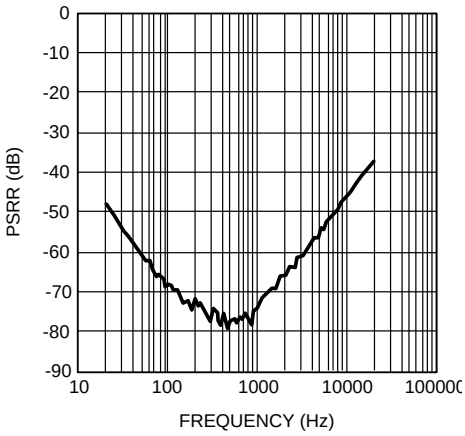

Figure 42.

PSRR vs Frequency
Differential Input, Headphone 2
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω

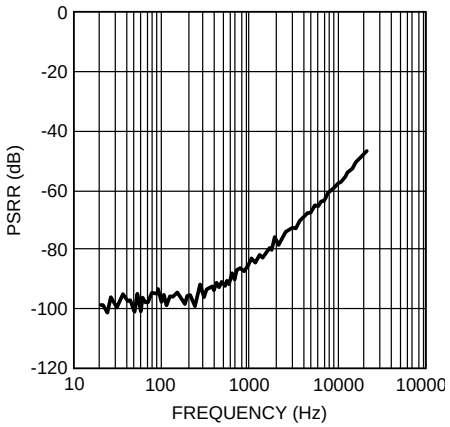

Figure 43.

PSRR vs Frequency
Single-Ended Input, Speaker Output Mode 2
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω

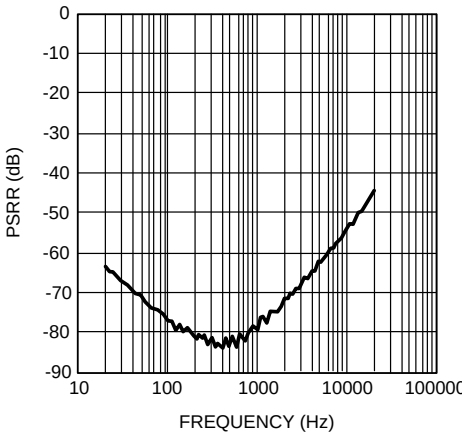

Figure 44.

CMRR vs Frequency
Speaker Output Mode 2
V_{DD} = 3.6V, V_{IN} = 500mV_{P-P}

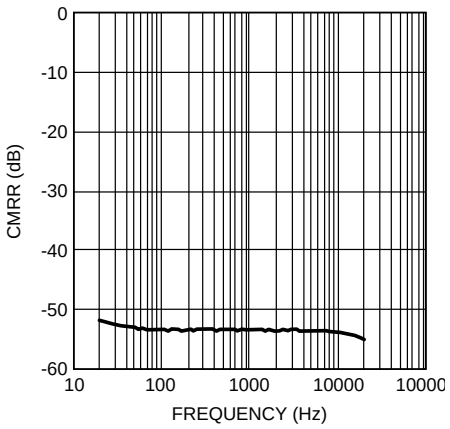

Figure 45.

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Typical Performance Characteristics (continued)

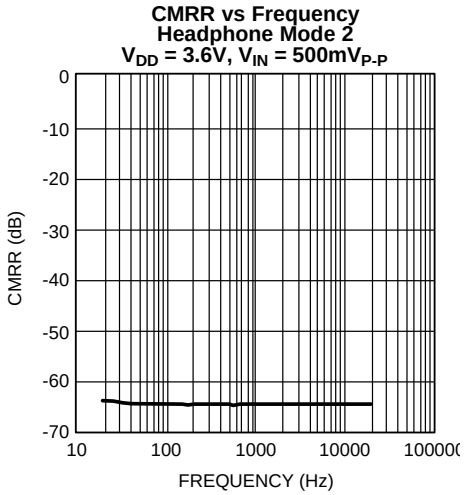

Figure 46.

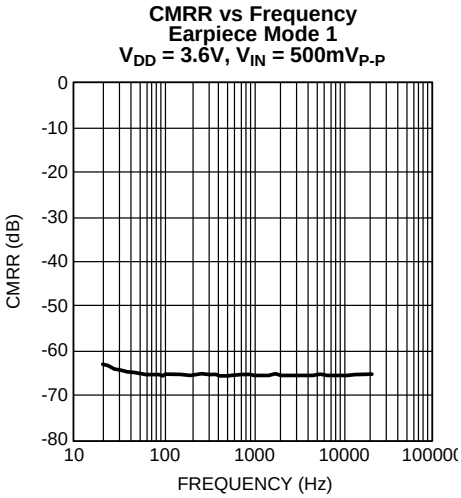

Figure 47.

APPLICATION INFORMATION

I²C COMPATIBLE INTERFACE

The LM49250 is controlled through an I²C compatible serial interface that consists of two wires; clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector) although the LM49250 does not write to the I²C bus. The maximum clock frequency specified by the I²C standard is 400kHz.

To avoid an address conflict with another device on the I²C bus, the LM49250 address is determined by the ADR pin, the state of ADR determines address bit A1 (Table 2). When ADR = 0, the address is 1111 1000. When ADR = 1 the device address is 1111 1010.

Table 2. Device Address

ADR	A7	A6	A5	A4	A3	A2	A1	A0
X	1	1	1	1	1	0	X	0
0	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	1	0

BUS FORMAT

The I²C bus format is shown in Figure 48. The “start” signal is generated by lowering the data signal while the clock is high. The start signal alerts all devices on the bus that a device address is being written to the bus.

The 8-bit device address is written to the bus next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock is high.

After the last address bit is sent, the master device releases the data line, during which time, an acknowledge clock pulse is generated. If the LM49250 receives the address correctly, then the LM49250 pulls the data line low, generating an acknowledge bit (ACK).

Once the master device has registered the ACK bit, the 8-bit register address/data word is sent. Each data bit should be stable while the clock level is high. After the 8–bit word is sent, the LM49250 sends another ACK bit. Following the acknowledgement of the data word, the master device issues a “stop” bit, allowing SDA to go high while the clock signal is high.

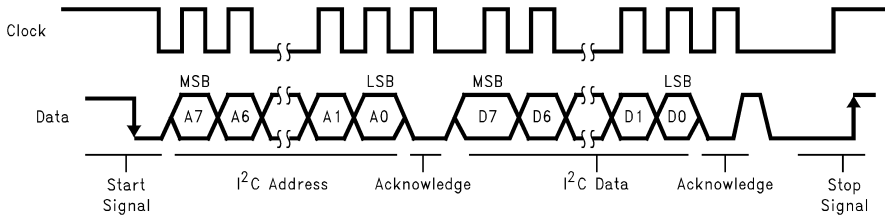

Figure 48. I²C Bus Format

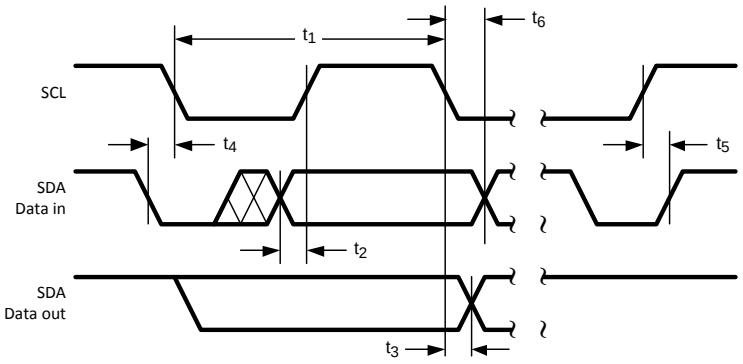

Figure 49. I²C Timing Diagram

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I²C RESET PIN

When the I²C RESET pin is pulled low, the device will go into shutdown and the PWR_ON bit (see Table 3) in the shutdown control register will reset. The device will remain in shutdown until an I²C command brings the device out of shutdown (see timing diagram in Figure 50). This pin can be connected to I^2CV_{DD} pin to prevent undefined and unwanted state changes that may occur when the I²C supply voltage is cycled.

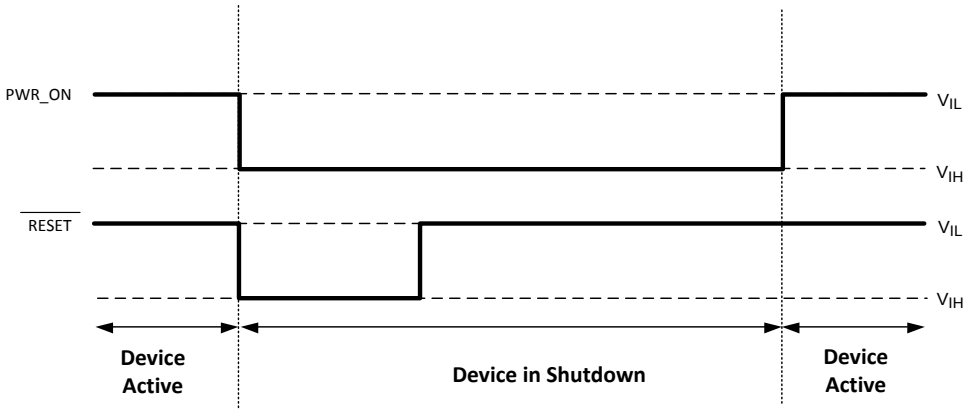

Figure 50. I²C Reset Timing Diagram

Table 3. I²C Control Registers

	REGISTER (#)	REGISTER NAME	D7	D6	D5	D4	D3	D2	D1	D0
C00	0	Shutdown Control	0	0	0	0	0	0	0	PWR_ON
C01	0.1	Stereo Input Mode Control	0	0	0	0	1	MUTE	L1_INSEL	L2_INSEL
C02	0.2	3D Control	0	0	0	1	0	3DN[1]	3DLS	3DHP
C03	0.3	3D Gain Control	0	0	0	1	1	0	3D_GAIN1	3D_GAIN0
C10	1	LDO Control	0	0	1	0	0	0	LDOH	T_ON
C11	1	Headphone Gain Control	0	0	1	0	1	HPG2	HPG1	HPG0
C12		Speaker Output Stage Gain Control	0	0	1	1	0	SS[2]	LSRG	LSLG
C13	1	Earpiece MUX/Gain COntrol	0	0	1	1	1	EP_GAIN	EP_MSEL	EP_SSEL
C2X	2	Speaker (LS) Output MUX Control	0	1	0	LS_XSEL	LSR_MSEL	LSR_SSEL	LSL_MSEL	LSL_SSEL
C3X	3	Headphone (HP) Output MUX Control	0	1	1	HP_XSEL	HP_MSEL	HPR_SSEL	HPL_MSEL	HP_LSSEL
C4X	4	Output On/Off Control	1	0	0	EP_ON	HPR_ON	HPL_ON	LRS_ON	LSL_ON
C5X	5	Mono Input Gain Control	1	0	1	MG4	MG3	MG2	MG1	MG0
C6X	6	Left Input Gain Control	1	1	0	LG4	LG3	LG2	LG1	LG0
C7X	7	Right Input Gain Control	1	1	1	RG4	RG3	RG2	RG1	RG0

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GENERAL AMPLIFIER FUNCTION

Class D Amplifier

The LM49250 features a high-efficiency, filterless, Class D stereo amplifier. The LM49250 Class D amplifiers feature a filterless modulation scheme. When there is no input signal applied, the outputs switch between V_{DD} and GND at a 50% duty cycle, with both outputs on, each channel in phase. Because the outputs of the LM49250 are differential and in phase, the result is zero net voltage across the speaker and no load current during the ideal state, thus conserving power. The switching frequency of each output is 300 kHz.

When an input signal is applied, the duty cycle (pulse width) changes. For increasing output voltages, the duty cycle of one output increases while the duty cycle of the other output decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage across the load.

Spread Spectrum

The LM49250 features a filterless spread spectrum modulation scheme. The switching frequency varies by ±30% about a 300kHz center frequency, reducing the wideband spectral content, reducing EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the LM49250 spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. In the Speaker Output Stage Gain control register, set SS = 1 to turn on the Spread Spectrum function.

Enhanced Emissions Suppression System (E^2S)

The LM49250 features TI's patent-pending E^2S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The LM49250 features advanced Edge Rate Control (ERC) that greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance. The overall result of the E^2S system is a filterless Class D amplifier that passes FCC Class B radiated emissions standards with 20 inches (50.8cm) of twisted pair cable, with excellent 0.02% THD+N and high 87% efficiency.

Differential Audio Amplifier Configuration

As logic supply voltages continue to shrink, system designers increasingly turn to differential signal handling to preserve signal to noise ratio with decreasing voltage swing. The LM49250 can be configured as a fully differential amplifier, amplifying the difference between the two inputs. The advantage of the differential architecture is any signal component that is common to both inputs is rejected, improving common-mode rejection (CMRR) and increasing the SNR of the amplifier by 6dB over a single-ended architecture. The improved CMRR and SNR of a differential amplifier reduce sensitivity to ground offset related noise injection, especially important in noisy applications such as cellular phones. Set bits L1_INSEL and L2_INSEL = 0 for differential input mode. The left and right stereo inputs have selectable differential or single-ended input modes, while the mono input is always differential.

Single-Ended Input Configuration

The left and right stereo inputs of the LM49250 can be configured for single-ended sources (Figure 51). In single-ended input mode, the LM49250 can accept up to 4 different single-ended audio sources. Set bits L1_INSEL = 1 and L2_INSEL = 0 to use the R1 and L1inputs. Set L1 _INSEL = 0 and L2_INSEL = 1 to use the R2 and L2 inputs. Set L1_INSEL = L2_INSEL = 1 to use both input pairs. Table 4 shows the available input combinations.

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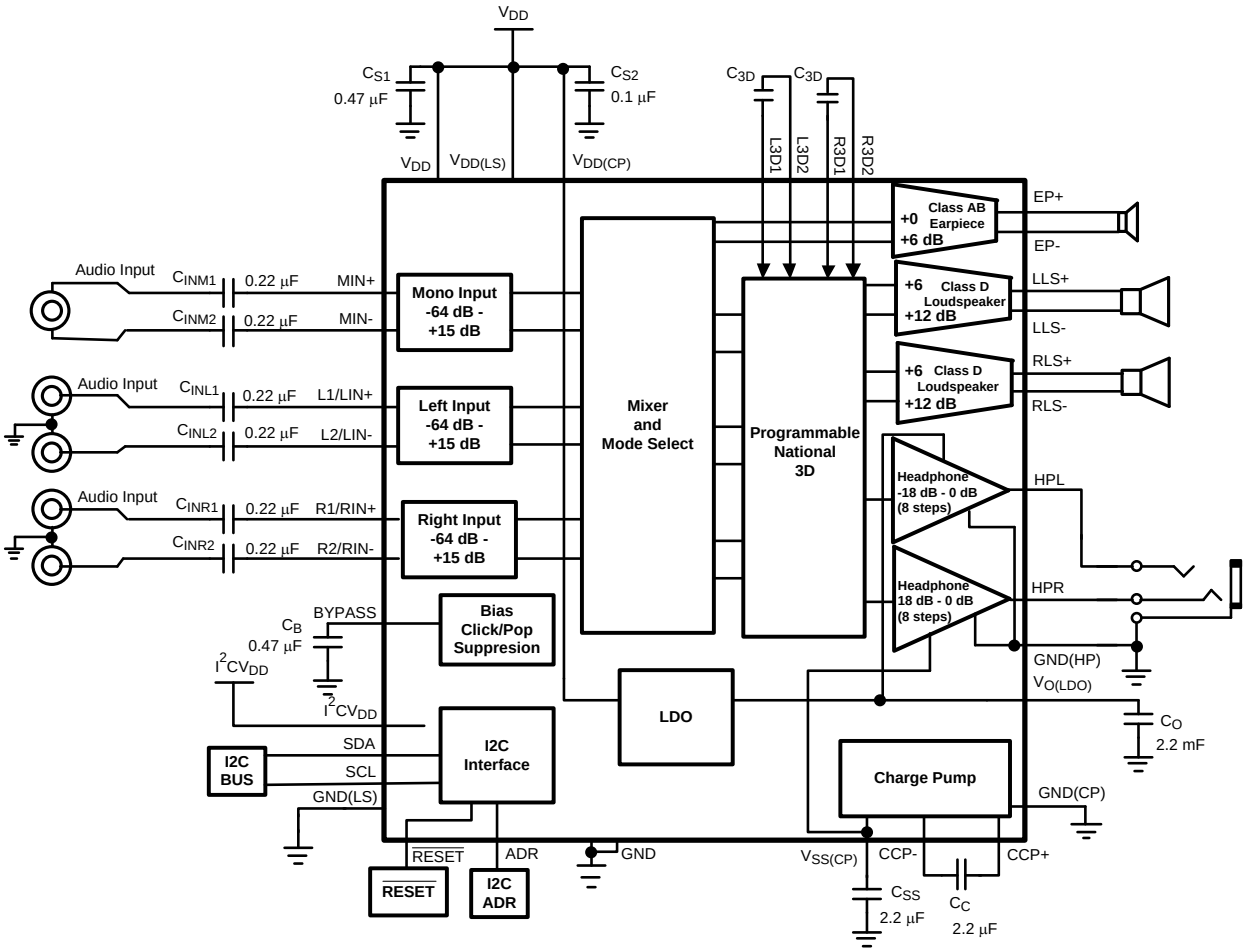

Figure 51. Single-Ended Input Configuration

Table 4. Stereo Input Modes

Input Mode	L1_INSEL	L2_INSEL	Input Description
0	0	0	Fully Differential Input Mode
1	0	1	Single-ended input. R2 and L2 selected
2	1	0	Single-ended input. R1 and L1 selected
3	1	1	Single-ended input. R1 mixed with R2 and L1 mixed with L2

Ground Reference Headphone Amplifier

The LM49250 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two, small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor form a high pass filter that

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not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49250 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49250 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

Charge Pump Capacitor Selection

For optimal performance, low (<100mΩ) ESR (equivalent series resistance) ceramic capacitors with X7R dielectric are recommended. Low ESR capacitors keep the charge pump output impedance to a minimum, extending the headroom on the negative supply. Higher ESR capacitors result in a reduction of output power from the audio amplifiers. Charge pump load regulation and output impedance are affected by the value of the flying capacitor (C_C). A larger valued C_C (up to 3.3µF) improves load regulation and minimizes charge pump output resistance. The switch-on resistance dominates the output impedance for capacitor values above 2.2µF.

The output ripple is affected by the value and ESR of the output capacitor (C_{SS}). Larger capacitors reduce output ripple on the negative power supply. Lower ESR capacitors minimize the output ripple and reduce the output impedance of the charge pump.

The LM49250 charge pump design is optimized for 2.2µF, low ESR ceramic capacitors for both C_C and C_{SS} (See Figure 1).

Input Mixer / Multiplexer

The LM49250 includes a comprehensive mixer/multiplexer controlled through the I^2C interface. **The mixer/multiplexer allows any input combination to appear on any output of the LM49250.** Control bits LSR_SSEL and LSL_SSEL (loudspeakers), and HPR_SSEL and HPL_SSEL (headphones) select the individual stereo input channels. For example, LSR_SSEL = 1 outputs the right channel stereo input on the right channel loudspeaker, while LSL_SSEL = 1 outputs the left channel stereo input on the left channel loudspeaker. Control bits LSR_MSEL and LSL_MSEL (loudspeaker), and HPR_MSEL and HPR_LSEL (headphones) direct the mono input to the selected output. Control bits LS_XSEL (loudspeaker) and HP_XSEL (headphone) selects both stereo input channels and directs the signals to the opposite outputs. For example, LS_XSEL = 1 outputs the right channel stereo input on the left channel loudspeaker, while the left channel stereo input is output on the right channel loudspeaker. Setting __XSEL selects both stereo inputs simultaneously, unlike the __SSEL controls which select the stereo input channels individually.

Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 5 and Table 6 show how the input signals are mixed together for each possible input selection combination.

Table 5. Loudspeaker Multiplexer Control

LS MODE	LS_XSEL	LSR_SSEL/ LSL_SSEL	LSR_MSEL/ LSL_MSEL	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
0	0	0	0	Mute	Mute
1	0	0	1	M	M
2	0	1	0	L'	R'
3	0	1	1	M + L'	M + R'
4	1	0	0	R'	L'
5	1	0	1	M + R'	M + L'
6	1	1	0	L' + R'	L' + R'
7	1	1	1	M + L' + R'	M + L' + R'

Table 6. Headphone Multiplexer Control

HPMODE	HP_XSEL	HPR_SSEL/ HPL_SSEL	HPR_MSEL/ HPL_MSEL	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
0	0	0	0	Mute	Mute
1	0	0	1	M	M
2	0	1	0	L'	R'

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Table 6. Headphone Multiplexer Control (continued)

HPMODE	HP_XSEL	HPR_SSEL/ HPL_SSEL	HPR_MSEL/ HPL_MSEL	LEFT CHANNEL OUTPUT	RIGHT CHANNEL OUTPUT
3	0	1	1	M + L'	M + R'
4	1	0	0	R'	L'
5	1	0	1	M + R'	M + L'
6	1	1	0	L' + R'	L' + R'
7	1	1	1	M + L' + R'	M + L' + R'

Table 7. Earpiece Multiplexer Control

EP MODE	EP_SSEL	EP_MSEL	MONO EARPIECE OUTPUT
0	0	0	Mute
1	0	1	Mono
2	1	0	L' + R'
3	1	1	M + L' + R'

LDO General Information

The LM49250 has different supplies for each portion of the device, allowing for the optimum combination of headroom, power dissipation and noise immunity. The speaker amplifiers are powered from $V_{DD(LS)}$. The ground reference headphone amplifiers are powered from the internal LDO. The separate power supplies allow the speakers to operate from a higher voltage for maximum headroom, while the headphone operate from a lower voltage, improving power dissipation.

Table 8. LDO Disabling Options

LDOH	HPR_ON/HPL_ON	PWR_ON	$V_{O(LDO)}$ (V)
0	0	X	0
0	1	1	2.25
0	1	0	0
1	X	0	V_{DD}
1	X	1	2.25

Shutdown Function

The LM49250 features six shutdown modes, configured through the I^2C interface. Bit D0 (PWR_ON) in the Shutdown Control register controls the shutdown function of the entire device. Set PWR_ON = 1 to enable the LM49250, set PWR_ON = 0 to disable the device. Bits D0 – D4 in the Output On/Off Control register controls the shutdown function of the individual output channels. EP_ON (D4) controls the earpiece output, HPR_ON (D3) controls the right channel headphone output, HPL_ON (D2) controls the left channel headphone output, LSR_ON (D1) controls the right channel loudspeaker output, and LRL_ON (D0) controls the left channel loudspeaker output. The PWR_ON bit takes precedence over the individual channel controls.

TI 3D Enhancement

The LM49250 features a stereo headphone, 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement creates a perceived spatial effect optimized for stereo headphone listening. The 3D function can be controlled from the 3D control register. Set 3DLS = 0 to disable the loudspeaker 3D; set 3DLS = 1 to enabel the loudspeaker 3D. Similarly, to enable the headphone, set 3DHP = 1 and to disable, set 3DHP = 0.

The LM49250 can be programmed for a “narrow” (3DN = 1) or “wide”(3DN = 0) soundstage perception. The narrow soundstage has a more focused approaching sound direction, while the wide soundstage has a spatial, theater-like effect. Within each of these two modes, four discrete levels of 3D effect that can be programmed: low, medium, high, and maximum (Table 9). The difference between each level is 3dB with an ever increasing aural effect with increased level.

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The external capacitors, shown in Figure 51, are required to enable the 3D effect. The value of the capacitors set the cutoff frequency of the 3D effect, as shown by Equation 1 and Equation 2. Note that the internal 40kΩ resistor is nominal.

Table 9. Programmable Texas Instruments 3D Audio

3D Mixing Level	3D-GAIN1	3D_GAIN0
Low	0	0
Medium	0	1
High	1	0
Maximum	1	1

Table 10. 3D Audio Control

3D Function	3DHP / 3DLS
HP/LS 3D ON	1
HP/LS 3D OF	0

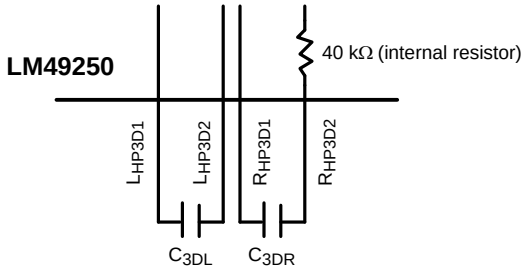

Figure 52. External RC Network with Optional $R_{3DL}$and R_{3DR}

$$f_{3DL}(–3dB) = 1 / (2\pi \times 40k\Omega \times C_{3DL}) \quad (Hz) \tag{1}$$

$$f_{3DR}(–3dB) = 1 / (2\pi \times 40k\Omega \times C_{3DR}) \quad (Hz) \tag{2}$$

Optional resistors R_{3DL} and R_{3DR} can also be added (Figure 52) to affect the -3dB frequency and 3D magnitude.

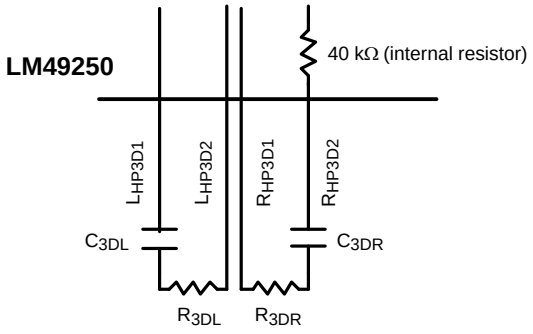

Figure 53. External 3D Effect Capacitors

$$f_{3DL}(–3dB) = 1 / [2\pi \times (40k\Omega + R_{3DL}) \times C_{3DL}] \quad (Hz) \tag{3}$$

$$f_{3DR}(–3dB) = 1 / [2\pi \times (40k\Omega + R_{3DR}) \times C_{3DR}] \quad (Hz) \tag{4}$$

ΔAV (change in AC gain) = 1 / 1 + M, where M represents some ratio of the nominal internal resistor, 40kΩ (see example below Table 9).

$$f_{3dB}(3D) = 1 / [2\pi (1+ M) (40k\Omega \times C_{3D})] \quad (Hz) \tag{5}$$

$$C_{EQUIVALENT}(new) = C_{3D} / (1 + M) \quad (F) \tag{6}$$

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Audio Amplifier Gain Setting

Each channel of the LM49250 has two separate gain stages. Each input stage features a 32 step volume control (Input Mode 0 & 3) with a range of -64dB to +15dB (Table 11). Each loud speaker output stage has 2 gain settings (Table 12); 6dB and 12dB when either a fully differential signal or two single-ended signals are applied on the R1/L1 and R2/L2 pins Each headphone output stage has 8 gain settings (Table 13), 0dB, -1.2 dB,-2.5dB, -4dB, -6dB, -8.5dB, -12dB and -18dB. In single-ended input mode with only one signal applied (Input Mode 1 & 2), the loud speaker and headphone output stage gain settings are increased by 6dB (Table 11). This allows for a maximum separation of 30dB between the speaker and headphone outputs when both are active. The mono input channel is not affected by L1_INSEL and L2_INSEL, and is always configured as a differential input.

Calculate the total gain of a given signal path as follows:

$$A_{VOL} + A_{OS} = A_{TOTAL} \text{ (dB)} \quad (7)$$

where:

A_{VOL} is the volume control level

A_{OS} is the gain setting of the output stage

A_{TOTAL} is the total gain for the signal path

Table 11. 32 Step Volume Control

Volume Step	MG4/LG4/RG4	MG3/LG3/RG3	MG2/LG2/RG2	MG1/LG1/RG1	MG0/LG0/RG0	Gain (dB) (Input Mode 0 & 3)	Gain (dB) (Input Mode 1 & 2)
0	0	0	0	0	0	–64	–58
1	0	0	0	0	1	–54.5	–48.5
2	0	0	0	1	0	–47	–41
3	0	0	0	1	1	–40	–34
4	0	0	1	0	0	–33	–27
5	0	0	1	0	1	–28	–21
6	0	0	1	1	0	–24	–18
7	0	0	1	1	1	–21	–15
8	0	1	0	0	0	–19.5	–13.5
9	0	1	0	0	1	–18	–12
10	0	1	0	1	0	–16.5	–10.5
11	0	1	0	1	1	–15	–9
12	0	1	1	0	0	–13.5	–7.5
13	0	1	1	0	1	–12	–6
14	0	1	1	1	0	–10.5	–4.5
15	0	1	1	1	1	–9.0	–3
16	1	0	0	0	0	–7.5	–1.5
17	1	0	0	0	1	–6	0
18	1	0	0	1	0	–4.5	2.5
19	1	0	0	1	1	–3	3
20	1	0	1	0	0	1.5	4.5
21	1	0	1	0	1	0	6
22	1	0	1	1	0	1.5	7.5
23	1	0	1	1	1	3	9
24	1	1	0	0	0	4.5	10.5
25	1	1	0	0	1	6	12
26	1	1	0	1	0	7.5	13.5
27	1	1	0	1	1	9	15
28	1	1	1	0	0	10.5	16.5
29	1	1	1	0	1	12	18

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Table 11. 32 Step Volume Control (continued)

Volume Step	MG4/LG4/RG4	MG3/LG3/RG3	MG2/LG2/RG2	MG1/LG1/RG1	MG0/LG0/RG0	Gain (dB) (Input Mode 0 & 3)	Gain (dB) (Input Mode 1 & 2)
30	1	1	1	1	0	13.5	19.5
31	1	1	1	1	1	15	21

Table 12. Loudspeaker Gain Setting

LSRG/LSLG	Gain (dB)
0	6
1	12

Table 13. Headphone Gain Setting

HPG2	HPG1	HPG0	Gain (dB)
0	0	0	0
0	0	1	–1.2
0	1	0	–2.5
0	1	1	–4
1	0	0	–6
1	0	1	–8.5
1	1	0	–12
1	1	1	–18

Table 14. EP_Gain

EP_Gain	Gain (dB)
0	0
1	6

Power Dissipation and Efficiency

The major benefit of a Class D amplifier is increased efficiency versus Class AB. The efficiency of the LM49250 speaker amplifiers is attributed to the output transistors' region of operation. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to their Class AB counterparts. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET on-resistance, along with the switching losses due to gate charge.

The maximum power dissipation per ground referenced headphone channel is given by:

$$P_{DMAX\text{-}HP} = V_{DD}^2 / 2\pi^2 R_L + (I_{DDQ} * V_{DD}) \text{ (W)} \quad (8)$$

The maximum power dissipation for the mono BTL earpiece output is given by:

$$P_{DMAX\text{-}EP} = 4V_{DD}^2 / 2\pi^2 R_L + (I_{DDq} * V_{DD}) \quad (9)$$

Refer to the Typical Performance Characteristics curves for power dissipation information at various power levels.

Audio Amplifier Power Supply Bypassing / Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Typical applications employ a voltage regulator with 10µF and 0.1µF bypass capacitors that increase supply stability. These capacitors do not eliminate the need for bypassing of the LM49250 supply pins. A 1µF ceramic capacitor placed close to each supply pin is recommended.

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Bypass Capacitor Selection

The LM49250 generates a $V_{DD}/2$ common-mode bias voltage internally. The BYPASS capacitor, C_B, improves PSRR and THD+N by reducing noise at the BYPASS node. Use a 4.7µF capacitor, placed as close to the device as possible for C_B.

Audio Amplifier Input Capacitor Selection

Input capacitors, C_{IN}, in conjunction with the input impedance of the LM49250 forms a high-pass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimal DC level. Assuming zero source impedance, the -3dB point of the high-pass filter is given by:

$$f_{-3dB} = 1 / [2\pi R_{IN} C_{IN}] \quad (Hz) \tag{10}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with low voltage coefficient dielectrics, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Other factors to consider when designing the input filter include the constraints of the overall system. Although high fidelity audio requires a flat frequency response between 20Hz and 20kHz, portable devices such as cell phones may only concentrate on the frequency range of the spoken human voice (typically 300Hz to 4kHz). In addition, the physical size of the speakers used in such portable devices limits the low frequency response; in this case, frequencies below 150Hz may be filtered out.

EVALUATION BOARD

For information on the evaluation board, refer to Application Note AN-1680 (Literature Number SNAA048).

PCB LAYOUT GUIDELINES

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM49250 and the load results in decreased output power and efficiency. Trace resistance between the power supply and GND of the LM49250 has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power-supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer.

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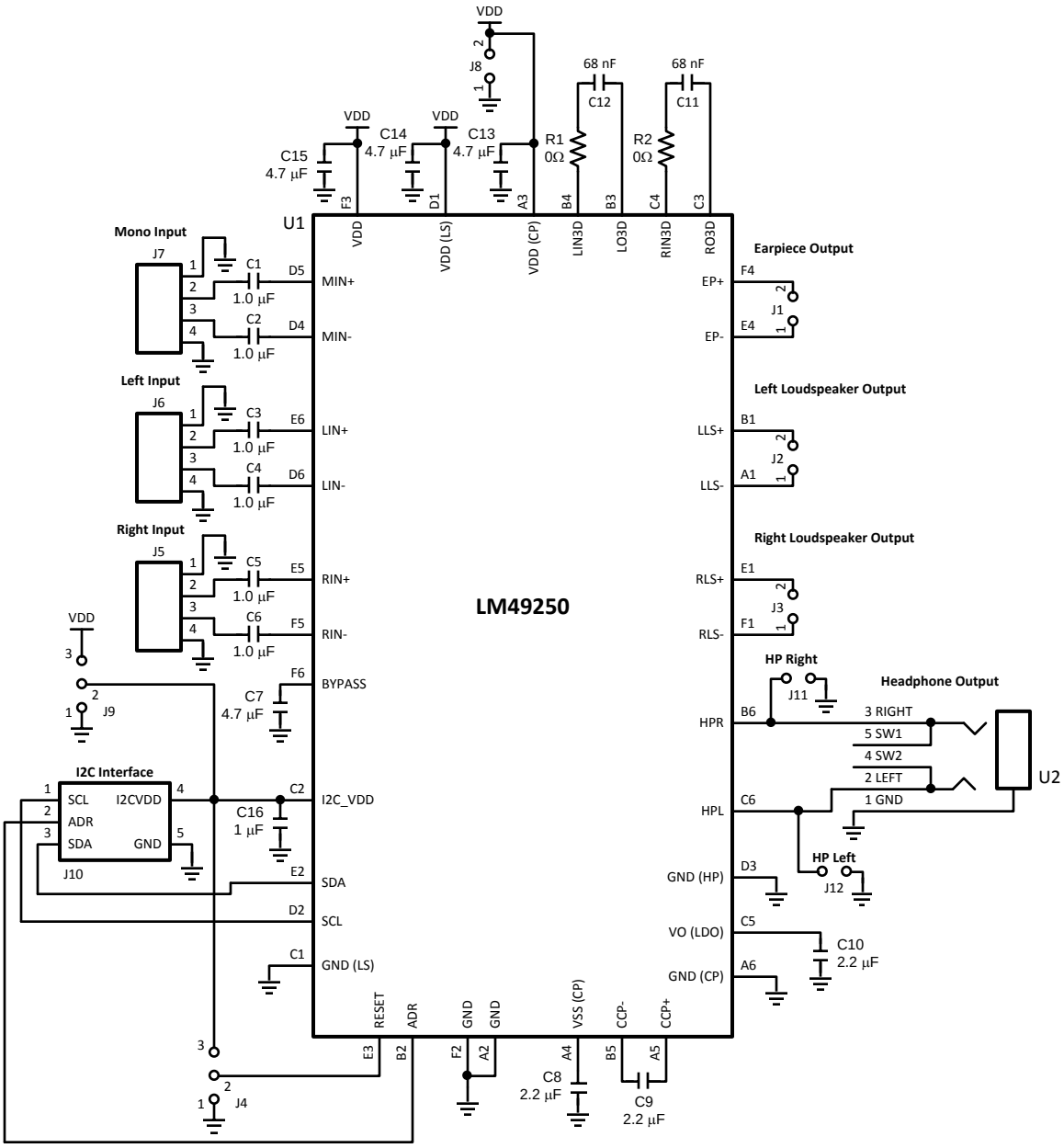
Demo Board Schematic



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Demo Board Layout

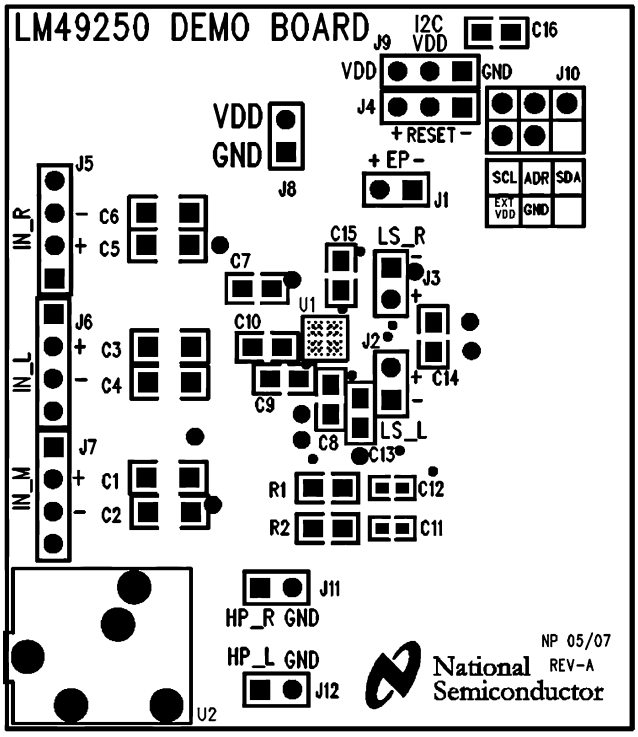

Figure 54. Top Silkscreen

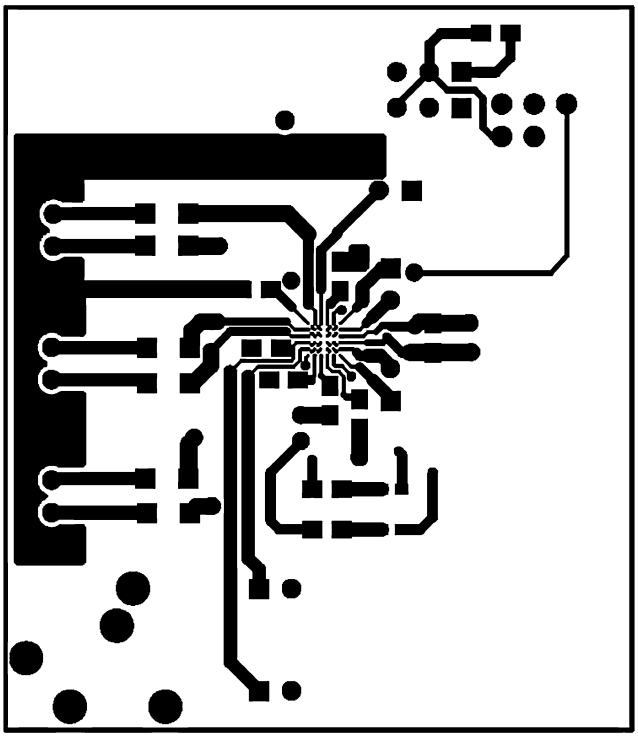

Figure 55. Top Layer

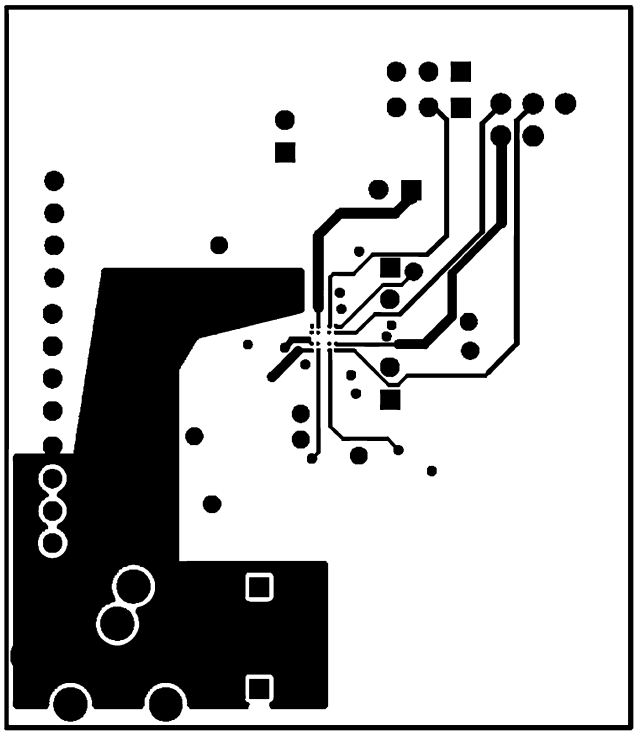

Figure 56. Layer 2

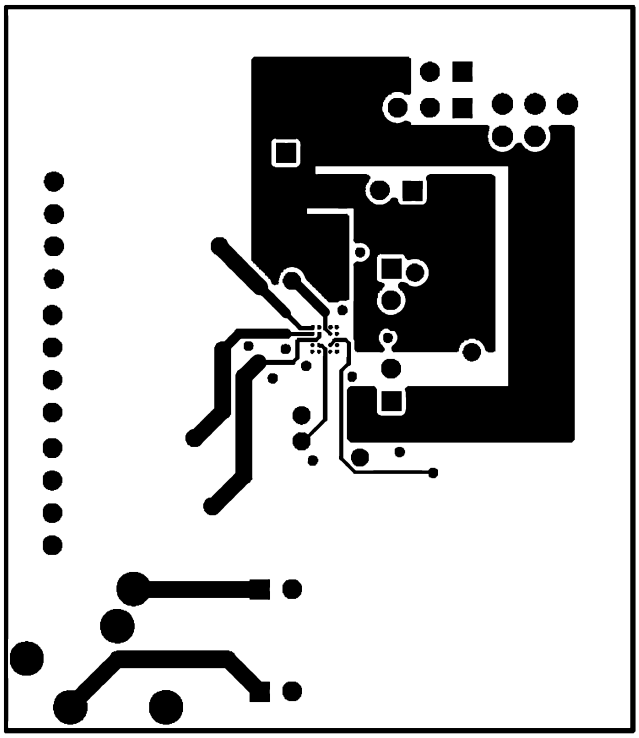

Figure 57. Layer 3

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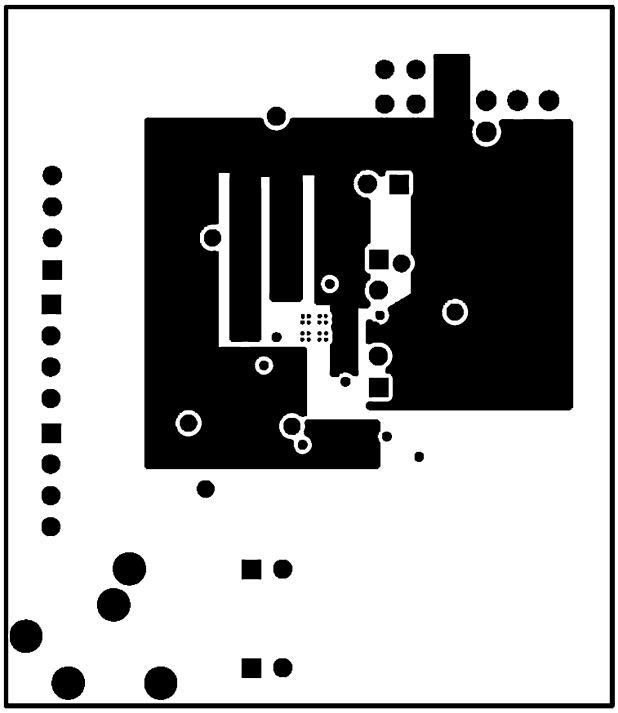

Figure 58. Bottom Layer

LM49250 Build of Materials

Part Description	Qty	Ref Designator	Manufacturer	Part Number
LM49250 DEMO BOARD	1			
LM49250TL	1	U1		
CAP CER 1UF 16V X7R 1206 10%	6	C1–C6	muRata	GRM319R71C105KC11D
CAP CER 4.7UF 16V X7R 0805	4	C7, C13, C14, C15	muRata	GRM21BR71C475KA73L
CAP CER 2.2UF 16V X5R 0805	3	C8, C9, C10	muRata	GRM21BR61C225KA88L
CAP CER 68nF 16V X7R 0805	2	C11, C12	muRata	GRM188R71C683KA01D
CAP CER 1UF 16V X7R 0805	1	C16	muRata	GRM21BR71C105KA01L
RES 0OHM 1/8W 5% 0805 SMD	1	R1, R2	Vishay/Dale	CRCW08050000Z0EA
Jumper Header Vertical Mount 2X1 0.100	7	J1, J2, J3, J8, J11, J12, J10 (bottom)		
Jumper Header Vertical Mount 4X1 0.101	3	J5, J6, J7		
Jumper Header Vertical Mount 3X1 0.102	2	J9, J4, J10 (top)		
Headphone Jack	1	U2		

Revision History

Rev	Date	Description
1.0	01/23/08	Initial release.
1.01	09/19/08	Text edits.
1.02	12/15/08	Changed the limit on Pout (V_{DD} = 3.6V, Loudspeaker mode, R_l = 8Ω, 1% THD) form 500 to 540.
C	05/03/13	Changed layout of National Data Sheet to TI format.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM49250RL/NOPB	ACTIVE	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GJ1	Samples
LM49250RLX/NOPB	ACTIVE	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GJ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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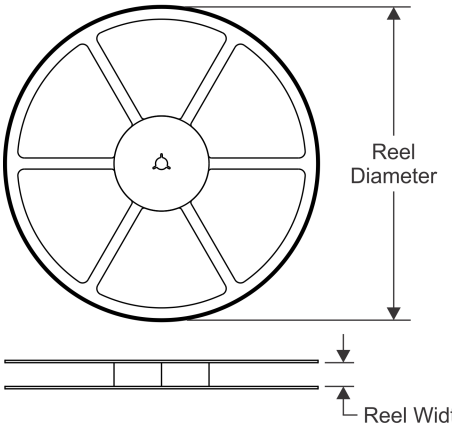
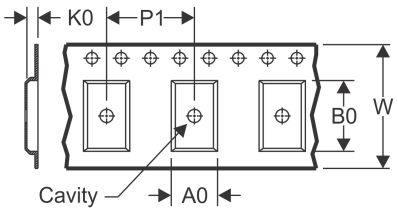
TAPE AND REEL INFORMATION

REEL DIMENSIONS

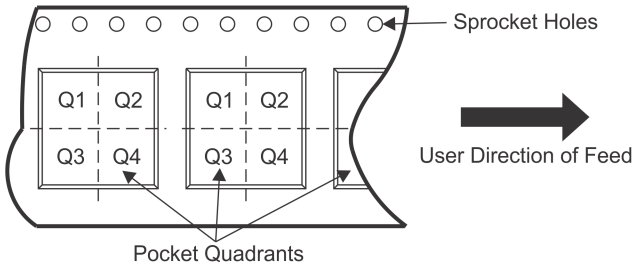


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

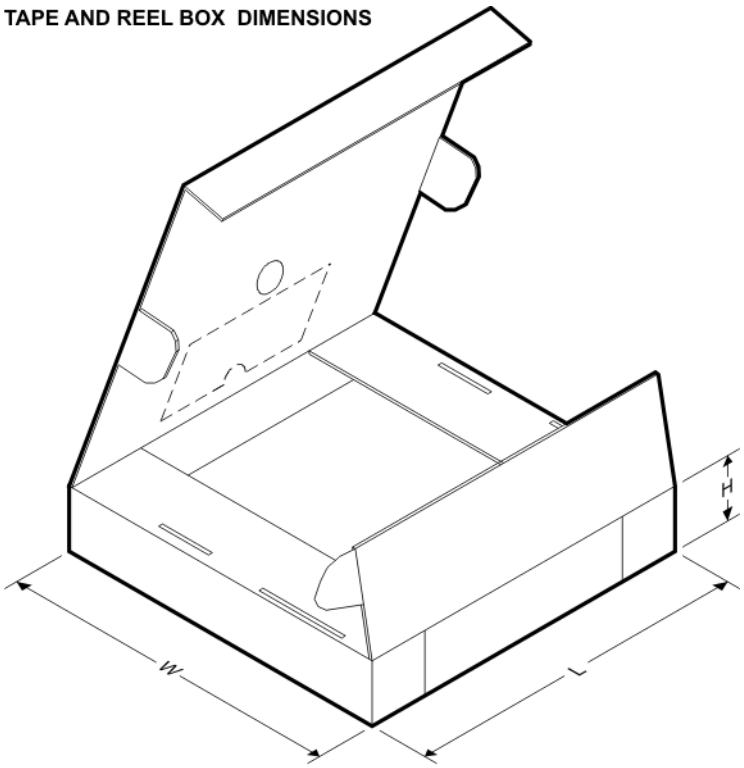
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49250RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1
LM49250RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.21	3.21	0.76	8.0	12.0	Q1

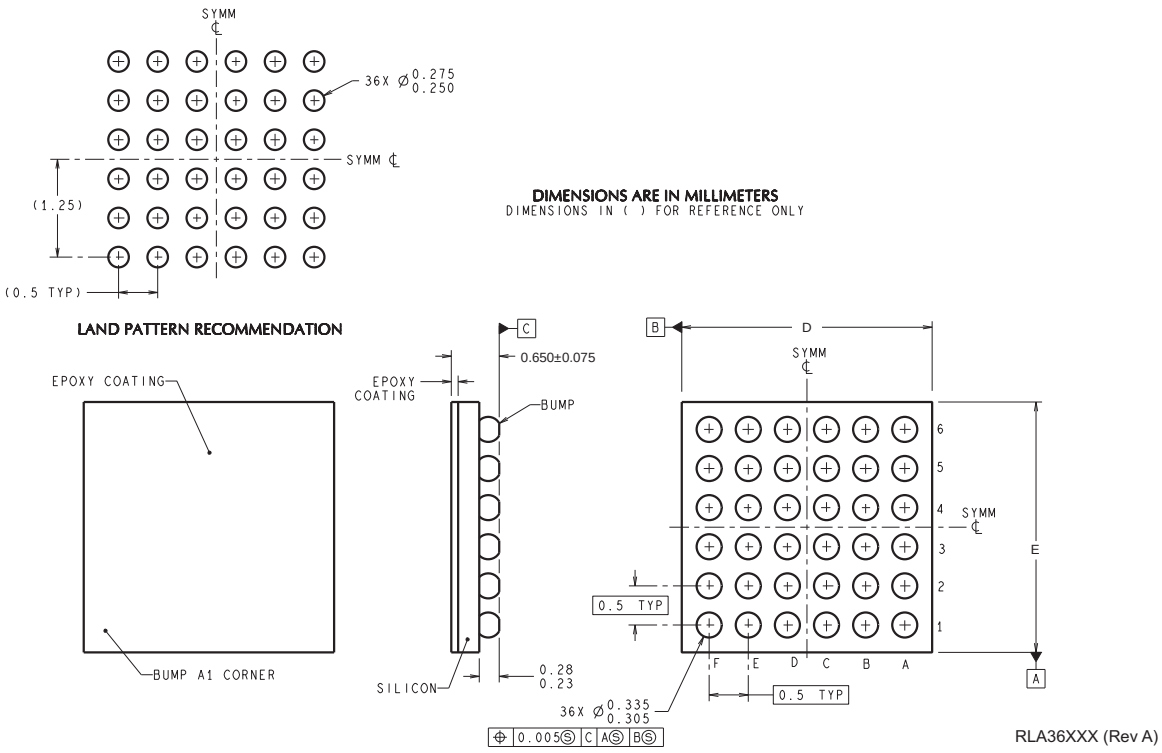
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49250RL/NOPB	DSBGA	YPG	36	250	210.0	185.0	35.0
LM49250RLX/NOPB	DSBGA	YPG	36	1000	210.0	185.0	35.0

YPG0036



D: Max = 3.071 mm, Min =3.011 mm

E: Max = 3.071 mm, Min =3.011 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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