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December 2013

### FQN1N60C

### N-Channel QFET® MOSFET

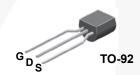
600 V, 0.30 A, 11.5 Ω

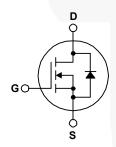
### **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

#### **Features**

- 0.30 A, 600 V,  $R_{DS(on)}$  = 11.5  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 0.15 A
- Low Gate Charge (Typ. 4.8 nC)
- Low Crss (Typ. 3.5 pF)
- · 100% Avalanche Tested





### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQN1N60CTA	Unit	
V <sub>DSS</sub>	Drain-Source Voltage		600	V	
I <sub>D</sub>	Drain Current - Co	ontinuous (T <sub>C</sub> = 25°C)		0.3	A
	- Co	ontinuous (T <sub>C</sub> = 100°C)		0.18	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)		(Note 1)	1.2	A
V <sub>GSS</sub>	Gate-Source Voltage			± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		(Note 2)	33	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	0.3	A
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	0.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C)			1	W
Power Dissipation (T <sub>L</sub> = 25°C)			3	W	
	- Derate above 25°C			0.02	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.		300	°C	

### **Thermal Characteristics**

Symbol	Parameter	FQN1N60CTA	Unit	
$R_{ heta JL}$	Thermal Resistance, Junction-to-Lead, Max.	(Note 5a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.		140	- 0/00

### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQN1N60CTA	1N60C	TO-92	AMMO	N/A	N/A	2000 units

### Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Parameter Test Conditions		Тур.	Max.	Unit
Off Characte	ristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	600			V
ΔBV <sub>DSS</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		0.6		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V			50	μΑ
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C			250	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	-		-100	nA
On Characte	ristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.15 A		9.3	11.5	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 0.3 \text{ A}$	\	0.75		S
Dynamic Ch	aracteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$	1	130	170	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz	1	19	25	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	3.5	6	pF
Switching C	haracteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 1.1 A,		7	24	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		21	52	ns
$t_{d(off)}$	Turn-Off Delay Time			13	36	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	- /	27	64	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 1.1 A,		4.8	6.2	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	-	0.7	/	nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)	ı	2.7		nC
Drain-Source	e Diode Characteristics and Maximum R	atings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				0.3	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				1.2	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.3 A			1.4	٧
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.1 A,		190		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_{F} / dt = 100 A/\mu s$		0.53		μC

- 1. Repetitive rating : pulse-width limited by maximum junction temperature.
- 2. L = 59 mH, I $_{AS}$  = 1.1 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C.
- $3.~I_{SD} \leq 0.3~A,~di/dt \leq 200~A/\mu s,~V_{DD} \leq BV_{DSS,}~starting~~T_J = 25^{\circ}C.$
- 4. Essentially independent of operating temperature.

5. a) Reference point of the R<sub>0,IL</sub> is the drain lead.
 b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment (R<sub>0,IA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance. R<sub>0CA</sub> is determined by the user's board design)

### **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

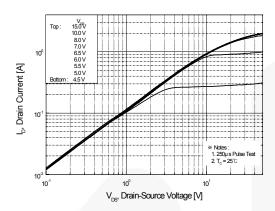


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

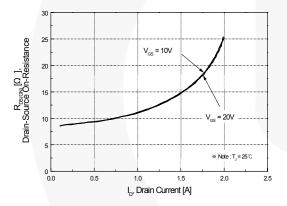


Figure 5. Capacitance Characteristics

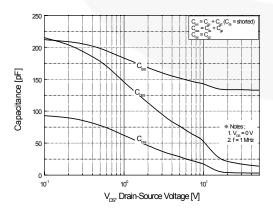


Figure 2. Transfer Characteristics

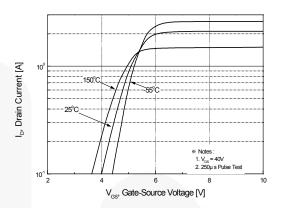


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

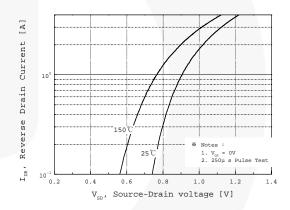
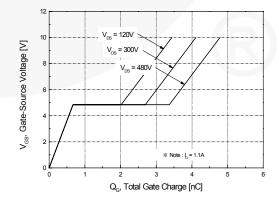


Figure 6. Gate Charge Characteristics



### **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

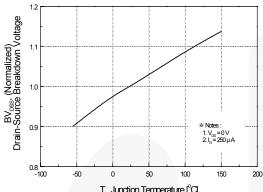


Figure 9. Maximum Safe Operating Area

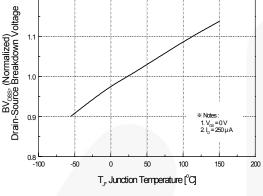


Figure 8. On-Resistance Variation vs. Temperature

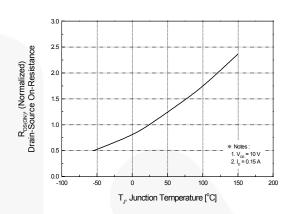
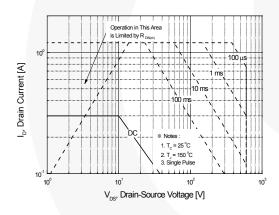


Figure 10. Maximum Drain Current vs. Case Temperature



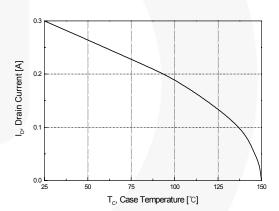
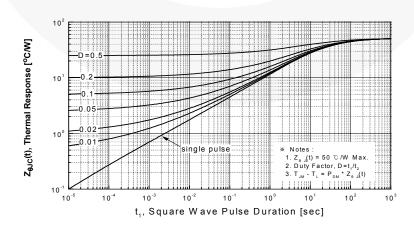


Figure 11. Transient Thermal Response Curve



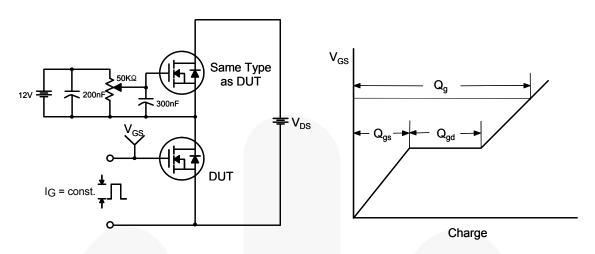


Figure 12. Gate Charge Test Circuit & Waveform

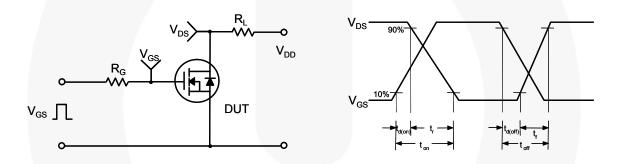


Figure 13. Resistive Switching Test Circuit & Waveforms

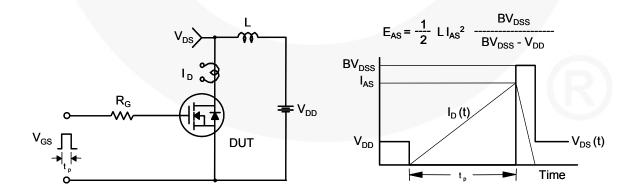


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

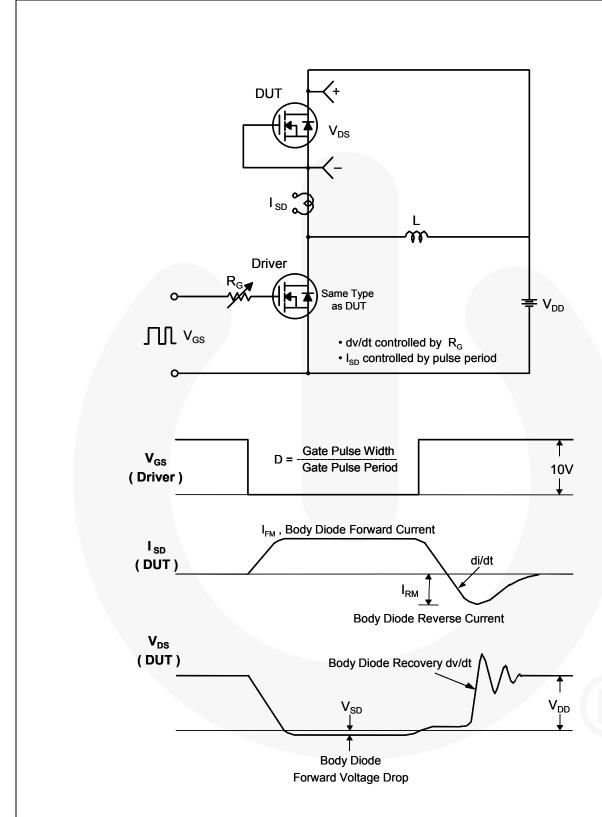


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

### **Mechanical Dimensions**

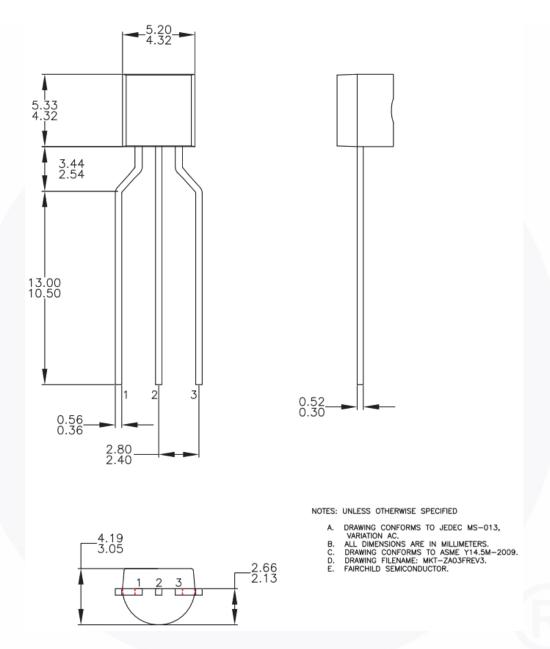


Figure 16. TO92, Molded, 3-Lead, 0.200 In Line Spacing LD Form (J61Z Option)

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