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# FCH041N60E

## N-Channel SuperFET® II Easy-Drive MOSFET

600 V, 77 A, 41 mΩ

### Features

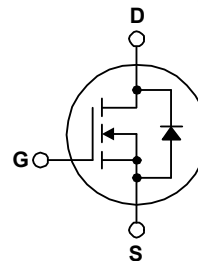
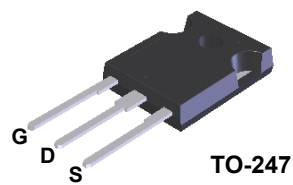
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 36\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 285\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 735\text{ pF}$ )
- 100% Avalanche Tested
- An Integrated Gate Resistor
- RoHS Compliant

### Applications

- LCD / LED / PDP TV Lighting
- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET II MOSFET easy-drive series offers slightly slower rise and fall times compared to the SuperFET II MOSFET series. Noted by the "E" part number suffix, this family helps manage EMI issues and allows for easier design implementation. For faster switching in applications where switching losses must be at an absolute minimum, please consider the SuperFET II MOSFET series.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCH041N60E	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC ( $f > 1\text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	77
		- Continuous ( $T_C = 100^\circ\text{C}$ )	48.7
$I_{DM}$	Drain Current	- Pulsed (Note 1)	231
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	2025
$I_{AR}$	Avalanche Current	(Note 1)	15
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	5.92
$dv/dt$	MOSFET $dv/dt$		100
	Peak Diode Recovery $dv/dt$	(Note 3)	20
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	592
		- Derate Above $25^\circ\text{C}$	4.74
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCH041N60E	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N60E	FCH041N60E	TO-247	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_C = 25^\circ\text{C}$	600	-	-	V
		$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_C = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.67	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	9.7	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 39\text{ A}$	-	36	41	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 39\text{ A}$	-	71	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	10300	13700	pF
$C_{oss}$	Output Capacitance		-	355	475	
$C_{rss}$	Reverse Transfer Capacitance		-	4	6	
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	187	-	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	735	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 39\text{ A}, V_{GS} = 10\text{ V}$	-	285	380	nC
$Q_{gs}$	Gate to Source Gate Charge	(Note 4)	-	45	-	
$Q_{gd}$	Gate to Drain "Miller" Charge		-	105	-	
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	1.2	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 39\text{ A}, V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$	-	50	110	ns
$t_r$	Turn-On Rise Time		-	50	110	
$t_{d(off)}$	Turn-Off Delay Time		-	320	650	
$t_f$	Turn-Off Fall Time	(Note 4)	-	85	180	ns

### Drain-Source Diode Characteristics

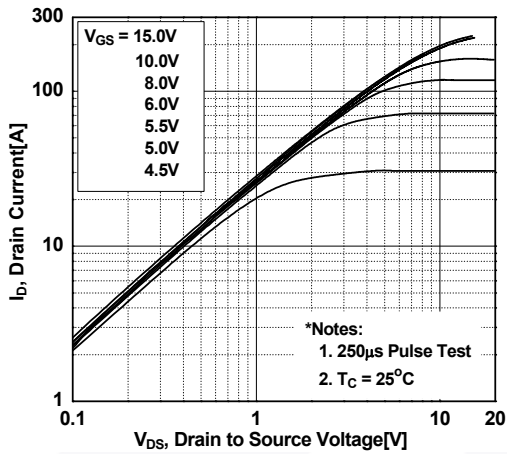
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	77	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	231	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 39\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 39\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	590	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	18	-	

#### Notes:

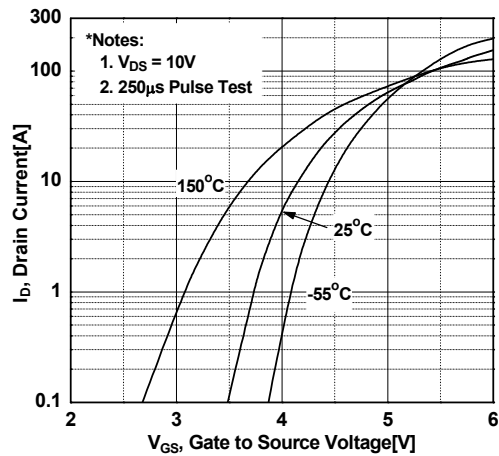
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 15\text{ A}, R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 39\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

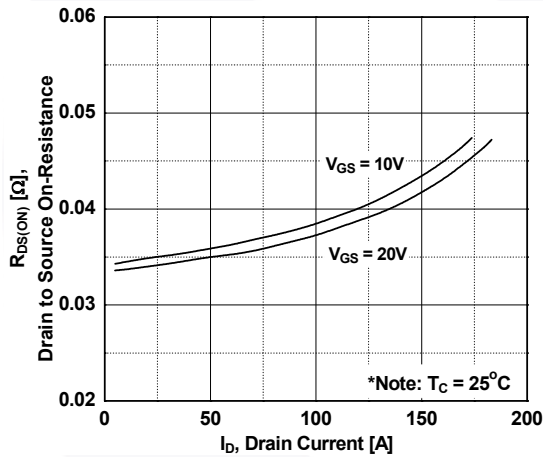
**Figure 1. On-Region Characteristics**



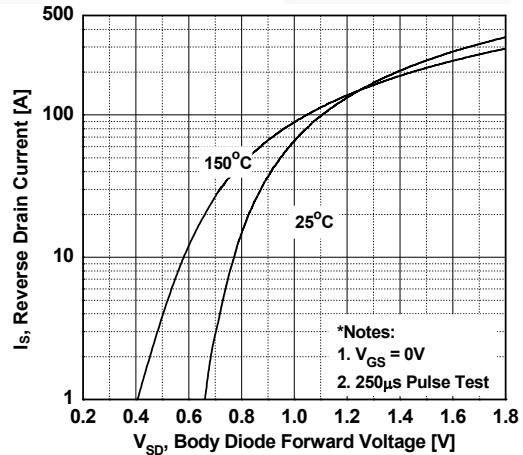
**Figure 2. Transfer Characteristics**



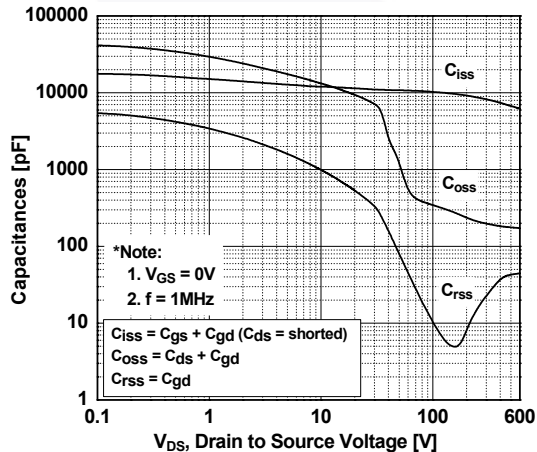
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



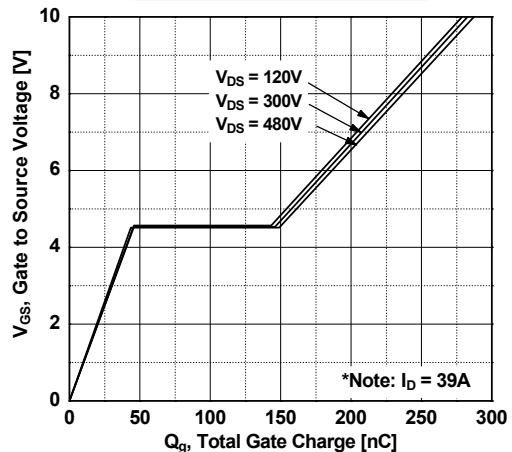
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

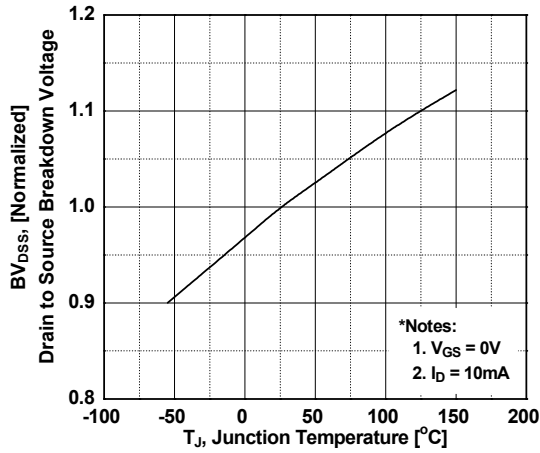


**Figure 6. Gate Charge Characteristics**

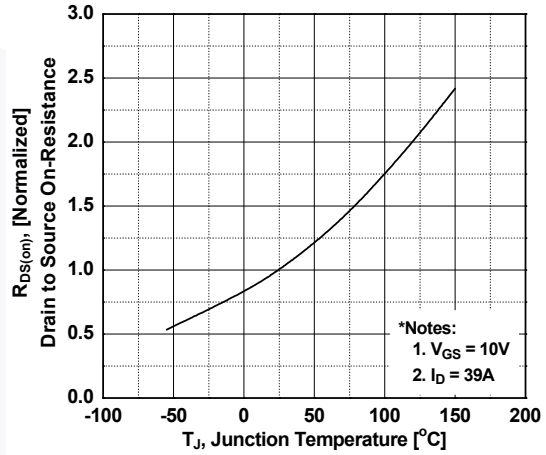


**Typical Characteristics** (Continued)

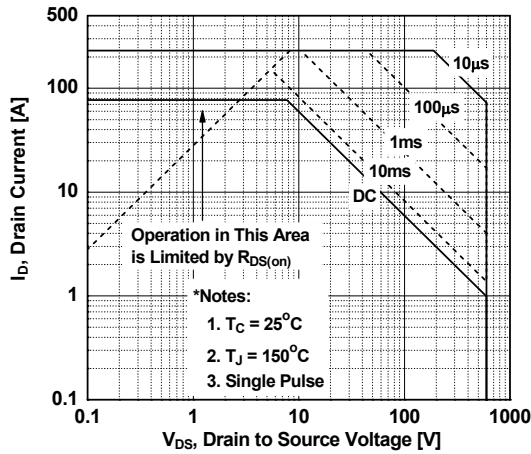
**Figure 7. Breakdown Voltage Variation vs. Temperature**



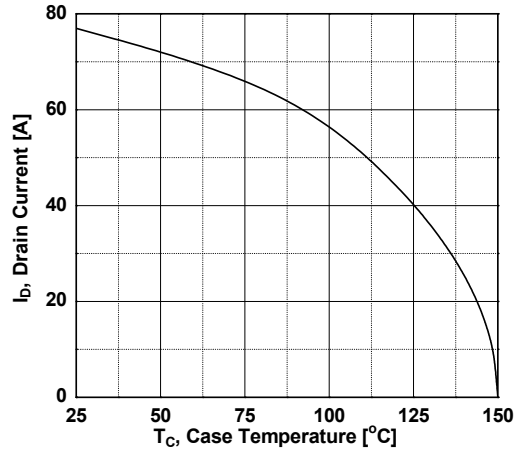
**Figure 8. On-Resistance Variation vs. Temperature**



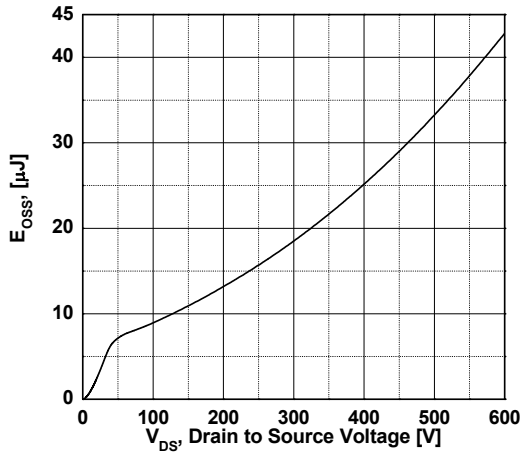
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

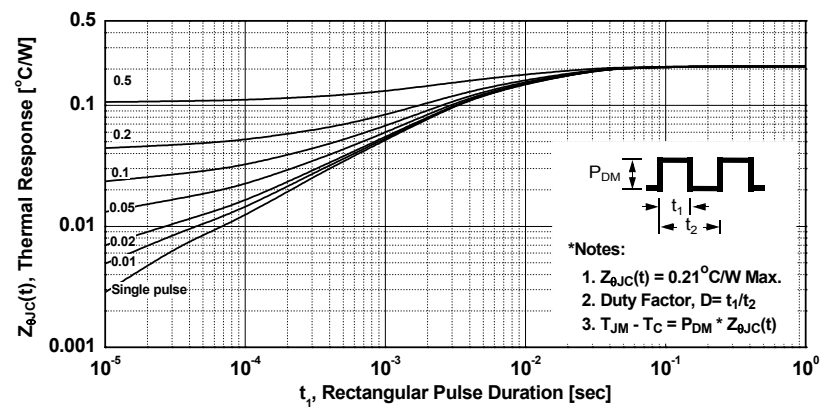


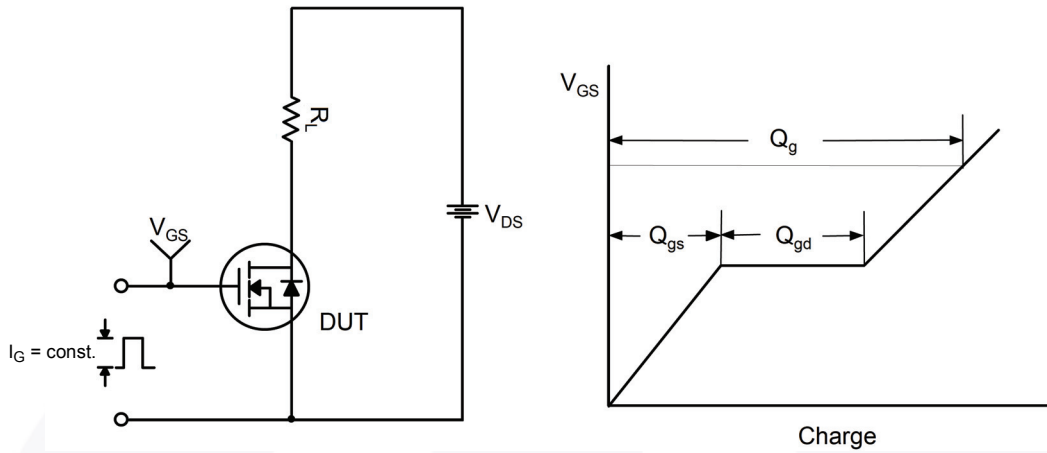
**Figure 11. Eoss vs. Drain to Source Voltage**



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve





**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**



**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**

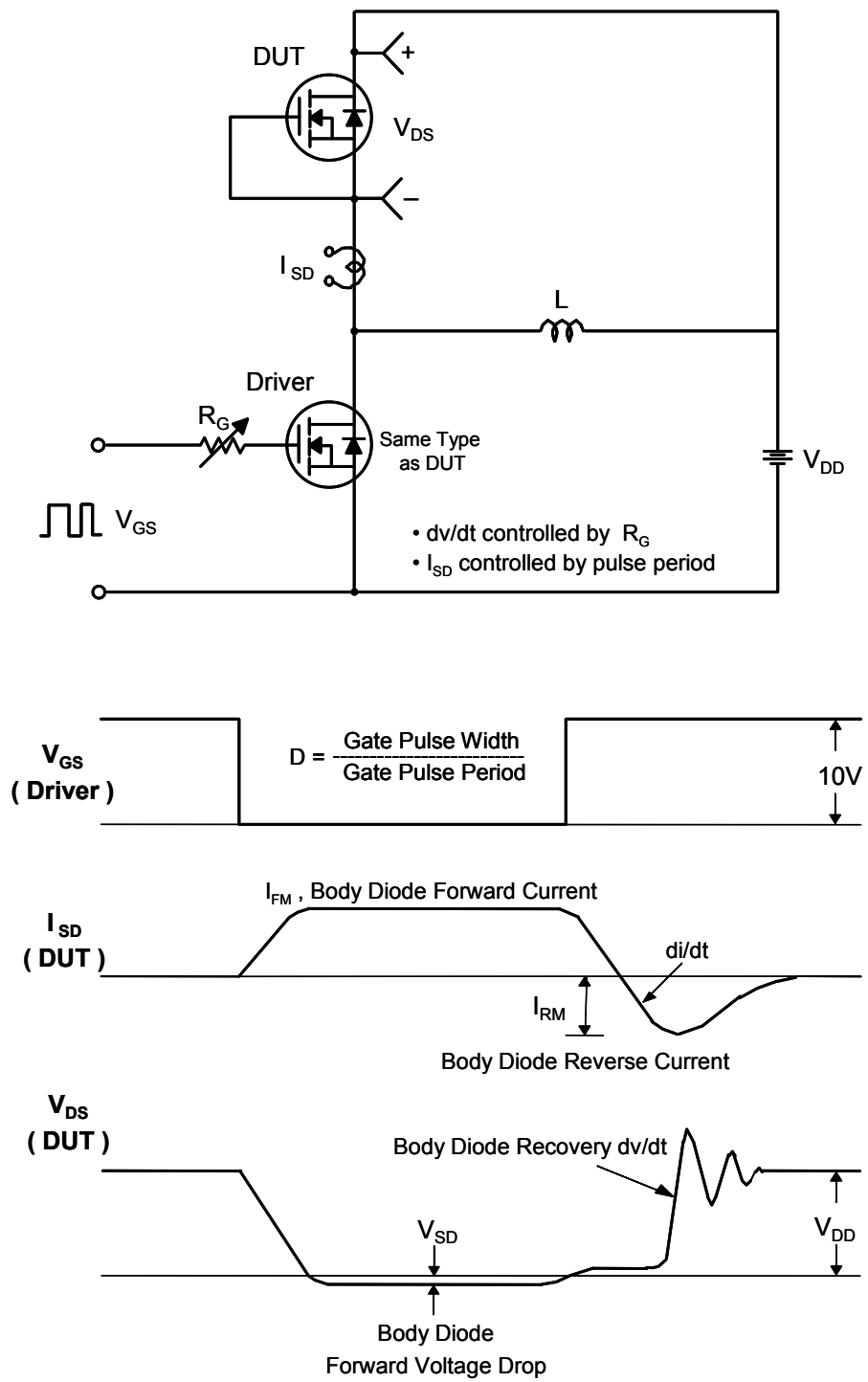
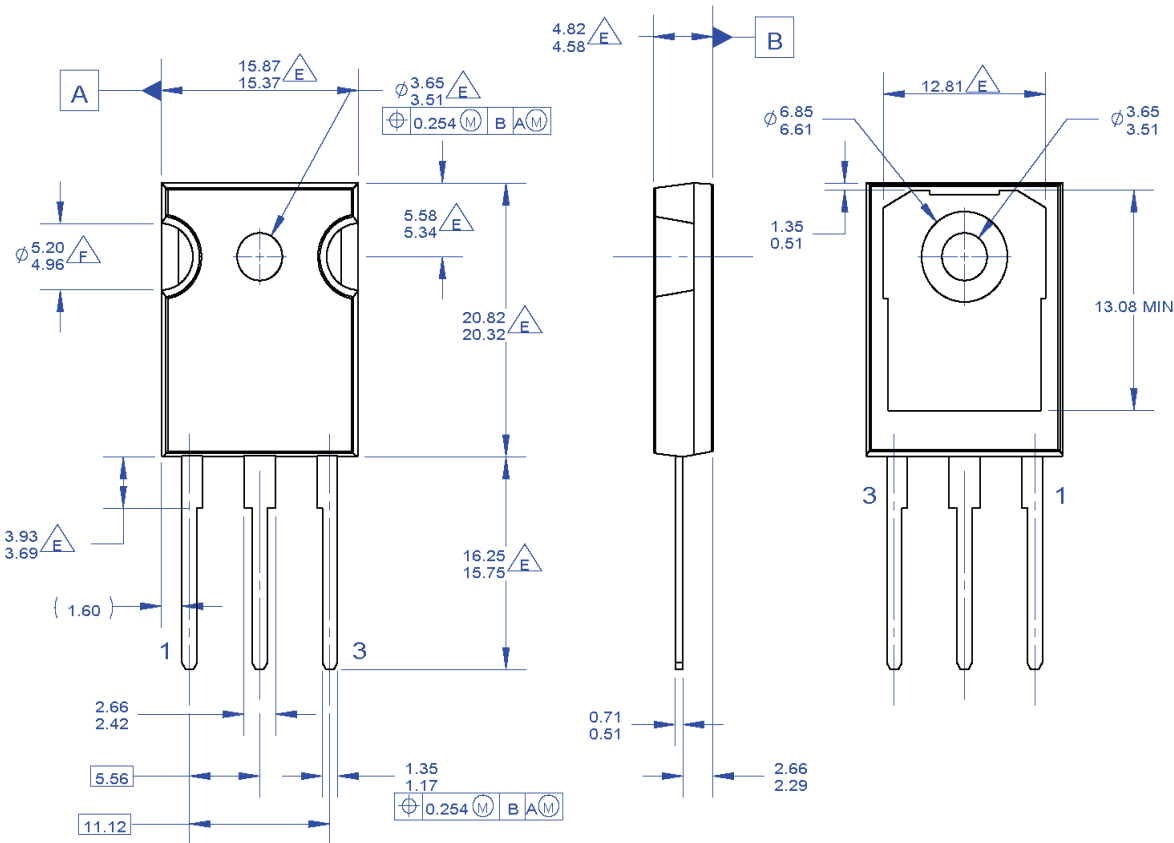


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



## Mechanical Dimensions



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- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

DOES NOT COMPLY JEDEC STANDARD VALUE

NOTCH MAY BE SQUARE

G. DRAWING FILENAME: MKT-TO247A03\_REV03

**Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB**

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