

## PCIe® Gen 2 Networking Clock Generator

### Features

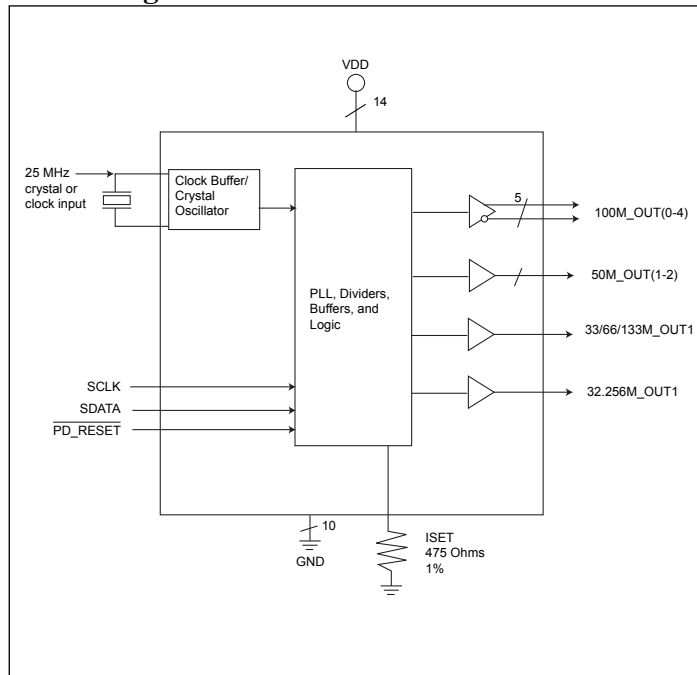
- 3.3V +/-10% Supply Voltage
- Uses 25MHz xtal
- Five PCIe® Gen. 2 100MHz HCSL outputs with optional -0.5% spread spectrum support
- Two LVCMOS 50MHz outputs that support +/- 10% frequency margining
- One frequency selectable 33/66/133MHz LVCMOS output
- One 32.256MHz LVCMOS output
- Industrial temperature -40°C to 85°C
- Package: 48-pin TSSOP package

### Description

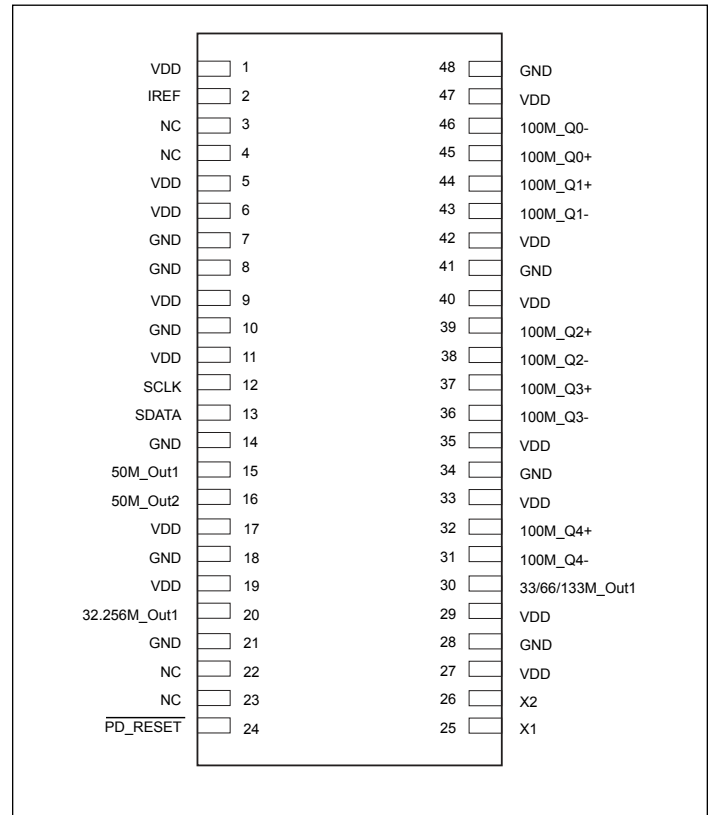
The PI6C49003A is a clock generator device intended for PCIe® Gen2 networking applications. The device includes five 100MHz differential Host Clock Signal Level (HCSL) outputs for PCIe Gen 2, two single-ended 50MHz outputs, one single-ended 32.256MHz output, and one selectable single-ended 33/66/133MHz output.

Using a serially programmable SMBUS interface, the PI6C49003A incorporates spread spectrum modulation on the twelve 100MHz HCSL PCIe Gen 2 outputs, and independent frequency margining on the 50MHz output, 33.333MHz and 66.6666MHz clock outputs.

### Block Diagram



### Pin Configuration



## Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	V <sub>DD</sub>	Power	3.3V Supply Pin
2	IREF	Output	Connect to 475-Ohm resistor to set HCSL output drive current
3	NC		No connect. Leave open
4	NC		No connect. Leave open
5	V <sub>DD</sub>	Power	3.3V Supply Pin
6	V <sub>DD</sub>	Power	3.3V Supply Pin
7	GND	Power	Ground
8	GND	Power	Ground
9	V <sub>DD</sub>	Power	3.3V Supply Pin
10	GND	Power	Ground
11	V <sub>DD</sub>	Power	3.3V Supply Pin
12	SCLK	Input	SMBus compatible input clock. Supports fast mode 400kHz input clock.
13	SDATA	I/O	SMBus compatible data line
14	GND	Power	Ground
15	50M_Out1	Output	50MHz LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
16	50M_Out2	Output	50MHz LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
17	V <sub>DD</sub>	Power	3.3V Supply Pin
18	GND	Power	Ground
19	V <sub>DD</sub>	Power	3.3V Supply Pin
20	32.256M_Out1	Output	32.256MHz LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
21	GND	Power	Ground
22	NC		
23	NC		
24	PD_RESET	Input	Power down reset - when low all PLL's are powered down and outputs trisated. SMBus registers are reset to default values.
25	X1	Input	Crystal input. Integrated 6pF capacitance
26	X2	Output	Crystal output. Integrated 6pF capacitance
27	V <sub>DD</sub>	Power	3.3V Supply Pin
28	GND	Power	Ground
29	V <sub>DD</sub>	Power	3.3V Supply Pin
30	33/66/133M_Out1	Output	33/66/133MHz selectable LVCMOS output. When disabled, output is trisated and has a nominal 110k-Ohm pull-down.
31	100M_Q4-	Output	100MHz HCSL output
32	100M_Q4+	Output	100MHz HCSL output

**Pin Description (Cont..)**

Pin #	Pin Name	Pin Type	Pin Description
33	V <sub>DD</sub>	Power	3.3V Supply Pin
34	GND	Power	Ground
35	V <sub>DD</sub>	Power	3.3V Supply Pin
36	100M_Q3-	Output	100MHz HCSL output
37	100M_Q3+	Output	100MHz HCSL output
38	100M_Q2-	Output	100MHz HCSL output
39	100M_Q2+	Output	100MHz HCSL output
40	V <sub>DD</sub>	Power	3.3V Supply Pin
41	GND	Power	Ground
42	V <sub>DD</sub>	Power	3.3V Supply Pin
43	100M_Q1-	Output	100MHz HCSL output
44	100M_Q1+	Output	100MHz HCSL output
45	100M_Q0+	Output	100MHz HCSL output
46	100M_Q0-	Output	100MHz HCSL output
47	V <sub>DD</sub>	Power	3.3V Supply Pin
48	GND	Power	Ground

**50MHz Frequency Margining Table**

FS3	FS2	FS1	FS0	50M_OUT1, 50M_OUT2
0	0	0	0	nominal
0	0	0	1	nominal + 1%
0	0	1	0	nominal + 2%
0	0	1	1	nominal + 3%
0	1	0	0	nominal + 4%
0	1	0	1	nominal + 5%
0	1	1	0	nominal + 6%
0	1	1	1	nominal + 8%
1	0	0	0	nominal + 10%
1	0	0	1	nominal - 1%
1	0	1	0	nominal - 2%
1	0	1	1	nominal - 3%
1	1	0	0	nominal - 4%
1	1	0	1	nominal - 6%
1	1	1	0	nominal - 8%
1	1	1	1	nominal - 10%

**33/66/133MHz Frequency Margining Table**

FS6	FS5	FS4	33M/66M/133M_OUT1
0	0	0	33.3333MHz
0	0	1	66.6666MHz +2%
0	1	0	66.6666MHz +1%
0	1	1	66.6666MHz +0%
1	0	0	66.6666MHz -2%
1	0	1	66.6666MHz -4%
1	1	0	66.6666MHz -6%
1	1	1	133.3333MHz

## Serial Data Interface (SMBus)

PI6C49003A is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

### Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	0	0	1	0/1

### How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	D2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	...	Data Byte N - 1	Ack	Stop bit

#### Note:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

### How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	...	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting databyte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	...	S: sends data byte N+X-1	M: Not Acknowledge	M: Stop bit

## Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Spectrum Selection for 100MHz HCSL PCI-Express clocks	RW	0	All 100MHz HCSL PCI Express outputs	0=spread off 1 = -0.5% down spread
6	Enables hardware or software control of OE bits (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{\text{PD\_RESET}}$ pin, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{\text{PD\_RESET}}$ bit. Enables or disables all outputs (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4	Frequency margining select bit FS3	RW	1	50M_Out1 and 50M_Out2	See 50MHz Frequency Margining Table on Page 3
3	Frequency margining select bit FS2	RW	0		
2	Frequency margining select bit FS1	RW	1		
1	Frequency margining select bit FS0	RW	0		
0	OE for single-ended 50MHz output 50M_Out2	RW	1	Single-ended 50MHz output 50M_Out2	0 = disabled 1 = enabled

**Byte 0 - Bit 6 and Bit 5 Functionality**

Bit 6	Bit 5	Description
0	X	( $\overline{\text{PD\_RESET}}$ = "H" will enable all outputs; SMBus cannot control each output.)
1	0	Disables all outputs and tri-states the outputs, $\overline{\text{PD\_RESET}}$ HW pin/signal = DO NOT CARE
1	1	Enable outputs according to the SMBus default values; SMBus can control each output. $\overline{\text{PD\_RESET}}$ HW pin/signal = DON'T CARE

**Byte 1: Control Register**

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 32.256M_Out1	RW	1	32.256M_Out1	0 = disabled 1 = enabled
6	OE for 50M_Out1	RW	1	50M_Out1	0 = disabled 1 = enabled
5	OE for 33/66/133M_Out1	RW	1	33/66/133M_Out1	0 = disabled 1 = enabled
4	OE for 100M_Q11 HCSL output	RW	1	100M_Q11	0 = disabled 1 = enabled
3	OE for 100M_Q10 HCSL output	RW	0	100M_Q10	0 = disabled 1 = enabled
2	OE for 100M_Q09 HCSL output	RW	0	100M_Q9	0 = disabled 1 = enabled
1	OE for 100M_Q08 HCSL output	RW	0	100M_Q8	0 = disabled 1 = enabled
0	OE for 100M_Q07 HCSL output	RW	0	100M_Q7	0 = disabled 1 = enabled

**Byte 2: Control Register**

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Frequency margining select bit FS6	RW	1	33/66/133M_Out1	See 33/66/133MHz Frequency Margining Table on Page 3
6	Frequency margining select bit FS5	RW	0		
5	Frequency margining select bit FS4	RW	0		
4 to 0	Reserved	R	Undefined	Not Applicable	

### Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 100M_Q6 HCSL Output	RW	0	100M_Q6	0 = disabled 1 = enabled
6	OE for 100M_Q5 HCSL Output	RW	0	100M_Q5	0 = disabled 1 = enabled
5	OE for 100M_Q4 HCSL Output	RW	0	100M_Q4	0 = disabled 1 = enabled
4	OE for 100M_Q3 HCSL Output	RW	0	100M_Q3	0 = disabled 1 = enabled
3	OE for 100M_Q2 HCSL Output	RW	0	100M_Q2	0 = disabled 1 = enabled
2	OE for 100M_Q1 HCSL Output	RW	1	100M_Q1	0 = disabled 1 = enabled
1	OE for 100M_Q0 HCSL Output	RW	1	100M_Q0	0 = disabled 1 = enabled
0	Reserved	R	Undefined	Not Applicable	

### Byte 4 & 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

### Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	0	Not Applicable	
6	Revision ID bit 2	R	0	Not Applicable	
5	Revision ID bit 1	R	0	Not Applicable	
4	Revision ID bit 0	R	0	Not Applicable	
3	Vendor ID bit 3	R	0	Not Applicable	
2	Vendor ID bit 2	R	0	Not Applicable	
1	Vendor ID bit 1	R	1	Not Applicable	
0	Vendor ID bit 0	R	1	Not Applicable	

**Absolute Maximum Ratings<sup>1</sup>** (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V <sub>DD</sub>	3.3V I/O Supply Voltage	-0.5	4.6	V
V <sub>IH</sub>	Input High Voltage		4.6	
V <sub>IL</sub>	Input Low Voltage	-0.5		
T <sub>s</sub>	Storage Temperature	-65	150	°C
V <sub>ESD</sub>	ESD Protection	2000		V

**Note:**

1. Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

**Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, V <sub>DD</sub> .....	7V
All Inputs and Outputs .....	-0.5V to V <sub>DD</sub> +0.5V
Ambient Operating Temperature .....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Junction Temperature .....	125°C
Peak Soldering Temperature .....	260°C

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics**

Unless otherwise specified, V<sub>DD</sub>=3.3V±10%, Ambient Temperature -40°C to +85°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>DD</sub>	Operating Supply Voltage		3.0		3.6	V
V <sub>IH</sub>	Input High Voltage		2		V <sub>DD</sub>	
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	
V <sub>IH</sub>	Input High Voltage	SDATA, SCLK	0.7V <sub>DD</sub>		V <sub>DD</sub>	
V <sub>IL</sub>	Input Low Voltage	SDATA, SCLK			0.3V <sub>DD</sub>	
I <sub>DD</sub>	Operating Supply Current			320		mA
	IDD at Output Disable Condition	$\overline{\text{PD\_RESET}} = 0$		3.0		
R <sub>PU</sub> /R <sub>PD</sub>	Internal Pull-Up/Pull-Down Resistor	$\overline{\text{PD\_RESET}}$		216		k-Ohm
		All single-ended outputs			75	
C <sub>IN</sub>	Input Capacitance	All input pins		6		pF

**Electrical Characteristics - Single-Ended**

 Unless otherwise specified,  $V_{DD}=3.3V\pm 10\%$ , Ambient Temperature  $-40^{\circ}C$  to  $+85^{\circ}C$ 

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$F_{IN}$	Input Clock Frequency			25		MHz
	SCLK Frequency			100	400	kHz
	Minimum Pulse Width of $\overline{PD\_RESET}$ Input		100			ns
	Output Frequency Error	$FS_0, FS_6 = 0$		0		ppm
	Output Frequency Error	32.256MHz			7	
$t_r, t_f$	Output Rise/Fall Time	$V_{DD}=3.3V, 0.8V$ to $2.4V$		0.5	1	ns
	Output Clock Duty Cycle	Measured at $V_{DD}/2$	45	50	55	%
$V_{OH}$	High-Level Output Voltage	$I_{OH} = -4mA$	$V_{DD}-0.4$			V
$V_{OH}$	High-Level Output Voltage	$I_{OH} = -8mA$	2.4			
$V_{OL}$	Low-Level Output Voltage	$I_{OL} = 8mA$			0.4	
	Peak-to-Peak Jitter	50MHz clock output		140	200	ps
		33/66/133MHz clock output		125	175	
		32.256MHz clock output		115	150	
	Cycle-to-Cycle Jitter	50MHz clock output		120	175	
		33/66/133 MHz clock output		120	160	
	Clock Stabilization Time from Power Up		3		10	

## Electrical Characteristics - 100MHz Differential HCSL Outputs

Unless otherwise specified,  $V_{DD}=3.3V\pm 10\%$ , Ambient Temperature  $-40^{\circ}C$  to  $+85^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Output Frequency				100	MHz
$T_{CC/Jitter}$	Cycle-to-Cycle Jitter				150	ps
	Peak-to-Peak Phase Jitter	Using PCIe jitter measurement method			86	
$J_{RMS2.0}$	PCIe 2.0 RMS Phase Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
	Spread Modulation Percentage			-0.5	0	%
	Spread Modulation Frequency			32		kHz
$T_{DC}$	Duty Cycle		45	50	55	%
	Rising/Falling Edge Rate	Note 3, 4	0.6		4.5	V/ns
$T_{OSKEW}$	Output Skew	$V_T = 50\%$ (measurement threshold)			200	ps
$Z_{C-DC}$	Clock Source DC Impedance, single ended			50		Ohm
$V_{OH}$	High-Level Output Voltage	Note 2, ( $R_S=33\text{-Ohm}$ , $R_T=50\text{-Ohm}$ )	0.65	0.71	0.95	V
$V_{OL}$	Low-Level Output Voltage		-0.20	0	0.05	
$I_{OH}$	$I_{OH} @ 6 \cdot I_{REF}$		-13	-14.2	-18.5	mA
$V_{CROSS}$	Absolute Crossing Point Voltage	Note 2, 5, 6	0.25		0.55	V
$V_{CROSS\ Delta}$	Variation of $V_{CROSS}$ over all rising clock edges	Note 2, 5, 8			140	mV
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	Note 3, 9, 10	-300		2800	ppm
$T_{PERIOD\ ABS}$	Absolute Period (including jitter and spread spectrum)	Note 3, 7	9.847		10.203	ns

### Notes:

1. Measured at the end of an 8-inch trace with a 5pF load.
2. Measurement taken from a single-ended waveform.
3. Measurement taken from a differential waveform.
4. Measured from -150 mV to +150 mV on the differential waveform. The signal is monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
5. Measured at crossing point where the instantaneous voltage value of the rising edge of 100M+ equals the falling edge 100M-.
6. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
7. Defines as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
8. Defined as the total variation of all crossing voltages of rising 100M+ and falling 100M-.
9. Refer to section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.
10. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 PPM there is an error budget of  $100\text{Hz}/\text{PPM} * 300\text{ PPM} = 30\text{ kHz}$ . The period is measured with a frequency counter with measurement window set at 100 ms or greater. With spread spectrum turned off the error is less than  $\pm 300\text{ ppm}$ . With spread spectrum turned on there is an additional +2500 PPM nominal shift in maximum period resulting from the -0.5% down spread.

**Crystal Load Capacitors**

If an input crystal is used, crystal should be connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

$C_L$  = Crystal's load capacitance in pF

Crystal Capacitors (pF) =  $(C_L - 8) * 2$

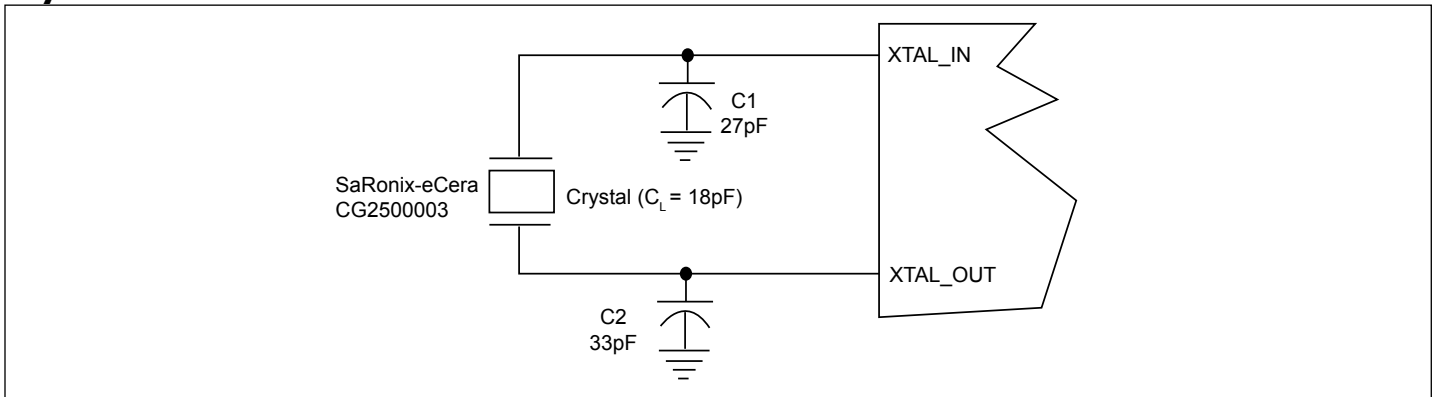
For example, for a crystal with a 18pF load cap, each external crystal cap would be 18pF.  $(18 - 8) * 2 = 18$ .

**Application Notes**

**Crystal circuit connection**

The following diagram shows PI6LC4830-01 crystal circuit connection with a parallel crystal. For the  $C_L=18pF$  crystal, it is suggested to use  $C1= 27pF$ ,  $C2= 33pF$ .  $C1$  and  $C2$  can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

**Crystal Oscillator Circuit**

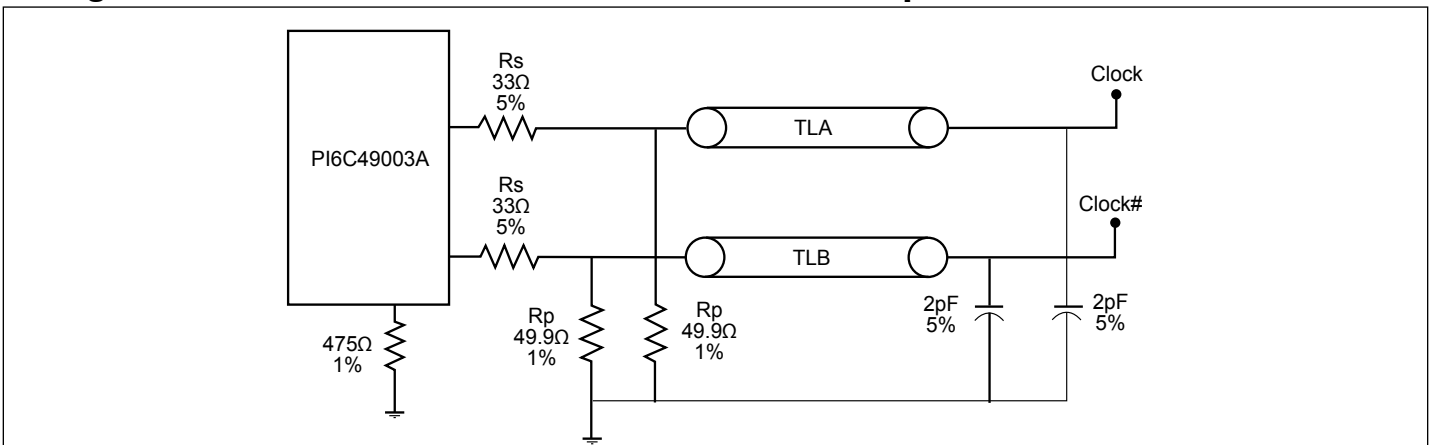


**Recommended Crystal Specification**

Pericom recommends:

- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M,  $C_L=18pF$ , +/-30ppm, [http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500081, SMD 5x3.2(4P), 25M,  $C_L=18pF$ , +/-30ppm, [http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M,  $C_L=18pF$ , +/-20ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>

**Configuration test load board termination for HCSL Outputs**



**Figure 4. Configuration Test Load Board Termination**

**Packaging Mechanical: 48-Contact TSSOP(A)**

<p>The drawing shows three views of the 48-pin TSSOP(A) package. The top view shows a rectangular package with 48 pins on both long sides. Dimensions include a total length of .488 inches (12.4 mm) and .496 inches (12.6 mm), and a width of .236 inches (6.0 mm) and .244 inches (6.2 mm). The side view shows a height of .047 inches (1.20 mm) maximum and a .002 inch (.05 mm) gap from the seating plane. The detail view shows a .018 inch (.30 mm) lead width and a .319 inch (8.1 mm) BSC lead spacing. A note indicates that 'X.XX' denotes dimensions in millimeters.</p>	<p><b>DOCUMENT CONTROL NO.</b> PD - 1501</p> <hr/> <p><b>REVISION: G</b> <b>DATE: 03/09/05</b></p>
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<p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. Controlling dimensions in millimeters.</li> <li>2. Ref: JEDEC MO-153F/ED</li> <li>3. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm per side.</li> <li>4. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.</li> </ol>	<p><b>Pericom Semiconductor Corporation</b> 3545 N. 1st Street, San Jose, CA 95134 1-800-435-2335 • www.pericom.com</p> <hr/> <p><b>DESCRIPTION: 48-Pin 240-Mil Wide TSSOP</b></p> <hr/> <p><b>PACKAGE CODE: A</b></p>
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**Note:** For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information<sup>(1-3)</sup>**

Ordering Code	Package Code	Package Description
PI6C49003AAE	A	48-pin, 240-Mil Wide (TSSOP)

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

# Mouser Electronics

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