250μA, 3MHz, 200V/μs Operational Amplifier

FEATURES

- **3MHz Gain Bandwidth**
- **200V/μs Slew Rate**
- **250μA Supply Current**
- **Available in Tiny MSOP Package**
- C-Load™ Op Amp Drives All Capacitive Loads
- Unity-Gain Stable
- Power Saving Shutdown Feature
- Maximum Input Offset Voltage: 600μV
- Maximum Input Bias Current: 50nA
- Maximum Input Offset Current: 15nA
- Minimum DC Gain, R_L = 2k: 30V/mV
- Input Noise Voltage: 14nV/√Hz
- Settling Time to 0.1%, 10V Step: 700ns
- Settling Time to 0.01%, 10V Step: 1.25μs
- Minimum Output Swing into 1k: ±13V
- Minimum Output Swing into 500Ω: ±3.4V
- Specified at ±2.5V, ±5V and ±15V

APPLICATIONS

- Battery-Powered Systems
- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

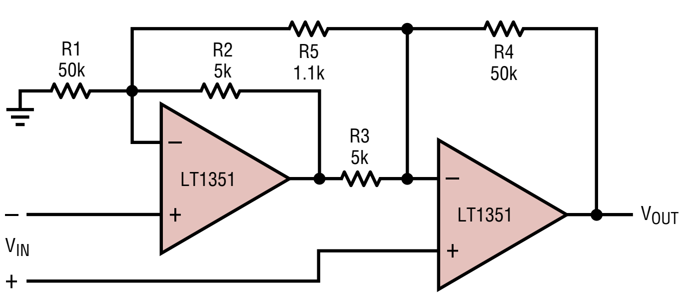
DESCRIPTION

The LT®1351 is a low power, high speed, high slew rate operational amplifier with outstanding AC and DC performance. The LT1351 features lower supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit combines the slewing performance of a current feedback amplifier in a true operational amplifier with matched high impedance inputs. The high slew rate ensures that the large-signal bandwidth is not degraded. The amplifier is a single gain stage with outstanding settling characteristics which make the circuit an ideal choice for data acquisition systems. The output drives a 1kΩ load to ±13V with ±15V supplies and a 500Ω load to ±3.4V on ±5V supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

The LT1351 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced complementary bipolar processing. For dual and quad amplifier versions of the LT1351 see the LT1352/LT1353 data sheet. For higher bandwidth devices with higher supply current see the LT1354 through LT1365 data sheets. Singles, duals and quads of each amplifier are available.

TYPICAL APPLICATION

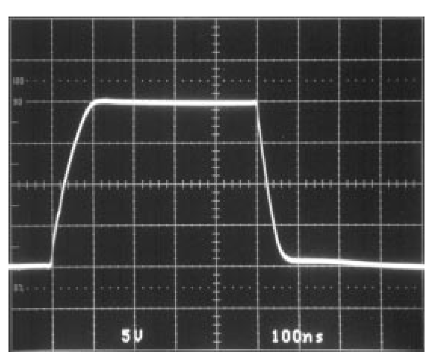
Instrumentation Amplifier



GAIN = [R4/R3][1 + (1/2)(R2/R1 + R3/R4) + (R2 + R3)/R5] = 102
TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 30kHz

1351 TA01

Large-Signal Response



$A_V = -1$

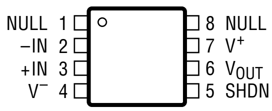
1351 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage (Transient Only, Note 1) ... ±10V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 2) .... Indefinite
Operating Temperature Range .... –40°C to 85°C
Specified Temperature Range (Note 6) ..... –40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

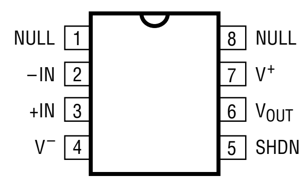


MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LT1351CMS8
MS8 PART MARKING
LTBT

TOP VIEW



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)

ORDER PART NUMBER
LT1351CN8 LT1351CS8
S8 PART MARKING
1351

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V		0.2	0.6	mV
			±5V		0.2	0.6	mV
			±2.5V		0.3	0.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		5	15	nA
I_B	Input Bias Current		±2.5V to ±15V		20	50	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		14		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.5		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	300	600		MΩ
		Differential	±15V		20		MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Positive Input Voltage Range		±15V	12.0	13.5		V
			±5V	2.5	3.5		V
			±2.5V	0.5	1.0		V
	Negative Input Voltage Range		±15V		–13.5	–12.0	V
			±5V		–3.5	–2.5	V
			±2.5V		–1.0	–0.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	±15V	80	94		dB
		V_{CM} = ±2.5V	±5V	78	86		dB
		V_{CM} = ±0.5V	±2.5V	68	77		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		90	106		dB

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 5k$	±15V	40	80		V/mV
		$V_{OUT} = \pm10V$, $R_L = 2k$	±15V	30	60		V/mV
		$V_{OUT} = \pm10V$, $R_L = 1k$	±15V	20	40		V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 5k$	±5V	30	60		V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 2k$	±5V	25	50		V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	15	30		V/mV
		$V_{OUT} = \pm1V$, $R_L = 5k$	±2.5V	20	40		V/mV
V_{OUT}	Output Swing	$R_L = 5k$, $V_{IN} = \pm10mV$	±15V	13.5	14.0		±V
		$R_L = 2k$, $V_{IN} = \pm10mV$	±15V	13.4	13.8		±V
		$R_L = 1k$, $V_{IN} = \pm10mV$	±15V	13.0	13.4		±V
		$R_L = 1k$, $V_{IN} = \pm10mV$	±5V	3.5	4.0		±V
		$R_L = 500\Omega$, $V_{IN} = \pm10mV$	±5V	3.4	3.8		±V
		$R_L = 5k$, $V_{IN} = \pm10mV$	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	$V_{OUT} = \pm13V$	±15V	13.0	13.4		mA
		$V_{OUT} = \pm3.4V$	±5V	6.8	7.6		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	30	45		mA
SR	Slew Rate	$A_V = -1$, $R_L = 5k$ (Note 3)	±15V	120	200		V/µs
			±5V	30	50		V/µs
	Full-Power Bandwidth	10V Peak (Note 4)	±15V		3.2		MHz
		3V Peak (Note 4)	±5V		2.6		MHz
GBW	Gain Bandwidth	$f = 200kHz$, $R_L = 10k$	±15V	2.0	3.0		MHz
			±5V	1.8	2.7		MHz
			±2.5V		2.5		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V	±15V		46		ns
			±5V		53		ns
	Overshoot	$A_V = 1$, 0.1V	±15V		13		%
			±5V		16		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		41		ns
			±5V		52		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	±15V		700		ns
		10V Step, 0.01%, $A_V = -1$	±15V		1250		ns
		5V Step, 0.1%, $A_V = -1$	±5V		950		ns
		5V Step, 0.01%, $A_V = -1$	±5V		1400		ns
R_O	Output Resistance	$A_V = 1$, $f = 20kHz$	±15V		1.5		Ω
I_{SHDN}	Shutdown Input Current	SHDN = V_{EE} + 0.1V	±15V		–10		µA
		SHDN = V_{CC}	±15V		0.1	2	µA
I_S	Supply Current		±15V		250	330	µA
			±5V		220	300	µA
		SHDN = V_{EE} + 0.1V	±5V		10		µA

$0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V			0.8	mV
			±5V			0.8	mV
			±2.5V			1.0	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V		3	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V			20	nA
I_B	Input Bias Current		±2.5V to ±15V			75	nA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	78			dB
		$V_{CM} = \pm2.5V$	±5V	77			dB
		$V_{CM} = \pm0.5V$	±2.5V	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to $\pm15V$		89			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 5k$	±15V	25			V/mV
		$V_{OUT} = \pm10V$, $R_L = 2k$	±15V	20			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 5k$	±5V	20			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 2k$	±5V	15			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	10			V/mV
		$V_{OUT} = \pm1V$, $R_L = 5k$	±2.5V	15			V/mV
V_{OUT}	Output Swing	$R_L = 5k$, $V_{IN} = \pm10mV$	±15V	13.4			±V
		$R_L = 2k$, $V_{IN} = \pm10mV$	±15V	13.3			±V
		$R_L = 1k$, $V_{IN} = \pm10mV$	±15V	12.0			±V
		$R_L = 1k$, $V_{IN} = \pm10mV$	±5V	3.4			±V
		$R_L = 500\Omega$, $V_{IN} = \pm10mV$	±5V	3.3			±V
		$R_L = 5k$, $V_{IN} = \pm10mV$	±2.5V	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	±15V	12.0			mA
		$V_{OUT} = \pm3.3V$	±5V	6.6			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	24			mA
SR	Slew Rate	$A_V = -1$, $R_L = 5k$ (Note 3)	±15V	100			V/µs
			±5V	21			V/µs
GBW	Gain Bandwidth	f = 200kHz, $R_L = 10k$	±15V	1.8			MHz
			± 5V	1.6			MHz
I_{SHDN}	Shutdown Input Current	SHDN = V_{EE} + 0.1V	±15V		– 20		µA
		SHDN = V_{CC}	±15V			3	µA
I_S	Supply Current		±15V			380	µA
			±5V			355	µA
		SHDN = V_{EE} + 0.1V	±5V		20		µA

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted (Note 6).

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V			1.0	mV
			±5V			1.0	mV
			±2.5V			1.2	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V		3	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V			30	nA
I_B	Input Bias Current		±2.5V to ±15V			100	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	76			dB
		$V_{CM} = \pm2.5V$	±5V	76			dB
		$V_{CM} = \pm0.5V$	±2.5V	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to $\pm15V$		87			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 5k$	±15V	20			V/mV
		$V_{OUT} = \pm10V$, $R_L = 2k$	±15V	15			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 5k$	±5V	15			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 2k$	±5V	10			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	8			V/mV
		$V_{OUT} = \pm1V$, $R_L = 5k$	±2.5V	10			V/mV

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, V_{CM} = 0V unless otherwise noted (Note 6).

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	R_L = 5k, V_{IN} = ±10mV	±15V	13.3			±V
		R_L = 2k, V_{IN} = ±10mV	±15V	13.2			±V
		R_L = 1k, V_{IN} = ±10mV	±15V	10.0			±V
		R_L = 1k, V_{IN} = ±10mV	±5V	3.3			±V
		R_L = 500Ω, V_{IN} = ±10mV	±5V	3.2			±V
		R_L = 5k, V_{IN} = ±10mV	±2.5V	1.1			±V
I_{OUT}	Output Current	V_{OUT} = ±10V	±15V	10.0			mA
		V_{OUT} = ±3.2V	±5V	6.4			mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	20			mA
SR	Slew Rate	A_V = –1, R_L = 5k (Note 3)	±15V	50			V/μs
			±5V	15			V/μs
GBW	Gain Bandwidth	f = 200kHz, R_L = 10k	±15V	1.6			MHz
			± 5V	1.4			MHz
I_{SHDN}	Shutdown Input Current	SHDN = V_{EE} + 0.1V	±15V		– 30		μA
		SHDN = V_{CC}	±15V			5	μA
I_S	Supply Current		±15V			390	μA
			±5V			380	μA
		SHDN = V_{EE} + 0.1V	±5V		30		μA

Note 1: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 3: Slew rate is measured between ±8V on the output with ±12V input for ±15V supplies and ±2V on the output with ±3V input for ±5V supplies.

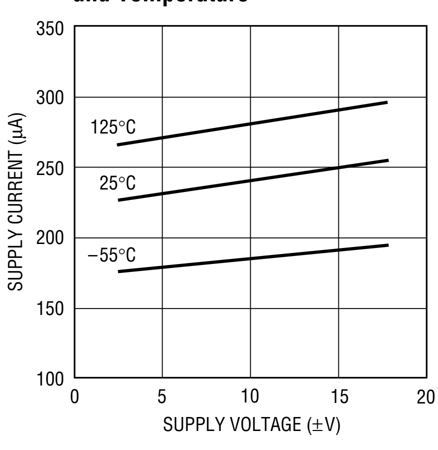
Note 4: Full-power bandwidth is calculated from the slew rate measurement: FPBW = (Slew Rate)/$2\pi V_P$.

Note 5: This parameter is not 100% tested.

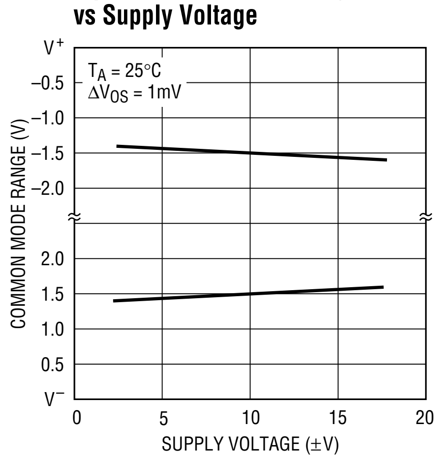
Note 6: The LT1351 is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and at 85°C. Guaranteed I grade parts are available; consult factory.

TYPICAL PERFORMANCE CHARACTERISTICS

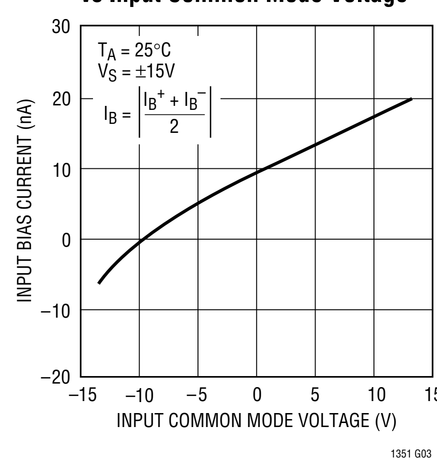
Supply Current vs Supply Voltage and Temperature



Input Common Mode Range vs Supply Voltage

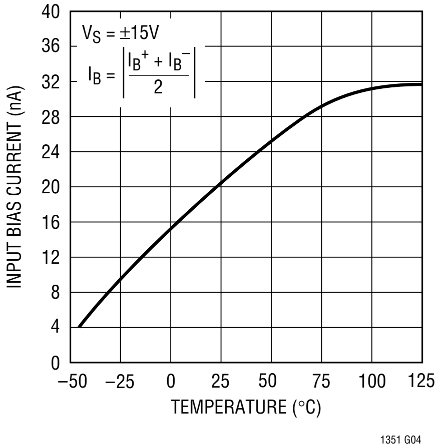


Input Bias Current vs Input Common Mode Voltage

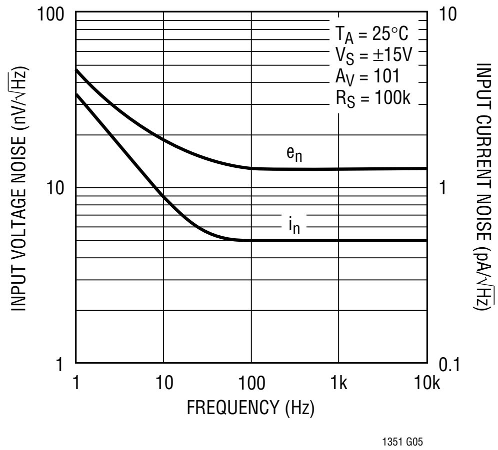


TYPICAL PERFORMANCE CHARACTERISTICS

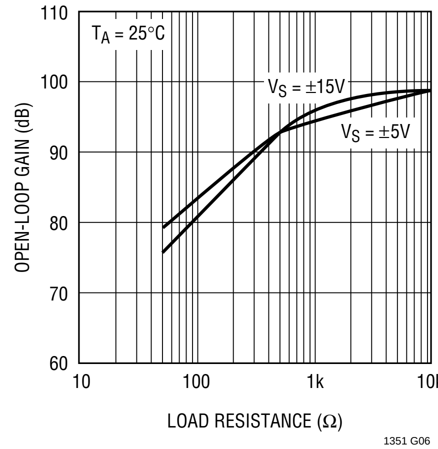
Input Bias Current vs Temperature



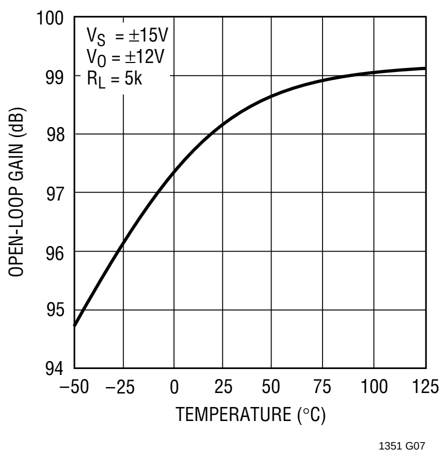
Input Noise Spectral Density



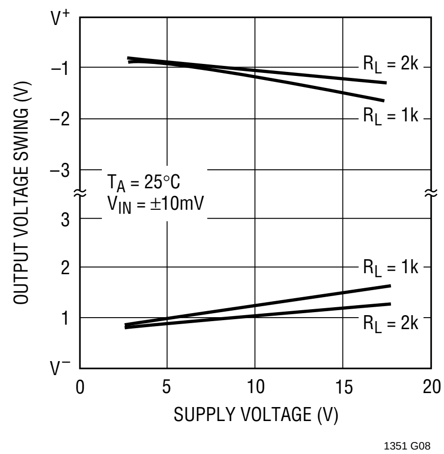
Open-Loop Gain vs Resistive Load



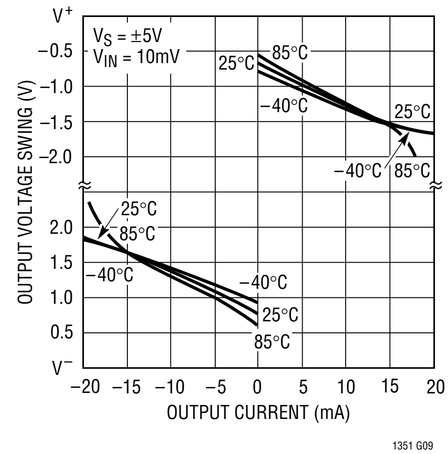
Open-Loop Gain vs Temperature



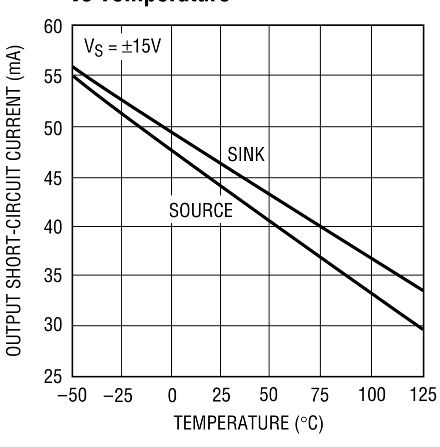
Output Voltage Swing vs Supply Voltage



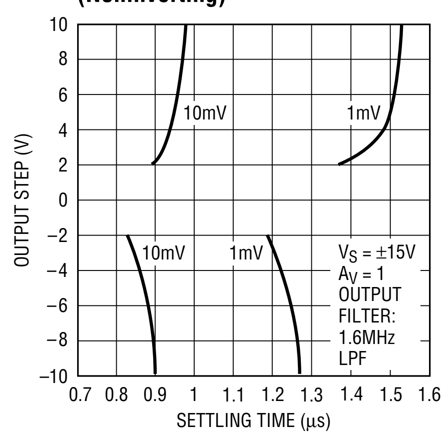
Output Voltage Swing vs Load Current



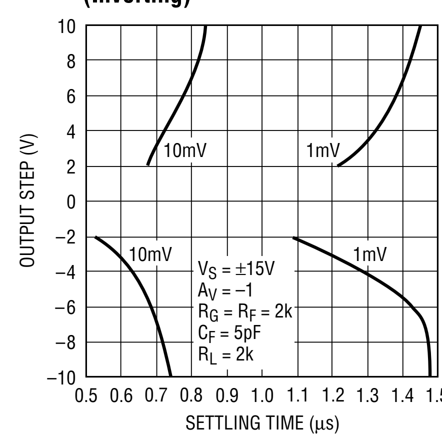
Output Short-Circuit Current vs Temperature



Settling Time vs Output Step (Noninverting)

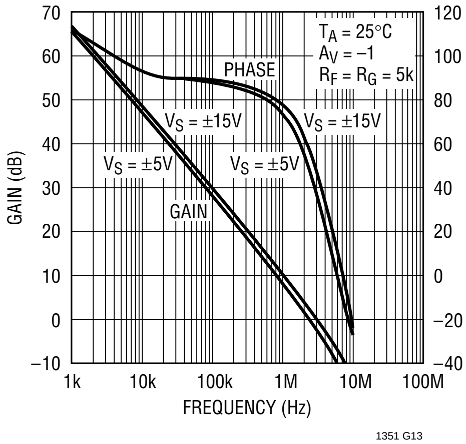


Settling Time vs Output Step (Inverting)

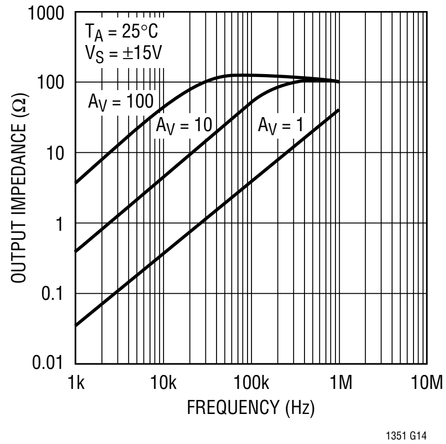


TYPICAL PERFORMANCE CHARACTERISTICS

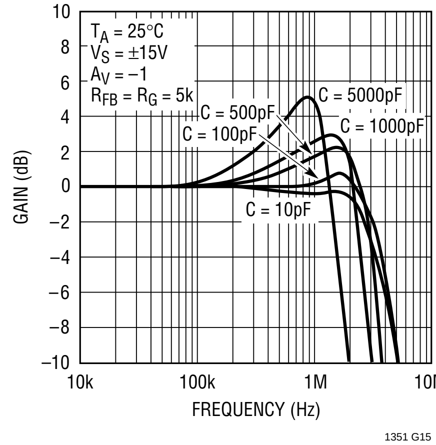
Gain and Phase vs Frequency



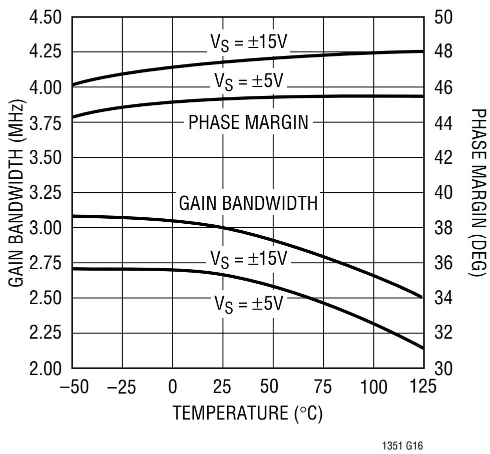
Output Impedance vs Frequency



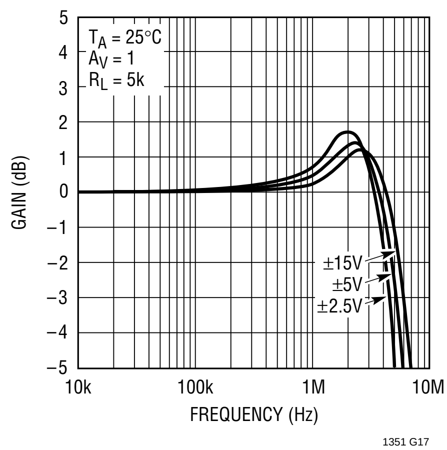
Frequency Response vs Capacitive Load



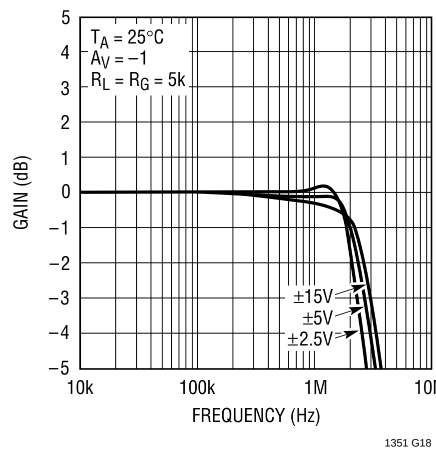
Gain Bandwidth and Phase Margin vs Temperature



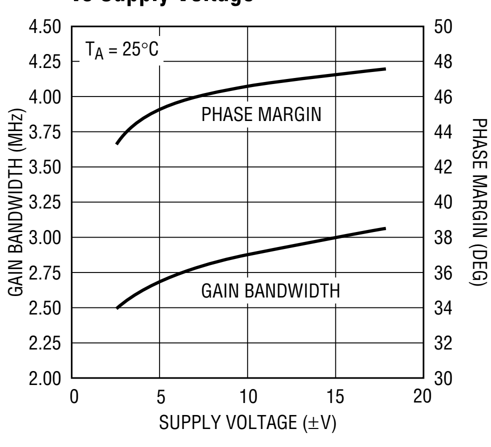
Frequency Response vs Supply Voltage (A_V = 1)



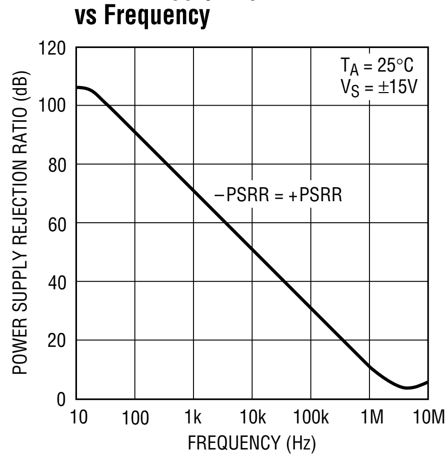
Frequency Response vs Supply Voltage (A_V = –1)



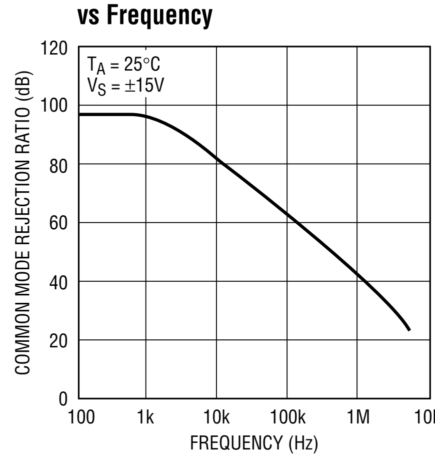
Gain Bandwidth and Phase Margin vs Supply Voltage



Power Supply Rejection Ratio vs Frequency

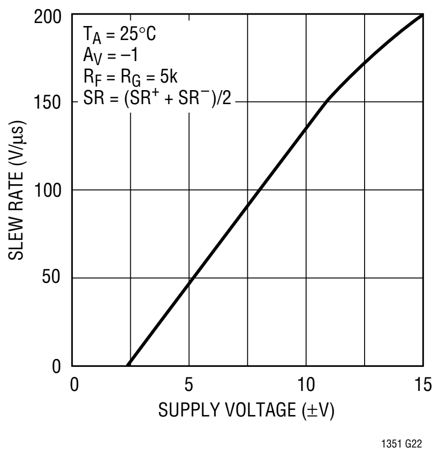


Common Mode Rejection Ratio vs Frequency

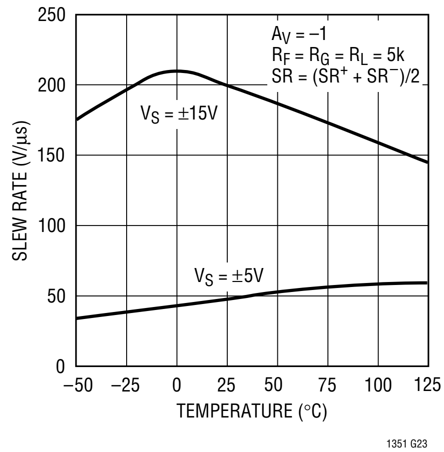


TYPICAL PERFORMANCE CHARACTERISTICS

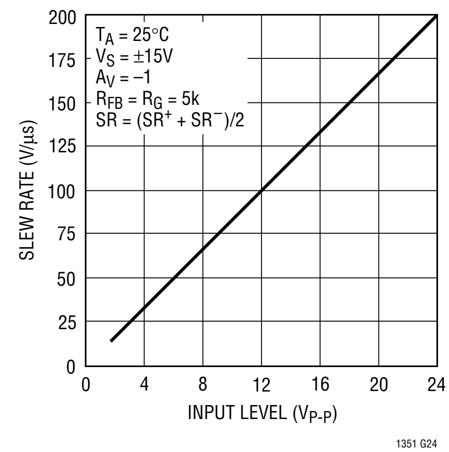
Slew Rate vs Supply Voltage



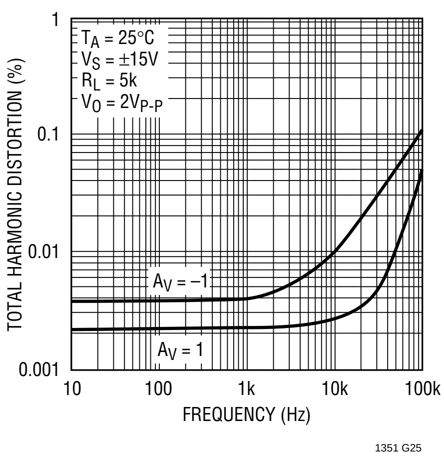
Slew Rate vs Temperature



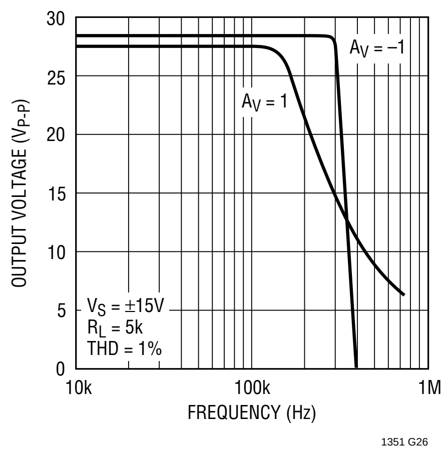
Slew Rate vs Input Level



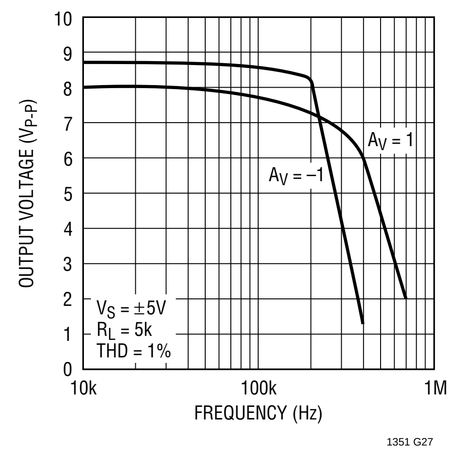
Total Harmonic Distortion vs Frequency



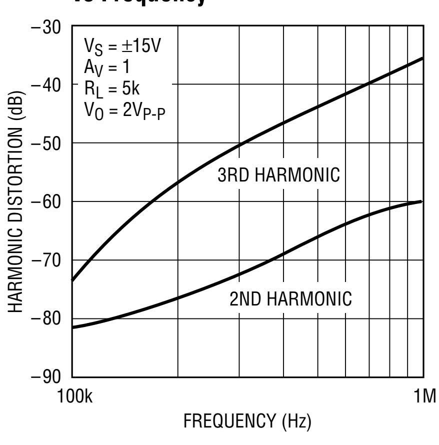
Undistorted Output Swing vs Frequency (±15V)



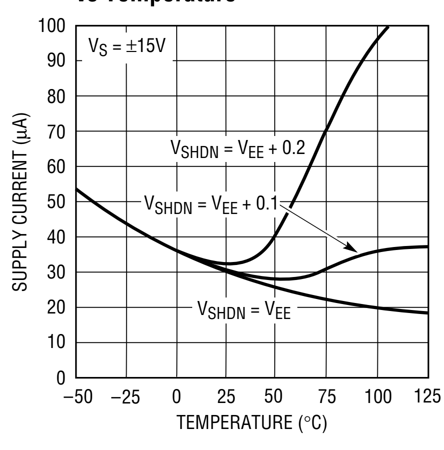
Undistorted Output Swing vs Frequency (±5V)



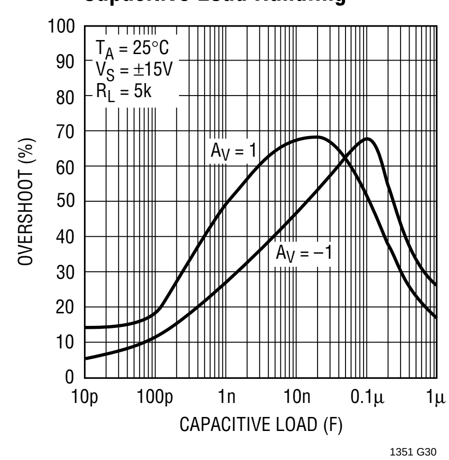
2nd and 3rd Harmonic Distortion vs Frequency



Shutdown Supply Current vs Temperature

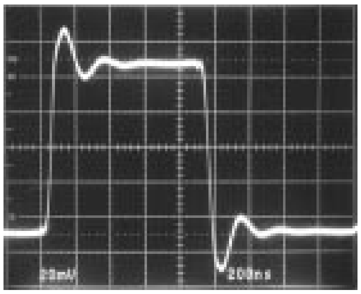


Capacitive Load Handling



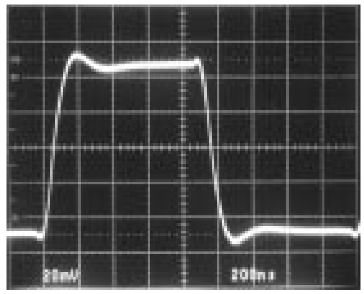
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient (A_V = 1)



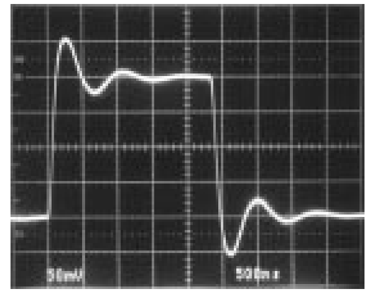
1351 G31

Small-Signal Transient (A_V = –1)



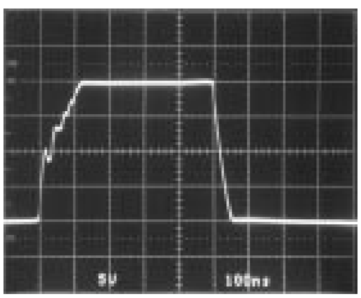
1351 G32

Small-Signal Transient (A_V = –1, C_L = 1000pF)



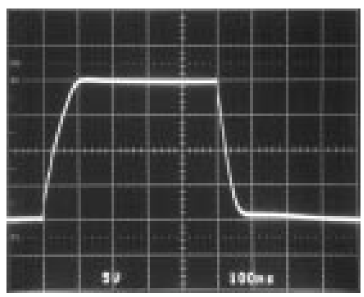
1351 G33

Large-Signal Transient (A_V = 1)



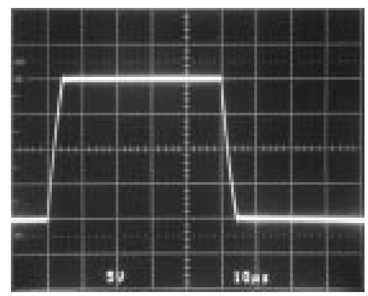
1351 G34

Large-Signal Transient (A_V = –1)



1351 G35

Large-Signal Transient (A_V = 1, C_L = 10,000pF)



1351 G36

APPLICATIONS INFORMATION

The LT1351 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1351 is shown in Figure 1.

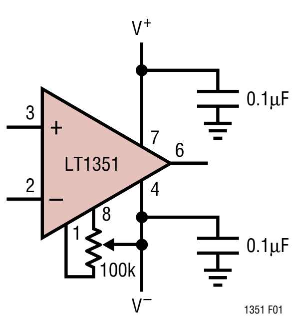


Figure 1. Offset Nulling

Layout and Passive Components

The LT1351 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). For details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 10k, a parallel capacitor of value, $C_F > (R_G)(C_{IN}/R_F)$ should be used to cancel the input pole and optimize dynamic performance. For applications where the DC

APPLICATIONS INFORMATION

noise gain is one and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be an I-to-V converter as shown in the Typical Applications section.

Capacitive Loading

The LT1351 is stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Graphs of Frequency Response vs Capacitive Load, Capacitive Load Handling and the transient response photos clearly show these effects.

Input Considerations

Each of the LT1351 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. *The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs*. Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Shutdown

The LT1351 has a Shutdown pin for conserving power. When this pin is open or 2V above the negative supply the part operates normally. When pulled down to V^- the supply current will drop to about 10μA. The current out of the Shutdown pin is also typically 10μA. In shutdown the amplifier output is not isolated from the inputs so the LT1351 cannot be used in multiplexing applications using the shutdown feature.

A level shift application is shown in the Typical Applications section so that a ground-referenced logic signal can control the Shutdown pin.

Circuit Operation

The LT1351 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic.

The inputs are buffered by complementary NPN and PNP emitter followers which drive R1, a 1k resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node and compensation capacitor C_T. Complementary followers form an output stage which buffers the gain node from the load. The output devices Q19 and Q22 are connected to form a composite PNP and composite NPN.

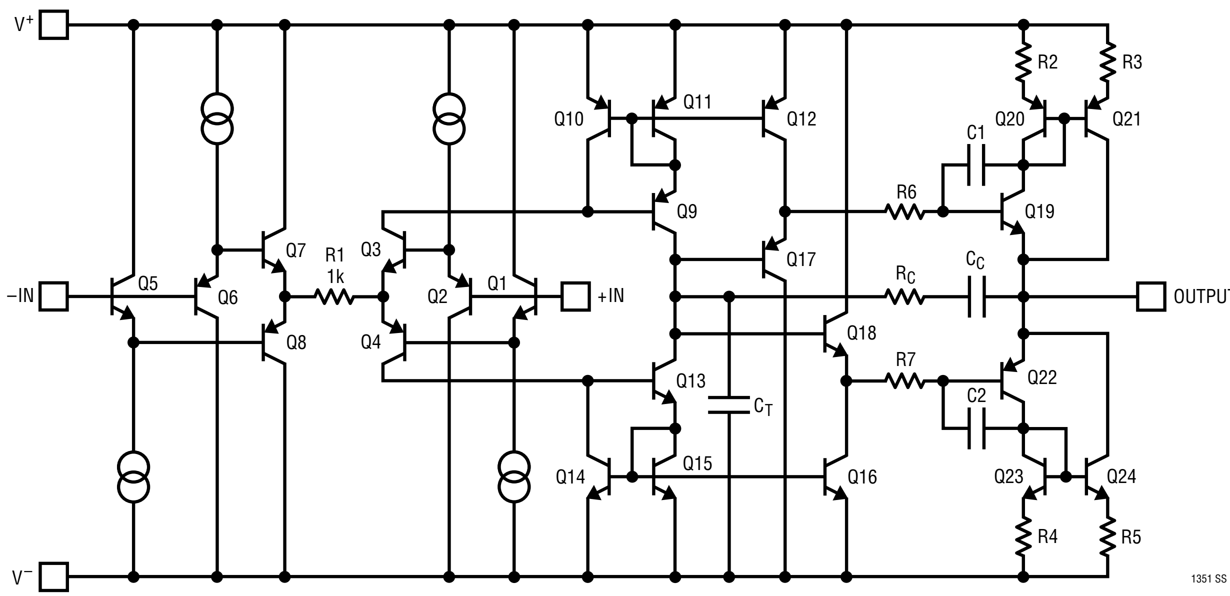
The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship.

Capacitive load compensation is provided by the R_C, C_C network which is bootstrapped across the output stage. When the amplifier is driving a light load the network has no effect. When driving a capacitive load (or a low value

APPLICATIONS INFORMATION

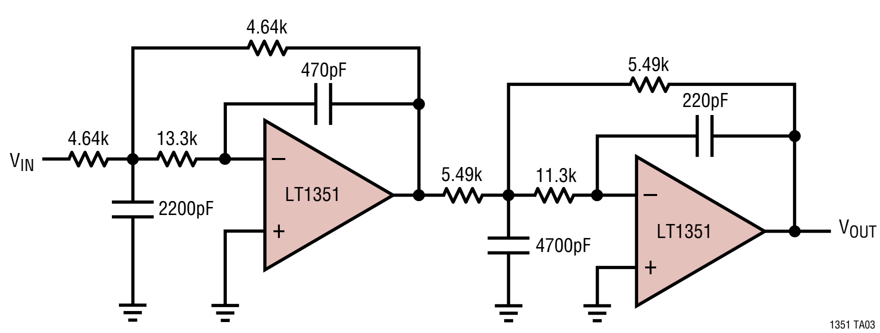
resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier and a zero is created by the RC combination, both of which improve the phase margin. The design ensures that even for very large load capacitances the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

SIMPLIFIED SCHEMATIC



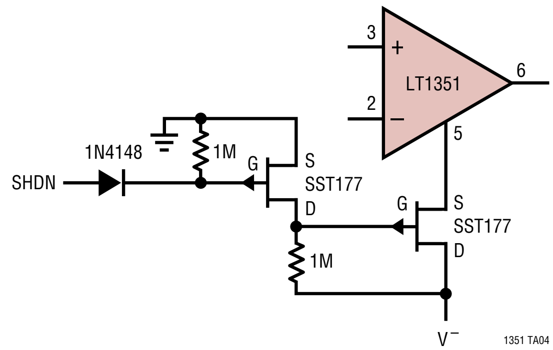
TYPICAL APPLICATIONS

20kHz, 4th Order Butterworth Filter

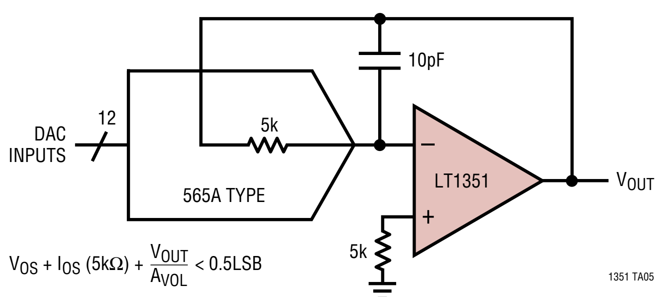


TYPICAL APPLICATIONS

Shutdown Circuit



DAC I-to-V Converter

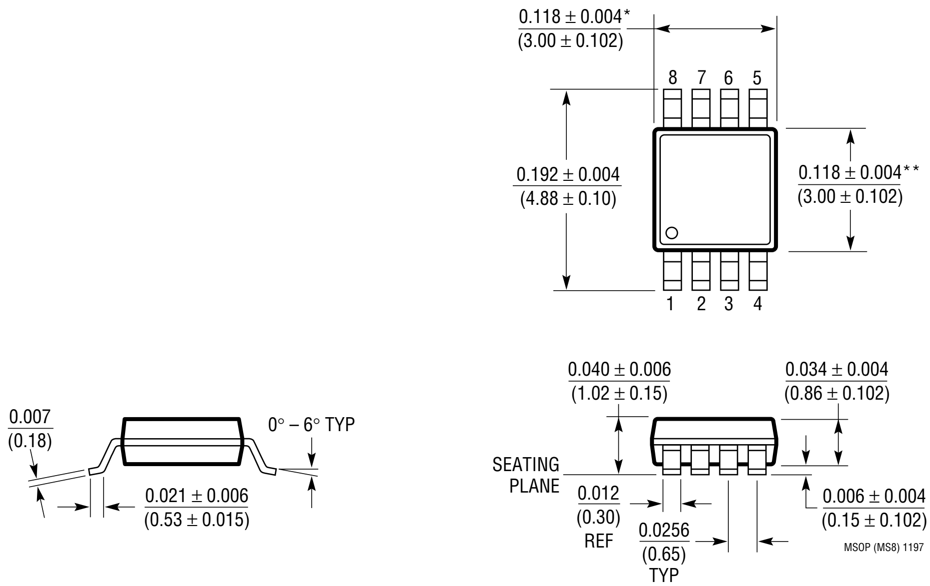


$V_{OS} + I_{OS}\,(5k\Omega) + \frac{V_{OUT}}{A_{VOL}} < 0.5LSB$

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



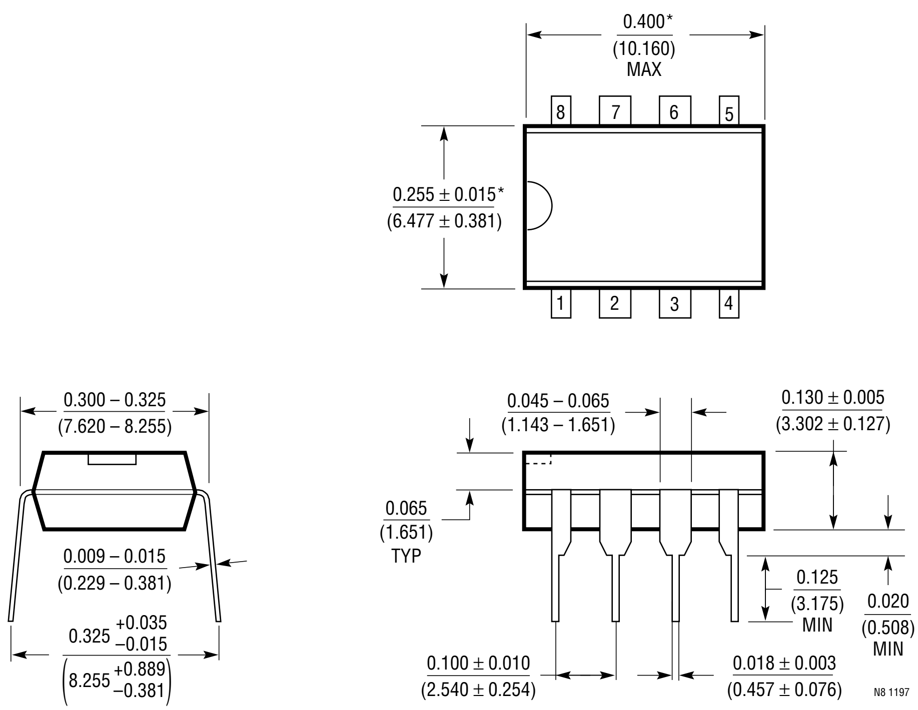
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

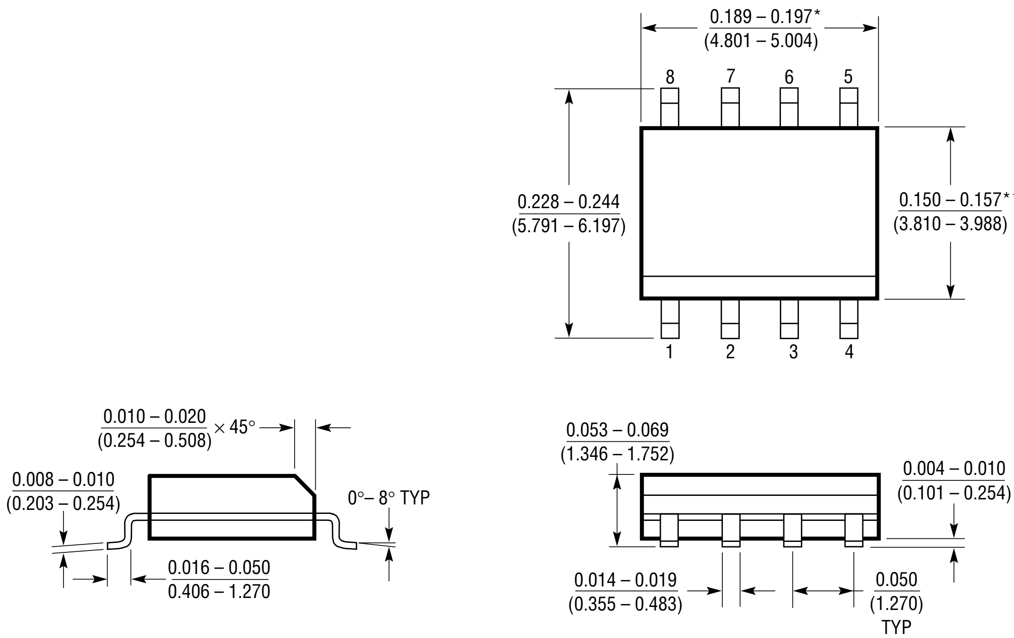


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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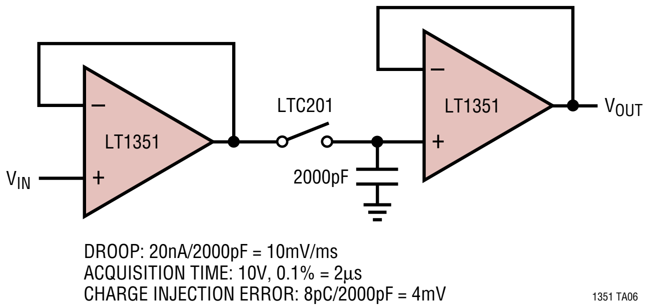
TYPICAL APPLICATION

Low Power Sample-and-Hold



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1352/LT1353	Dual/Quad 250µA, 3MHz, 200V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1354	1mA, 12MHz, 400V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads

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