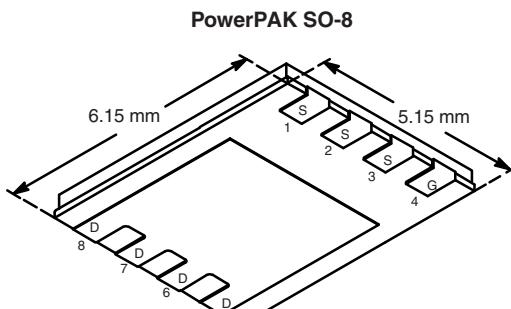


N-Channel 30 V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.00825 at $V_{GS} = 10$ V	15
	0.00975 at $V_{GS} = 4.5$ V	13

FEATURES

- Halogen-free According to IEC 61249-2-21
- Definition
- Extremely Low Q_{gd} for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

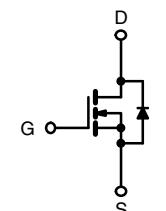


Bottom View

Ordering Information: Si7342DP-T1-E3 (Lead (Pb)-free)
Si7342DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- High-Side DC/DC Conversion
 - Notebook
 - Server



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	30	± 12	V
Gate-Source Voltage	V_{GS}			
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	15	9	A
		12	7	
Pulsed Drain Current	I_{DM}	± 60		A
Continuous Source Current (Diode Conduction) ^a	I_S	4.1	1.5	
Maximum Power Dissipation ^a	P_D	5	1.8	W
		3.2	1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^a	$t \leq 10$ s	R_{thJA}	20	25
	Steady State		53	70
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.1	3.2

Notes:

- Surface mounted on 1" x 1" FR4 board.
- See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

MOSFETS SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.6		1.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 70^\circ\text{C}$		10		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		0.0066	0.00825	Ω
		$V_{GS} = 4.5 \text{ V}$, $I_D = 13 \text{ A}$		0.0077	0.00975	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 15 \text{ A}$		65		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.73	1.1	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		1900		pF
Output Capacitance	C_{oss}			530		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 15 \text{ A}$		12.5	19	nC
Gate-Source Charge	Q_{gs}			3.9		
Gate-Drain Charge	Q_{gd}			2.1		
Gate Resistance	R_g		0.8	1.2	1.8	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}$, $R_L = 15 \Omega$ $I_D \geq 1 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_G = 6 \Omega$		13	20	ns
Rise Time	t_r			8	13	
Turn-Off Delay Time	$t_{d(\text{off})}$			48	75	
Fall Time	t_f			13	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$		36	55	

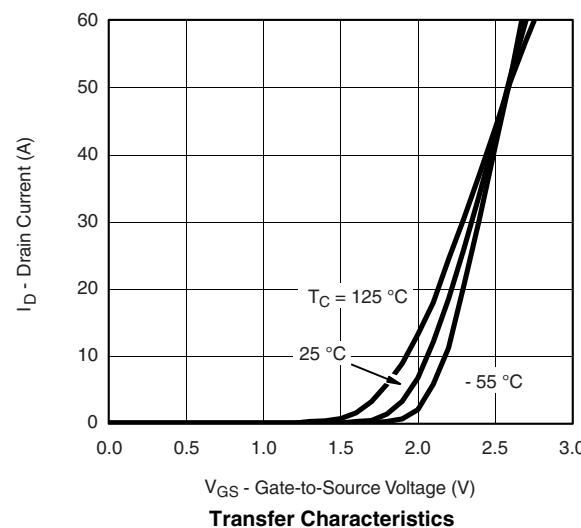
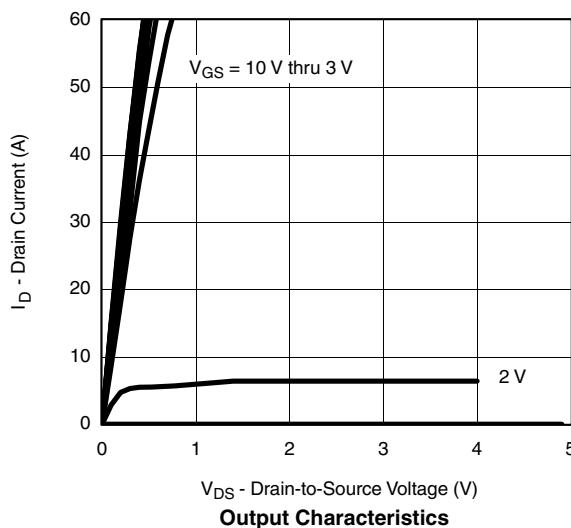
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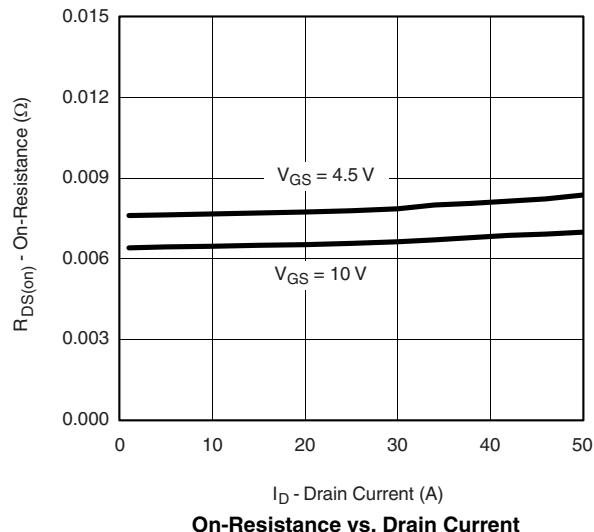
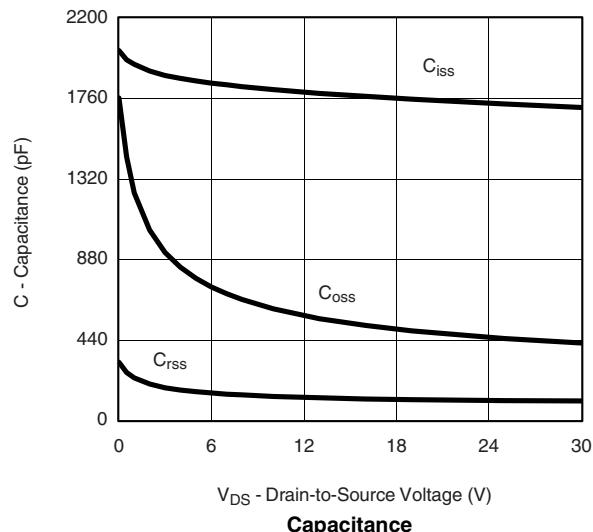
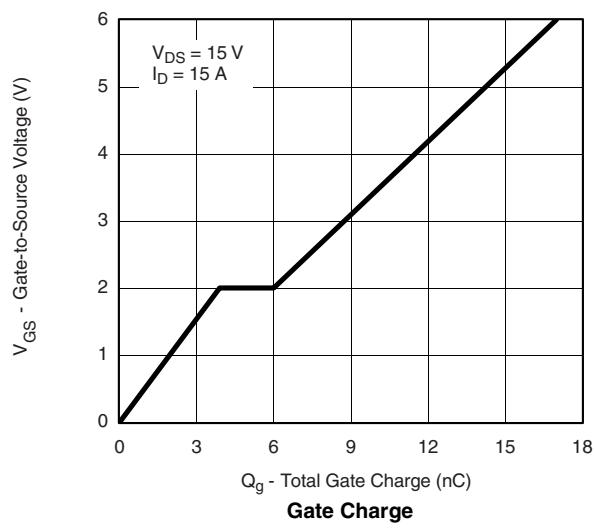
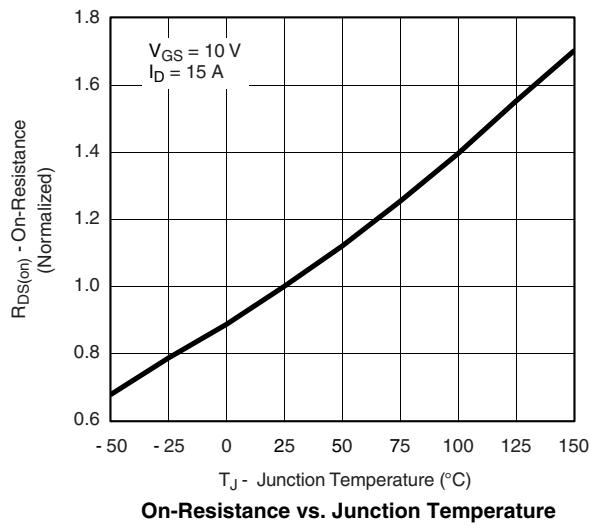
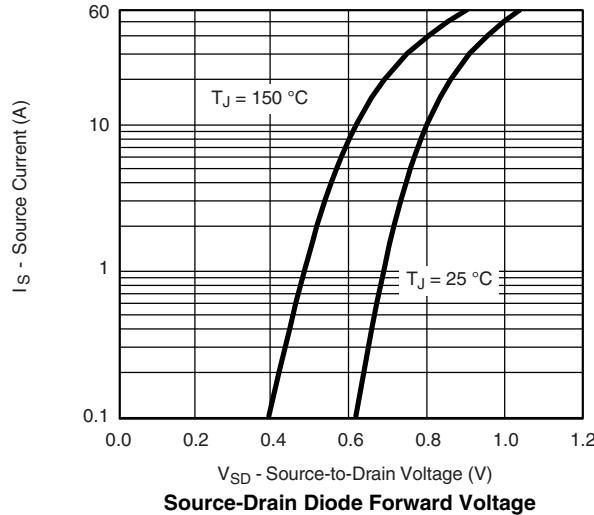
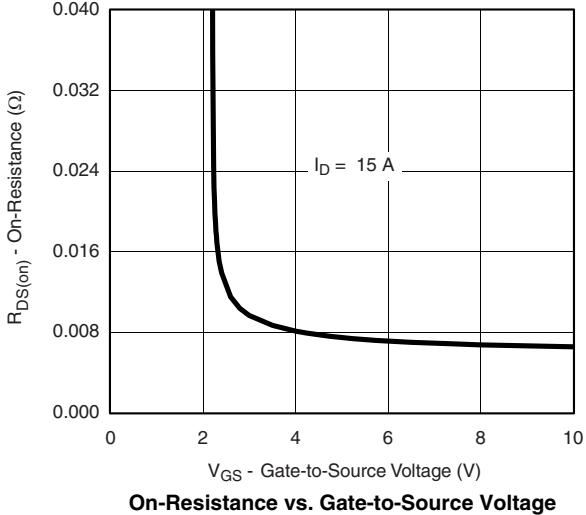
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$.

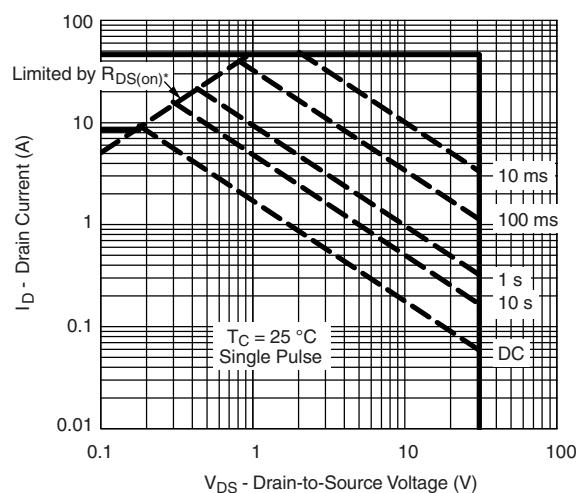
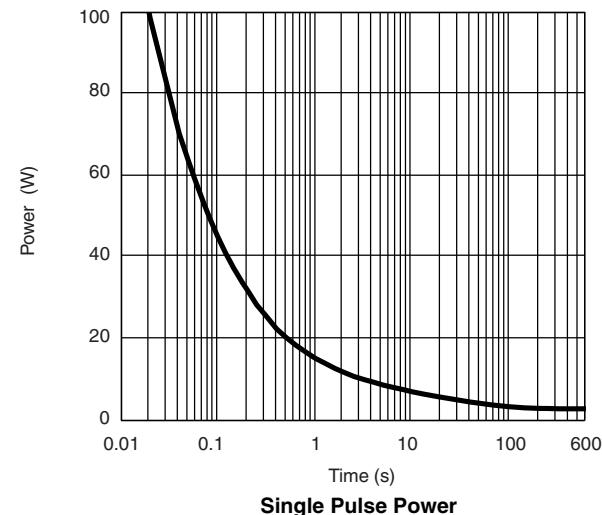
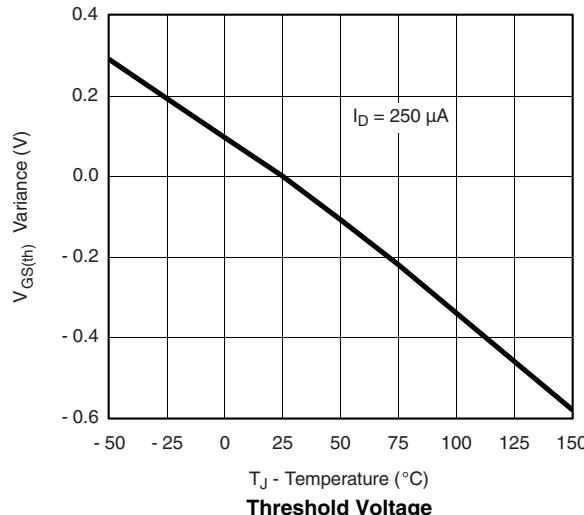
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

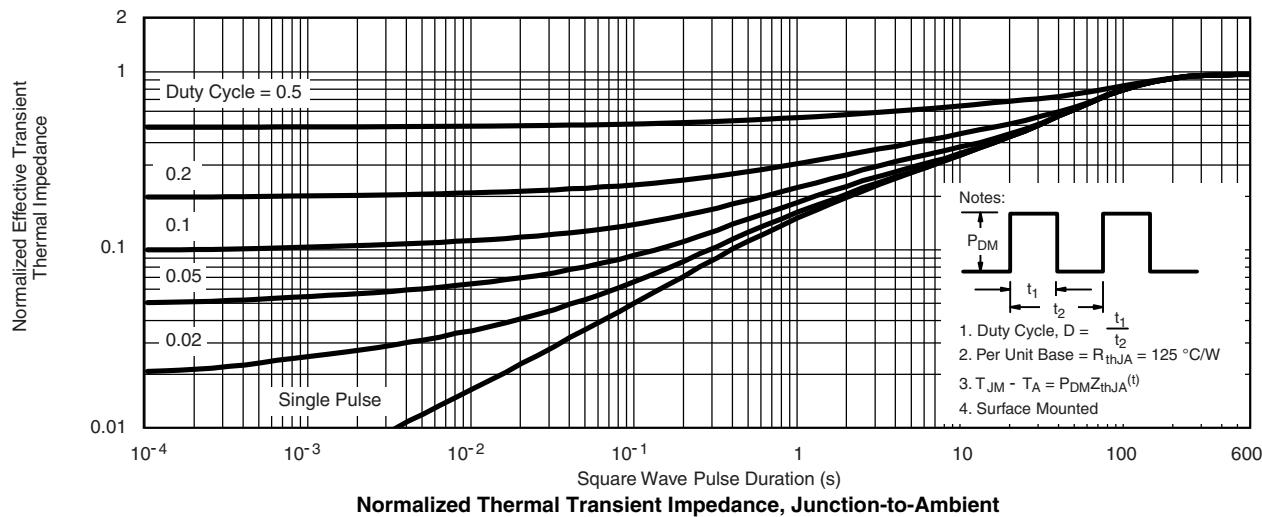
TYPICAL CHARACTERISTICS (25°C , unless otherwise noted)

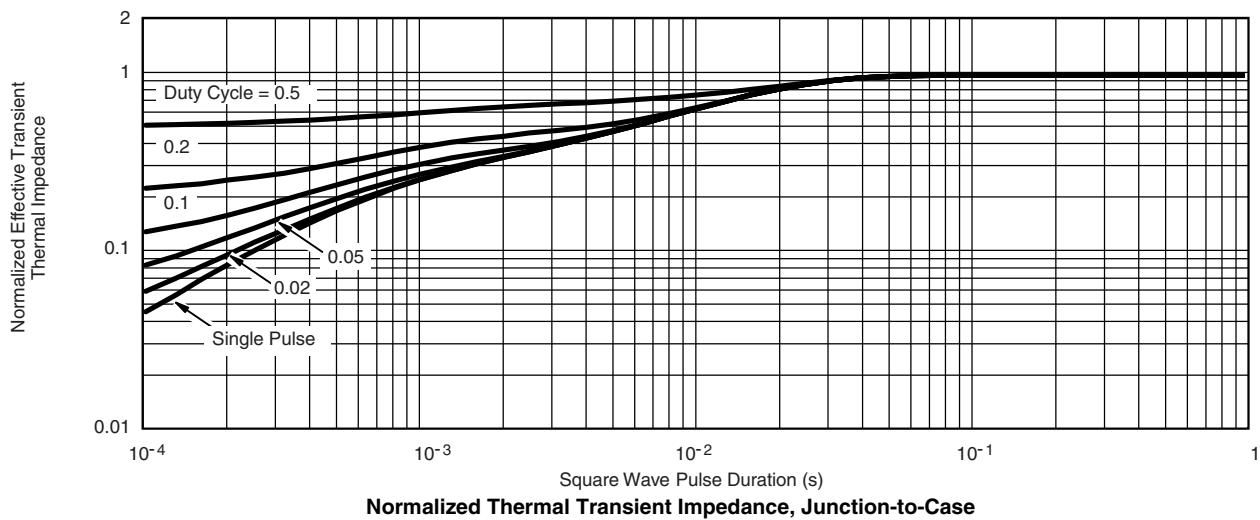


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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