TEXAS INSTRUMENTS

SN74AHC1GU04

SCLS343S – APRIL 1996 – REVISED OCTOBER 2016

SN74AHC1GU04 Single Inverter Gate

1 Features

- Operating Range of 2-V to 5.5-V V_{CC}
- Unbuffered Output
- ±8-mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Wireless and Telecom Infrastructure
- Audio Mixers
- TVs
- Set-Top-boxes
- Audio
- Servers
- Cameras: Surveillance
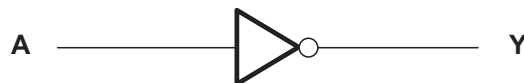- Software Defined Radio (SDR)

3 Description

The SN74AHC1GU04 device contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHC1GU04DBV	SOT-23 (5)	2.90 mm x 1.60 mm
SN74AHC1GU04DCK	SC-70 (5)	2.00 mm x 1.30 mm
SN74AHC1GU04DRL	SOT (5)	1.65 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (December 2014) to Revision S   **Page**

Changes from Revision Q (June 2005) to Revision R   **Page**

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View

```
        NC ⊏ 1        5 ⊐ V_CC
         A ⊏ 2
       GND ⊏ 3        4 ⊐ Y
```
Not to scale

DRL Package
5-Pin SOT
Top View

```
        NC ⊏ 1        5 ⊐ V_CC
         A ⊏ 2
       GND ⊏ 3        4 ⊐ Y
```
Not to scale

DCK Package
5-Pin SC70
Top View

```
        NC ⊏ 1        5 ⊐ V_CC
         A ⊏ 2
       GND ⊏ 3        4 ⊐ Y
```
Not to scale
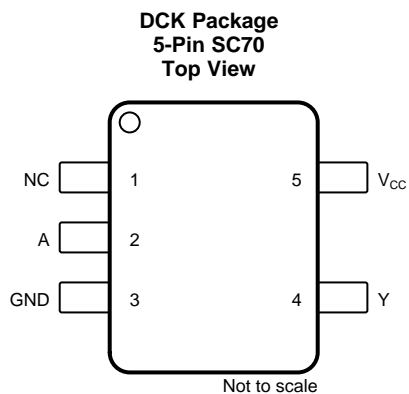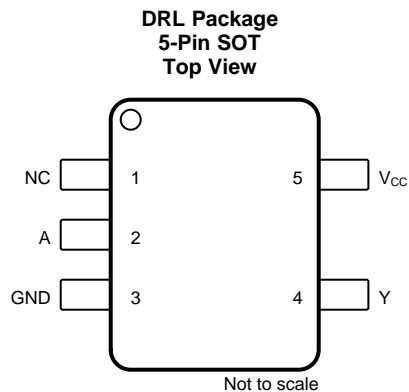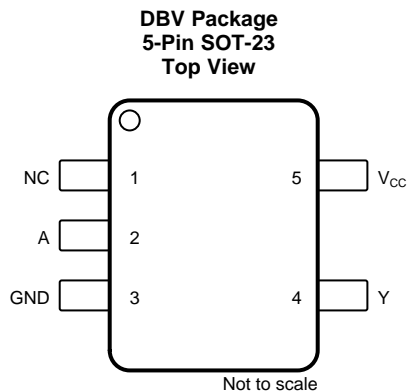
NC – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	No connection
2	A	I	Input A
3	GND	—	Ground pin
4	Y	O	Output Y
5	V_{CC}	—	Power pin

Product Folder Links: *SN74AHC1GU04*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
V_I	Input voltage [2]		−0.5	7	V
V_O	Output voltage [2]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through each V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.7		V
		$V_{CC} = 3$ V	2.4		
		$V_{CC} = 5.5$ V	4.4		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.3	V
		$V_{CC} = 3$ V		0.6	
		$V_{CC} = 5.5$ V		1.1	
V_{IH}	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Product Folder Links: *SN74AHC1GU04*

6.4 Thermal Information

THERMAL METRIC[1]		SN74AHC1GU04			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.3	287.6	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	119.9	97.7	105.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	65.	150.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.8	2.0	6.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.1	64.2	148.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			−40°C to +85°C		−40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	2 V	1.8	2		1.8		1.9		V
		3 V	2.7	3		2.7		2.7		
		4.5 V	4	4.5		4		4.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.2		0.2		0.1	V
		3 V			0.3		0.3		0.1	
		4.5 V			0.5		0.5		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.44		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10		10	μA
C_i	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			−40°C to +85°C		−40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	1	9.5	ns
t_{PHL}					5	7.1	1	8.5	1	9.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	1	13	ns
t_{PHL}					7.5	10.6	1	12	1	13	

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			−40°C to +85°C		−40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.5	5.5	1	6	1	6.5	ns
t_{PHL}					3.5	5.5	1	6	1	6.5	

Switching Characteristics, V$_{CC}$ = 5 V ± 0.5 V (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T$_A$ = 25°C			−40°C to +85°C		−40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t$_{PLH}$	A	Y	C$_L$ = 50 pF		5	7	1	8	1	8.5	ns
t$_{PHL}$					5	7	1	8	1	8.5	

6.8 Operating Characteristics

V$_{CC}$ = 5 V, T$_A$ = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C$_{pd}$	Power dissipation capacitance	No load,	f = 1 MHz	7.3	pF

6.9 Typical Characteristics
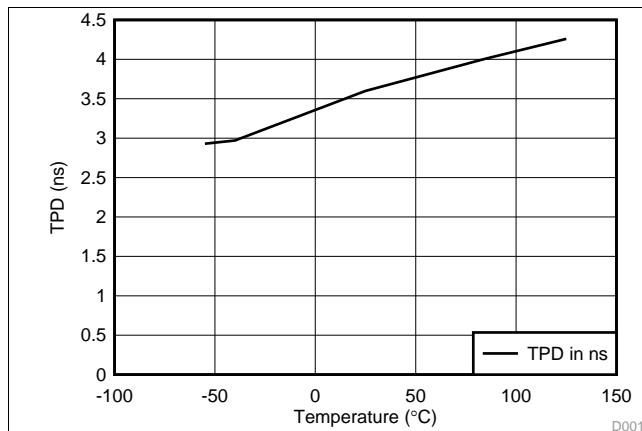
Figure 1. TPD vs Temperature

Figure 2. TPD vs V$_{CC}$ at 25°C

Product Folder Links: *SN74AHC1GU04*
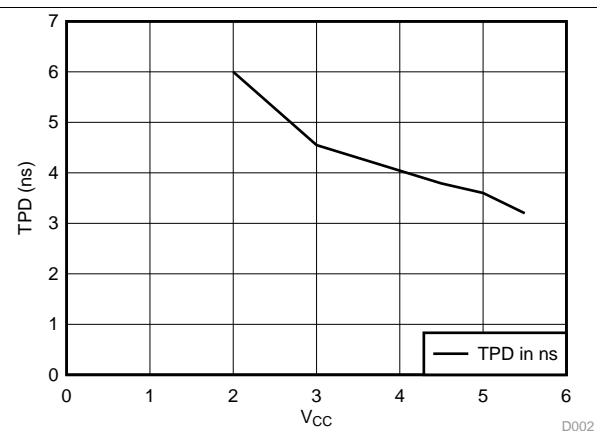
7 Parameter Measurement Information

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 3. Load Circuit And Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1GU04 device contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$. Internal circuitry consists of a single-stage inverter that can be used in analog applications, such as crystal oscillators.

8.2 Functional Block Diagram

A ⟶▷○⟶ Y

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Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- The unbuffered output is ideal for use in oscillator circuits

8.4 Device Functional Modes

Table 1 lists the functional modes of SN74AHC1GU04.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

Product Folder Links: *SN74AHC1GU04*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A CMOS inverter is used as a linear amplifier in oscillator applications. Similar to a conventional amplifier, their open-loop gain is a critical characteristic. The bandwidth of an inverter decreases as the operating voltage decreases. The open-loop gain of the AHC1GU04 device is shown in Figure 6.

9.2 Typical Application
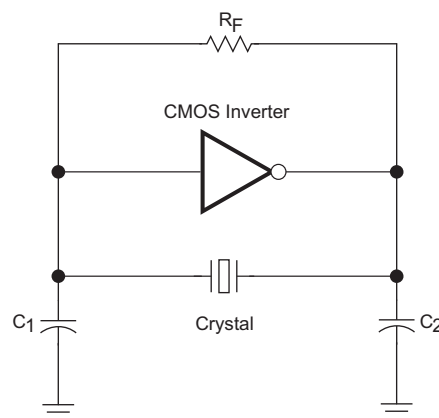
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Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – For rise time and fall time specifications, see $\Delta t/\Delta V$ in the *Recommended Operating Conditions* table.
   – For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions
   – Load currents should not exceed 25 mA per output and 50 mA total for the part.
   – Outputs should not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curve
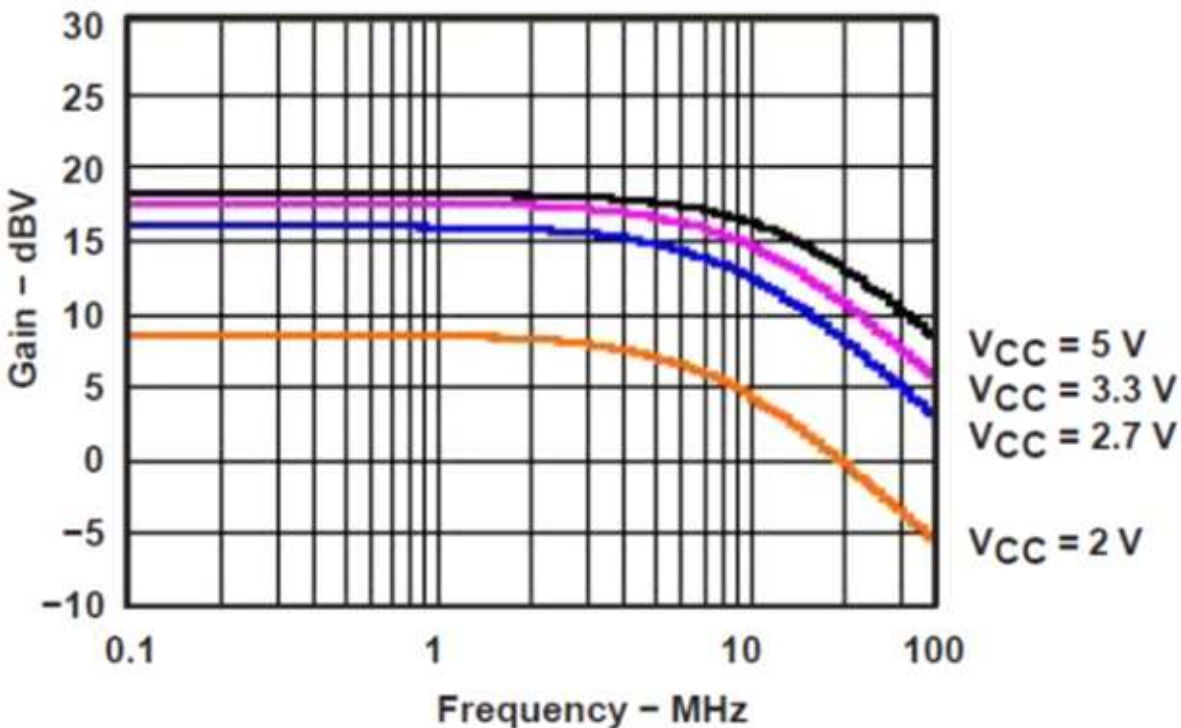
Figure 6. Open-Loop Gain

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Product Folder Links: *SN74AHC1GU04*

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.
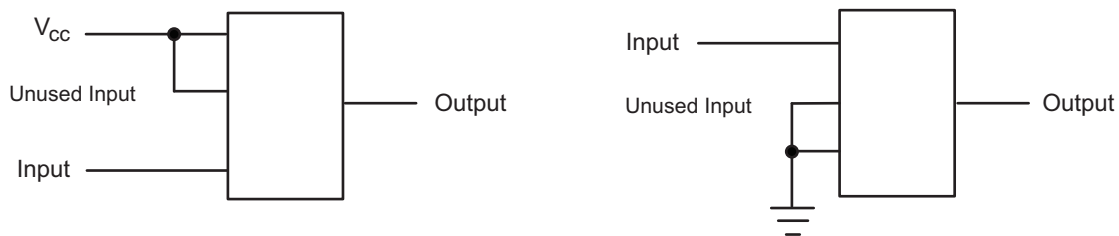
11.2 Layout Example

Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHC1GU04DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AU4G	Samples
74AHC1GU04DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AU4G	Samples
74AHC1GU04DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD3	Samples
SN74AHC1GU04DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(AU43, AU4G, AU4J, AU4L, AU4S)	Samples
SN74AHC1GU04DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(AU43, AU4G, AU4J, AU4L, AU4S)	Samples
SN74AHC1GU04DCK3	ACTIVE	SC70	DCK	5	3000	Pb-Free (RoHS)	SNBI	Level-1-260C-UNLIM	-40 to 85	ADY	Samples
SN74AHC1GU04DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(AD3, ADG, ADJ, AD L, ADS)	Samples
SN74AHC1GU04DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(AD3, ADG, ADJ, AD L, ADS)	Samples
SN74AHC1GU04DRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ADS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHC1GU04DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHC1GU04DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHC1GU04DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHC1GU04DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1GU04DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1GU04DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHC1GU04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1GU04DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1GU04DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHC1GU04DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHC1GU04DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
74AHC1GU04DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1GU04DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AHC1GU04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1GU04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1GU04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1GU04DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AHC1GU04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1GU04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1GU04DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

A

$\frac{1,70}{1,50}$

5X $\frac{0,27}{0,13}$

B

5   4

$\frac{1,30}{1,10}$

C

$\frac{1,70}{1,50}$

Pin 1 Index Area

1   2   3

0,50

5X $\frac{0,25}{0,15}$

⊕ | 0,10 Ⓜ | C | A | B
| 0,05 Ⓜ | C

$\frac{0,60}{0,50}$

⌒ | 0,05 | C

Seating Plane

$\frac{0,05}{0,00}$

C

$\frac{0,18}{0,08}$

1   2   3

5X $\frac{0,40}{0,20}$

5   4

Bottom View

4205622–2/D   08/2007

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
         B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.
             Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
         D. JEDEC package registration is pending.
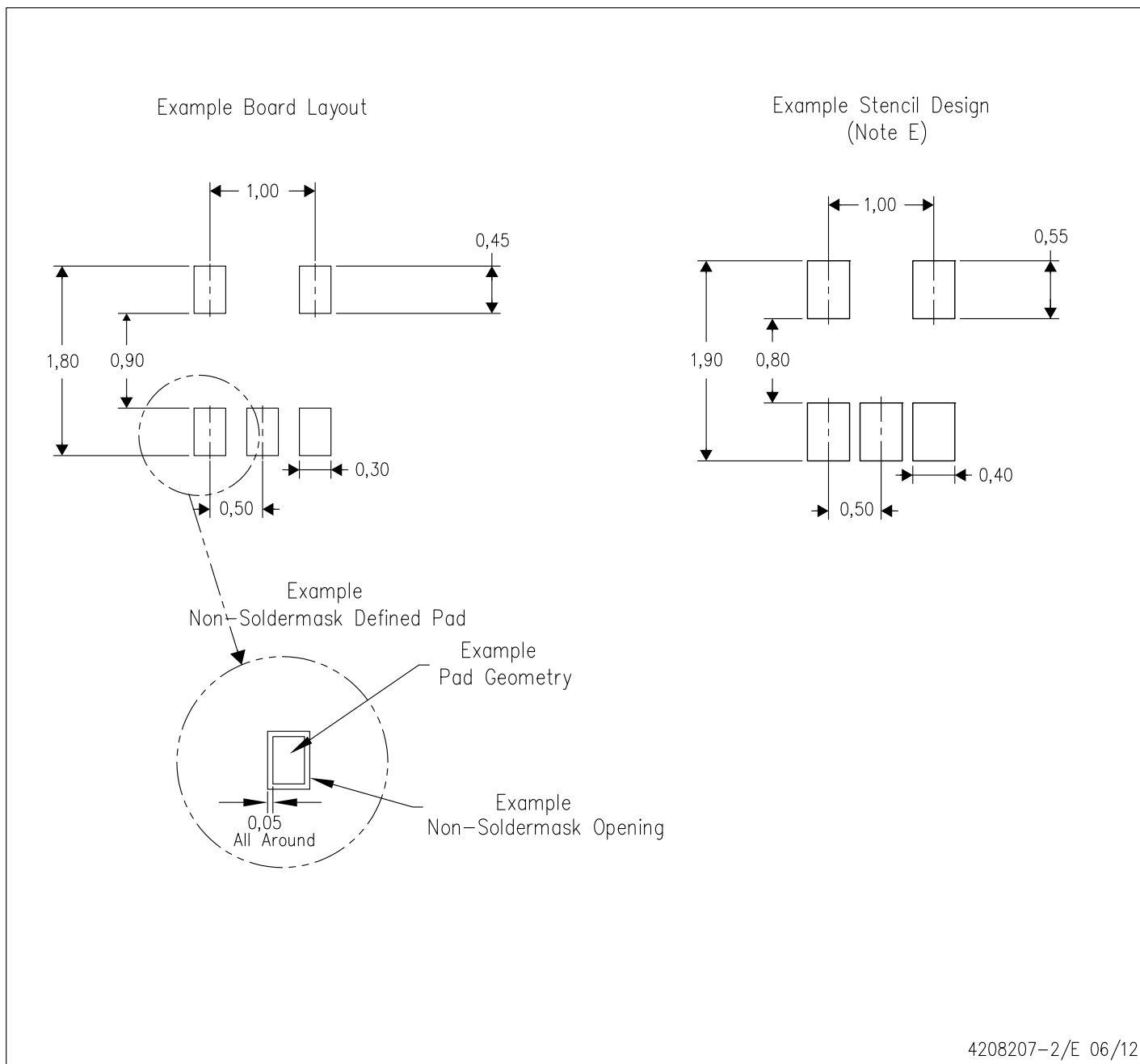
TEXAS
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DRL (R−PDSO−N5)   PLASTIC SMALL OUTLINE

Example Board Layout

Example Stencil Design
(Note E)

1,00

0,45

1,80   0,90

0,30

0,50

Example
Non−Soldermask Defined Pad

Example
Pad Geometry

Example
Non−Soldermask Opening

0,05
All Around

1,00

0,55

1,90   0,80

0,40

0,50

4208207−2/E 06/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
        E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
            if stencil manufacturing process allows for sufficient release at smaller opening.

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DCK (R−PDSO−G5) PLASTIC SMALL−OUTLINE PACKAGE

2,15 / 1,85

5 4

2,40 / 1,80

1,40 / 1,10

Pin 1 Index Area

1 3

0,65

5X 0,30 / 0,15

⊕ 0,10 Ⓜ

1,30

0,22 / 0,08

Gauge Plane
Seating Plane

0,15

0°−8°

0,46 / 0,26

1,10 / 0,80

0,10

Seating Plane

0,10 / 0,00

4093553−3/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  D. Falls within JEDEC MO−203 variation AA.

DCK (R−PDSO−G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x1,30

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−2/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

4214839/E   09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

PKG ℄

5X (1.1)

1

5X (0.6)

5

SYMM ℄

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX
ARROUND

0.07 MIN
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
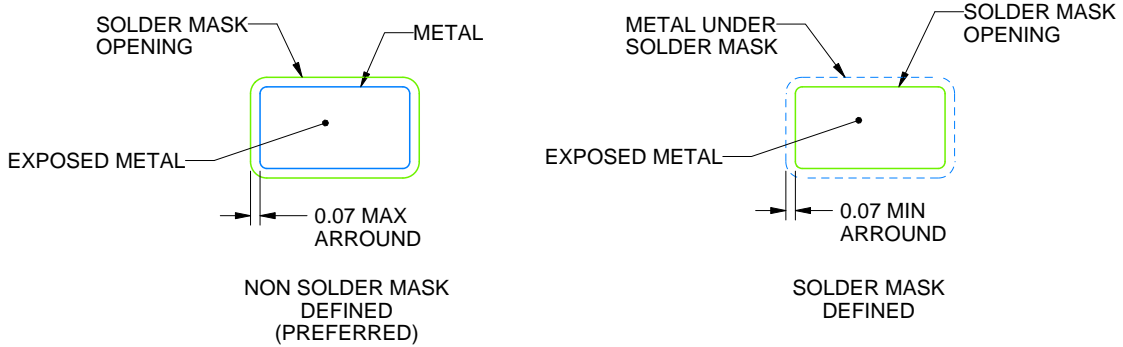
SOLDER MASK DETAILS

4214839/E   09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E   09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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