TPS8269xEVM-207

User's Guide

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This user's guide describes the characteristics, operation, and use of the TPS8269xEVM-207 evaluation module (EVM). The TPS8269xEVM-207 is a fully assembled and tested platform for evaluating the performance of the TPS8269xSIP high-frequency, synchronous, step-down DC-DC converters optimized for battery-powered portable applications. This document includes schematic diagrams, a printed circuit board (PCB) layout, bill of materials, and test data. Throughout this document, the abbreviations EVM and TPS8269xEVM and the term evaluation module are synonymous with the TPS8269xEVM-207 unless otherwise noted.

0.1 Introduction

The TPS8269xSIP device family is a high-frequency, synchronous, step-down DC-DC converters optimized for battery-powered portable applications. Intended for low-power applications, the TPS8269xSIP supports up to 500mA or 800mA and all TPS8269xSIP devices allow the use of low-cost chip inductors and capacitors. With a wide input voltage range of 2.3 V to 4.8 V, the devices support applications powered by lithium-ion (Li-Ion) batteries with extended voltage ranges. Different fixed voltage output versions of the TPS8269xSIP are available. These converters operate at a regulated 3-MHz switching frequency and enter a power-save mode operation under light load currents in order to maintain high efficiency over the entire load current range. A pulse frequency modulation (PFM) mode extends the battery life by reducing the quiescent current to 23 µA (typ) during light load operation.

0.1.1 Features

- Input Voltage Range: 2.3 V up to 4.8 V
- Fixed Output Voltages
- Up to 800-mA Output Current
- Sub 1-mm Profile Solution
- 3-MHz Regulated Frequency Operation
- Current Overload and Thermal Shutdown (Optional)
- Total Solution Size: < 6.7 mm^2
- Low Ripple Light-Load PFM Mode

0.1.2 Applications

- LDO Replacement
- Cell Phones, Smart-Phones
- PoL Applications

0.1.3 EVM Ordering Options

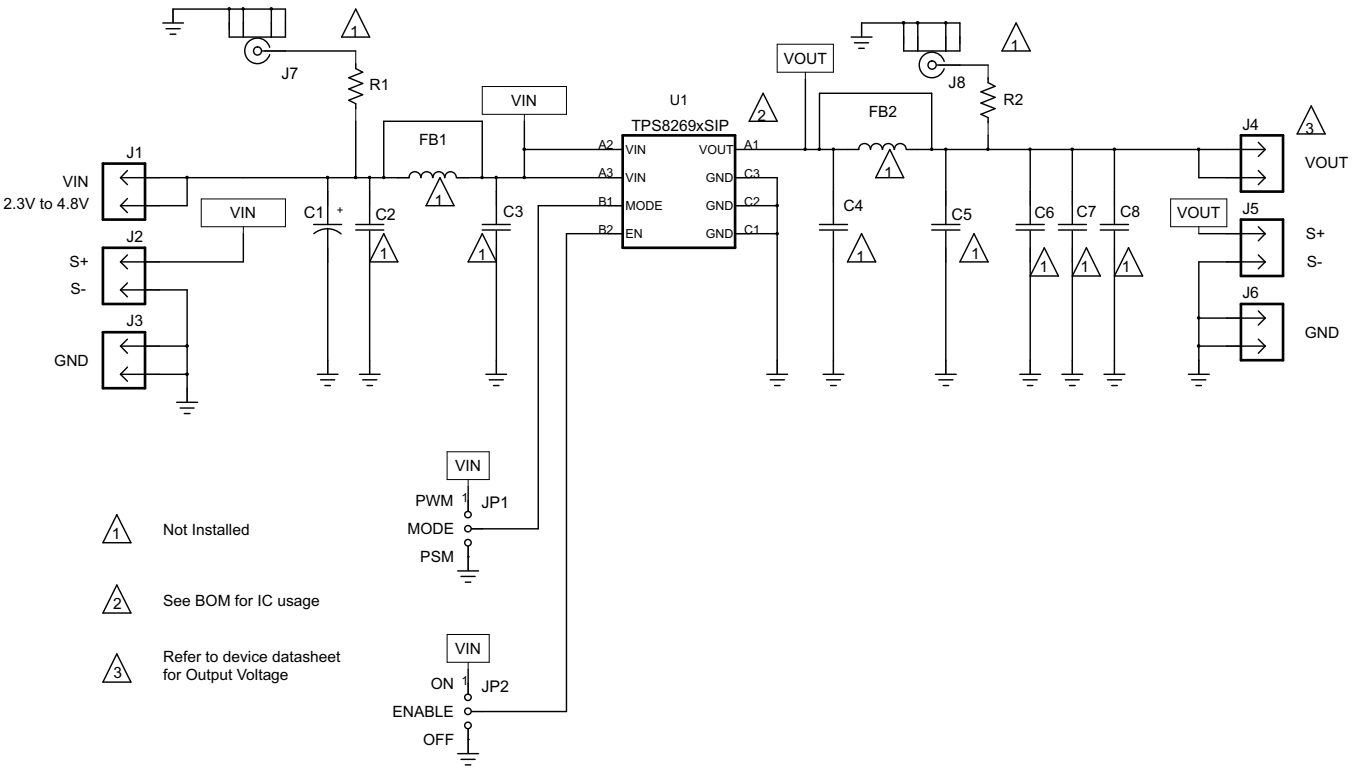
Table 0-1 provides the ordering information for the various EVM options.

Table 0-1. Ordering Information

Orderable EVM Number	Device Part Number	Output Voltage	Maximum Output Current
TPS82693EVM-207	TPS82693	2.85 V	800 mA

TPS8269xEVM Schematic

Figure 1-1 illustrates the TPS8269xEVM-207 schematic.



NOTE: For reference only; see Table A-1 for specific values.

Figure 1-1. TPS8269xEVM Schematic

Connector and Test Point Descriptions

2.1 Input / Output Connectors: TPS8269xEVM

2.1.1 J1 V_{IN}

This header is the positive connection to the input power supply. The power supply must be connected between J1 and J3 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 2.3 V and 4.8 V.

2.1.2 J2 S+ / S–

J2 S+ / S– are the sense connection for the input of the converter. Connect a voltmeter, sense connection of a power supply, or oscilloscope to this header.

2.1.3 J3 GND

This header is the return connection to the input power supply. Connect the power supply between J3 and J1 (V_{IN}). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 2.3 V and 4.8 V.

Capacitor C1 compensates for parasitic inductance as a result of the wires from the DC power supply to the EVM. It is not required in an actual application circuit.

2.1.4 J4 V_{OUT}

This header is the positive output of the step-down converter. The TPS8269x has fixed output voltages; refer to the specific device data sheet for detailed information on the device output voltage.

2.1.5 J5 S+ / S–

J5 S+ / S– are the sense connection for the output of the converter. Connect a voltmeter, sense connection of an electronic load, or oscilloscope to this header.

2.1.6 J6 GND

J6 is the return connection of the converter. A load can be connected between J6 and J4 (V_{OUT}).

2.2 Jumpers and Switches

2.2.1 JP1 ENABLE

This jumper can enable or disable the converter on the EVM. Placing a shorting bar between ENABLE and ON turns on the converter. Placing a shorting bar between ENABLE and OFF disables the converter.

2.2.2 JP2 MODE

This jumper can enable or disable the power-saving mode (PSM) under light loads. Placing a shorting bar between MODE and pulse width modulation (PWM) disables the PSM. If the PSM is disabled, the converter operates in forced PWM mode over the entire load current range.

Placing a shorting bar between MODE and PSM enables the power-saving mode. The device operates in power-saving mode under light load conditions. See the specific device data sheet for detailed information.

Test Configuration

3.1 Hardware Setup

Figure 3-1 illustrates a typical hardware test configuration.

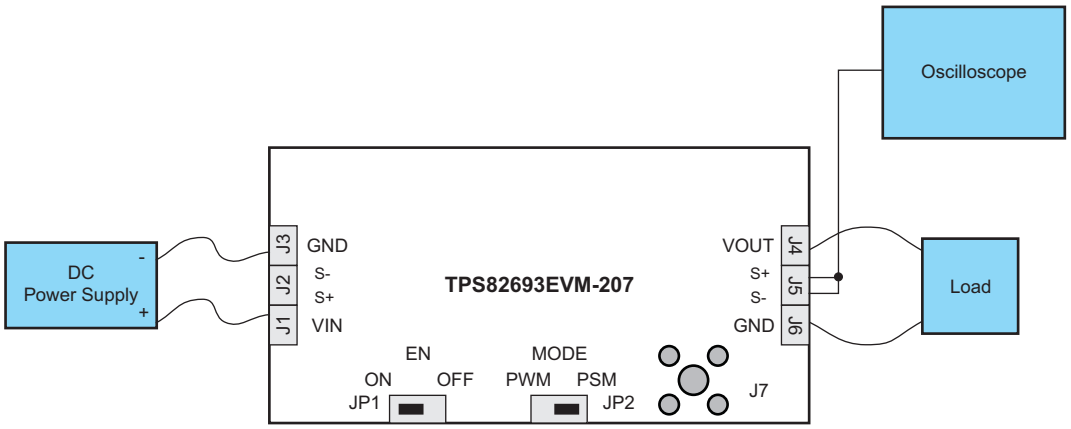


Figure 3-1. Hardware Board Connection

3.2 Procedure

Follow these procedures when configuring the EVM for testing.

CAUTION

Many of the components on the TPS8269xEVM-207 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses should also be worn.

- Work at an ESD workstation. Make sure that any wrist straps, bootstraps, or mats are connected and reference the user to earth ground before power is applied to the EVM. Electrostatic smocks and safety glasses should also be worn.
- Connect a DC power supply between J1 and J3 on the TPS8269xEVM. Note that the input voltage should range from 2.3 V to 4.8 V. Keep the wires from the input power supply to EVM as short as possible and twisted.
- Connect a DC voltmeter or oscilloscope to the output sense connection of the EVM.
- A load can be connected between J4 and J6 on the TPS8269xEVM.
- To enable the converter, connect the shorting bar on JP1 between ENABLE and ON on the TPS8269xEVM.
- The TPS8269xEVM has a feature that allows users to switch between PSM under light loads and forced PWM mode, with jumper JP2.

TPS8269xEVM Test Data

This section presents typical performance data for the TPS8269xEVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these results are presented for reference and may differ from actual results obtained by some users.

4.1 Thermal Performance

Figure 4-1 and Figure 4-2 show the typical thermal performance for the TPS82693 for two load scenarios, respectively.

4.1.1 Thermal Measurement TPS82693 , I_{OUT} = 400 mA

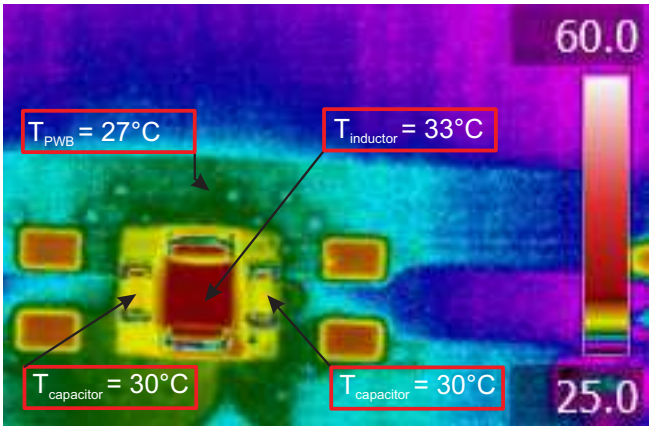


Figure 4-1. V_{IN} = 3.6 V, V_{OUT} = 2.85 V, I_{OUT} = 400 mA 80-mW Power Dissipation at Room Temperature

4.1.2 Thermal Measurement TPS82693 , I_{OUT} = 800 mA

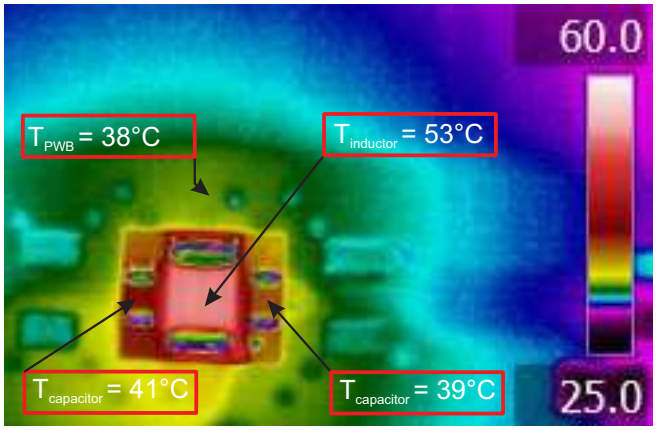


Figure 4-2. V_{IN} = 3.6 V, V_{OUT} = 2.85 V, I_{OUT} = 800 mA 330-mW Power Dissipation at Room Temperature

TPS8269xEVM Assembly Drawings and Layout

Figure 5-1 through Figure 5-5 show the design of the show the design of the TPS8269xEVM-207 printed circuit boards. The EVM was designed using a four-layer, 1-ounce copper-clad PCB with all components in an active area on the top side of the board. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS8269xEVM-207 PCBs.

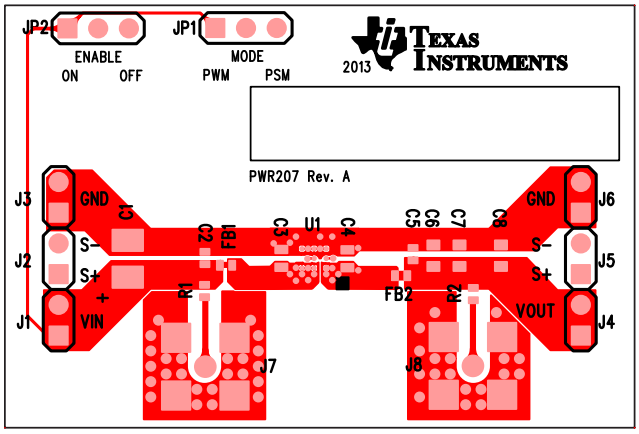


Figure 5-1. TPS8269xEVM Component Placement

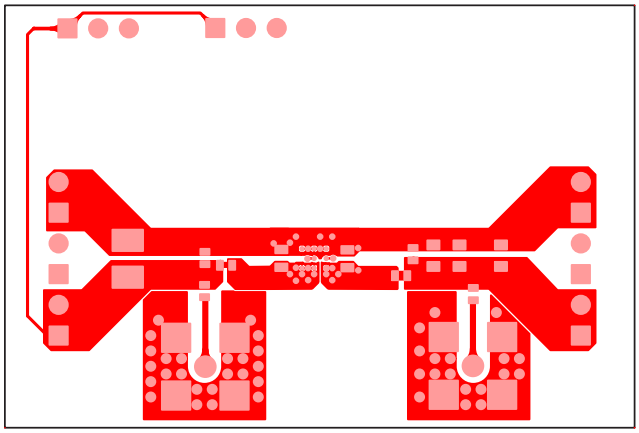


Figure 5-2. TPS8269xEVM Top Layer

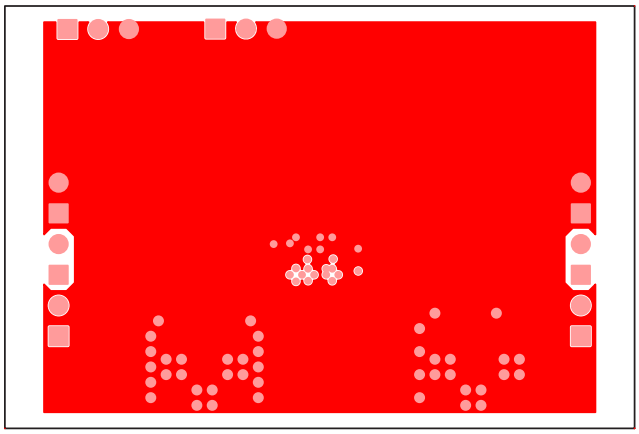


Figure 5-3. TPS8269xEVM Internal Layer 1

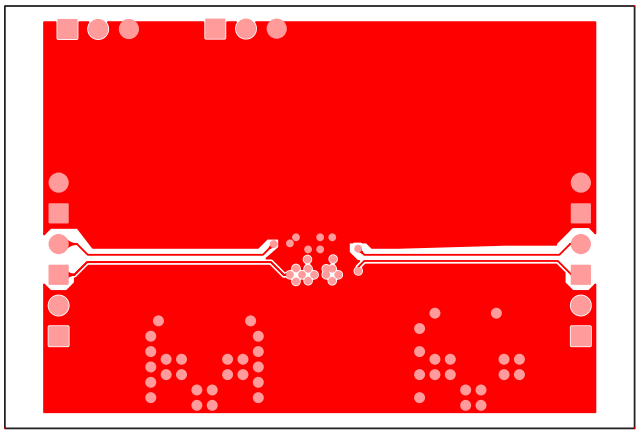


Figure 5-4. TPS8269xEVM Internal Layer 2

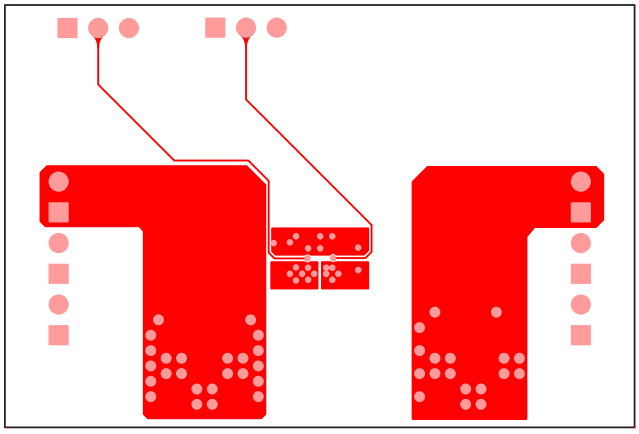


Figure 5-5. TPS8269xEVM Bottom Layer

Appendix

A.1 Bill of Materials

Table A-1 lists the bill of materials for the TPS8269xEVM.

Table A-1. TPS8269xEVM-207 Bill of Materials

EVM Device Option: Count		RefDes	Value	Description	Size	Part Number	Mfr
-001	-002						
0	0	C1	150 µF	Capacitor, Tantalum, 6.3 V, 25 mΩ, 20%	3528(B)	T520B157M006ATE025	Kemet
1	1	C2, C3, C4, C5, C6, C7, C8	Open	Capacitor, Ceramic	0603	Std	Std
6	6	J1, J2, J3, J4, J5, J6	PEC02SAAN	Header, Male 2-pin, 100 mil spacing	0.10 in x 2	PEC02SAAN	Sullins
0	0	J7, J8	Open	Connector, SMA , Straight, PC mount	0.210 in^2	901-144-8RFX	AMP
2	2	JP1, JP2	PEC03SAAN	Header, Male 3-pin, 100 mil spacing	0.10 in x 3	PEC03SAAN	Sullins
0	1	U1	TPS82693SIP	IC, 800-mA, High-Freq µModule Step-Down Converter	SIP-8	TPS82693	TI

A.2 Marking Information

Table A-2 provides the marking information for this EVM.

Table A-2. Marking Information

Assembly Number	Marking Text
PWR207-002	TPS82693EVM-207

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