ISL29020

A Low Power, High Sensitivity, Light-to Digital Sensor With I2C Interface

FN6505
Rev 1.00
August 20, 2009

The ISL29020 is a low power, high sensitivity, integrated light sensor with I^2C (SMBus Compatible) interface. Its state-of-the-art photodiode array provides close-to human eye response and good IR rejection. This ADC is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. The lux range select feature allows the user to program the lux range for optimized counts/lux.

In normal operation, typical power consumption 55µA. In order to further minimize power consumption, two power-down modes have been provided. If polling is chosen over continuous measurement of light, the auto-power-down function shuts down the whole chip after each ADC conversion for the measurement. The other power-down mode is controlled by software via the I^2C interface. The power consumption can be reduced to less than 1µA when powered down.

Designed to operate on supplies from 2.25V to 3.3V with I^2C supply from 1.7V to 3.6V, the ISL29020 is specified for operation over the -40°C to +85°C ambient temperature range.

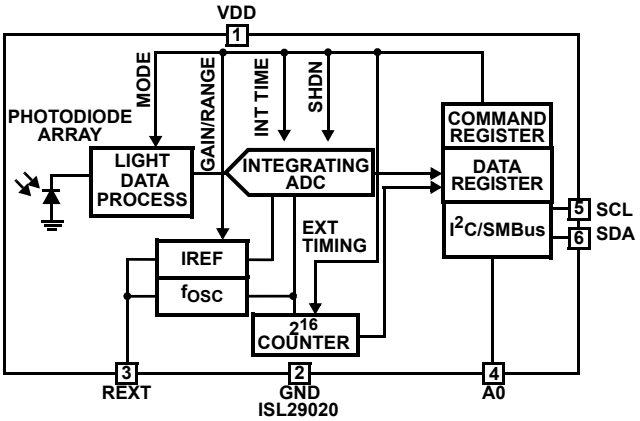
Ordering Information

PART NUMBER (Note)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL29020IROZ-T7*	6 Ld ODFN	L6.2x2.1
ISL29020IROZ-EVALZ	Evaluation Board (Pb-free)	

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Features

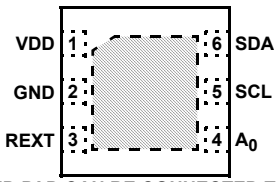
- Low Power
  - 65µA Max Operating Current
  - 0.5µA Max Shutdown Current
  - Software Shutdown and Automatic Shutdown
- Ideal Spectral Response
  - Close to Human Eye Response
  - Excellent IR and UV Rejection
- Easy to Use
  - Simple Output Code Directly Proportional to lux
  - I^2C (SMBus Compatible) Output
  - No Complex Algorithms Needed
  - Variable Conversion Resolution up to 16-bits
  - Adjustable Sensitivity up to 65 Counts per lux
  - Works Under Various Light Sources, Including Sunlight
  - Selectable Range (via I^2C)
  - Range 1 = 0.015 lux to 1,000 lux
  - Range 2 = 0.06 lux to 4,000 lux
  - Range 3 = 0.24 lux to 16,000 lux
  - Range 4 = 0.96 lux to 64,000 lux
  - Temperature Compensated
  - Integrated 50/60Hz Noise Rejection
- Small Form Factor
  - 2.0mmx2.1mmx0.7mm 6 Ld ODFN Package
- Additional Features
  - I^2C and SMBus Compatible
  - 1.7V to 3.6V Supply for I^2C Interface
  - 2.25V to 3.3V Supply
  - Address Selection Pin
- Pb-Free (RoHS compliant)

Applications

- Display and keypad dimming for:
  - Mobile devices: smart phone, PDA, GPS
  - Computing devices: notebook PC, webpad
  - Consumer devices: LCD-TV, digital picture frame, digital camera
- Industrial and medical light sensing

Pinout

ISL29020
(6 LD ODFN)
TOP VIEW



***EXPOSED PAD CAN BE CONNECTED TO GND OR ELECTRICALLY ISOLATED**

Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply Voltage between V_{DD} and GND 3.6V
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.2V to 3.6V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
REXT, A0 Pin Voltage . . . . . -0.2V to V_{DD}
ESD Rating
Human Body Model 2kV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
6 Ld ODFN	88

Maximum Die Temperature . . . . . +90°C
Storage Temperature . . . . . -40°C to +100°C
Operating Temperature . . . . . -40°C to +85°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{DD} = 3V, T_A = +25°C, R_{EXT} = 500kΩ 1% tolerance, 16-bit ADC operation, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Range		2.25		3.3	V
I_{DD}	Supply Current			55	65	µA
I_{DD1}	Supply Current when Powered Down	Software disabled or auto power-down		0.01	0.5	µA
$V_I{}^2C$	Supply Voltage Range for I^2C Interface		1.7		3.6	V
f_{OSC}	Internal Oscillator Frequency		650	725	800	kHz
t_{int}	ADC Integration/Conversion Time	16-bit ADC data		90		ms
$F_I{}^2C$	I^2C Clock Rate Range			1 to 400		kHz
DATA_0	Count Output When Dark	E = 0 lux, Range 1 (1k lux)		1	5	Counts
DATA_F	Full Scale ADC Code				65535	Counts
$\frac{\Delta DATA}{DATA}$	Count Output Variation Over Three Light Sources: Fluorescent, Incandescent and Sunlight	Ambient light sensing		±10		%
DATA_1	Light Count Output With LSB of 0.015 lux/count	E = 300 lux, Fluorescent light (Note 1), Ambient light sensing, Range 1 (1k lux)	15000	20000	25000	Counts
DATA_2	Light Count Output With LSB of 0.06 lux/count	E = 300 lux, Fluorescent light (Note 1), Ambient light sensing, Range 2 (4k lux)		5000		Counts
DATA_3	Light Count Output With LSB of 0.24 lux/count	E = 300 lux, Fluorescent light (Note 1), Ambient light sensing, Range 3 (16k lux)		1250		Counts
DATA_4	Light Count Output With LSB of 0.96 lux/count	E = 300 lux, Fluorescent light (Note 1), Ambient light sensing, Range 4 (64k lux)		312		Counts
DATA_IR1	Infrared Count Output	E = 210 lux, Sunlight (Note 2), IR sensing, Range 1	15000	20000	25000	
DATA_IR2	Infrared Count Output	E = 210 lux, Sunlight (Note 2), IR sensing, Range 2		5000		
DATA_IR3	Infrared Count Output	E = 210 lux, Sunlight (Note 2), IR sensing, Range 3		1250		
DATA_IR4	Infrared Count Output	E = 210 lux, Sunlight (Note 2), IR sensing, Range 4		312		
V_{REF}	Voltage of R_{EXT} Pin			0.52		V
V_{IL}	SCL and SDA Input Low Voltage				0.55	V
V_{IH}	SCL and SDA Input High Voltage		1.25			V
I_{SDA}	SDA Current Sinking Capability		4	5		mA

NOTES:

1. 550nm green LED is used in production test. The 550nm LED irradiance is calibrated to produce the same DATA count against an illuminance level of 300 lux fluorscent light.
2. 850nm green LED is used in production test. The 850nm LED irradiance is calibrated to produce the same DATA_IR count against an illuminance level of 210 lux sunlight at sea level.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION	
1	VDD	Positive supply; connect this pin to a 2.25V to 3.3V supply.	
2	GND	Ground pin.	
3	REXT	External resistor pin for ADC reference; connect this pin to ground through a (nominal) 500kΩ resistor.	
4	A_0	Bit 0 of I^2C address; ground or tie this pin to VDD. No floating.	
5	SCL	I^2C serial clock	The I^2C bus lines can be pulled from 1.7V to above V_{DD}, 3.6V max.
6	SDA	I^2C serial data	

Principles of Operation

Photodiodes and ADC

The ISL29020 contains two photodiode arrays which convert light into current. The spectral response for ambient light sensing and IR sensing is shown in Figure 8 in the “Typical Performance Curves” on page 9. After light is converted to current during the light signal process, the current output is converted to digital by a single built-in 16-bit Analog-to-Digital Converter (ADC). An I^2C command reads the ambient light or IR intensity in counts.

The converter is a charge-balancing integrating type 16-bit ADC. The chosen method for conversion is best for converting small current signals in the presence of an AC periodic noise. A 100ms integration time, for instance, highly rejects 50Hz and 60Hz power line noise simultaneously. See “Integration Time or Conversion Time” on page 6 and “Noise Rejection” on page 7.

The built-in ADC offers user flexibility in integration time or conversion time. There are two timing modes: Internal Timing Mode and External Timing Mode. In Internal Timing Mode, integration time is determined by an internal oscillator (f_{OSC}), and the n-bit (n = 4, 8, 12,16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive I^2C External Timing Mode commands. See “External Timing Mode” on page 6. A good balancing act of integration time and resolution depending on the application is required for optimal results.

The ADC has I^2C programmable ranges to dynamically accommodate various lighting conditions. For very dim conditions, the ADC can be configured at its lower range (Range 1). For bright conditions, the ADC can be configured at its higher range (Range 2).

I^2C Interface

There are three 8-bit registers available inside the ISL29020. The command register defines the operation of the device. The command register does not change until the register is overwritten. The two data registers are Read-Only for 16-bit ADC output or timer output. The data registers contain the ADC's or timer’s latest digital output.

The ISL29020’s I^2C interface slave address can be selected as 1000100 or 1000101 by connecting A0 pin to GND or VDD, respectively. When 1000100x or 1000101x with x as R or $\overline{W}$ is sent after the Start condition, this device compares the first seven bits of this byte to its address and matches.

Figure 1 shows a sample one-byte read. Figure 2 shows a sample one-byte write. Figure 3 shows a sync_I^2C timing diagram sample for externally controlled integration time. The I^2C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Every I^2C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The following byte is driven by the master, and includes the slave address and read/write bit. The receiving device is responsible for pulling SDA low during the acknowledgement period. Every I^2C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

For more information about the I^2C standard, please consult the Philips® I^2C specification documents.

Low-Power Operation

The ISL29020 initial operation is at the power-down mode after a supply voltage is provided. The data registers contain the default value of 0. When the ISL29020 receives an I^2C command to do a one-time measurement from an I^2C master, it will start light sensing and ADC conversion. It will go to the power-down mode automatically after one conversion is finished and keep the conversion data available for the master to fetch anytime afterwards. The ISL29020 will continuously do light sensing and ADC conversion if it receives an I^2C command of continuous measurement. It will continuously update the data registers with the latest conversion data. It will go to the power-down mode after it receives the I^2C command of power-down.

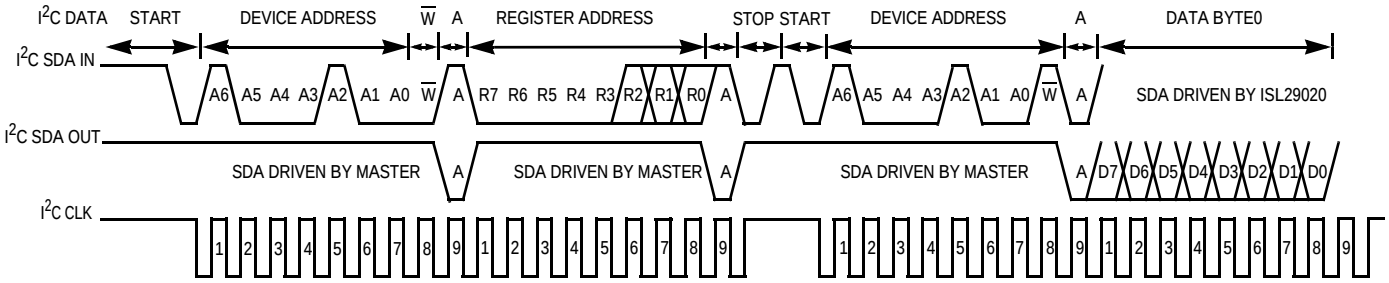


FIGURE 1. I²C READ TIMING DIAGRAM SAMPLE

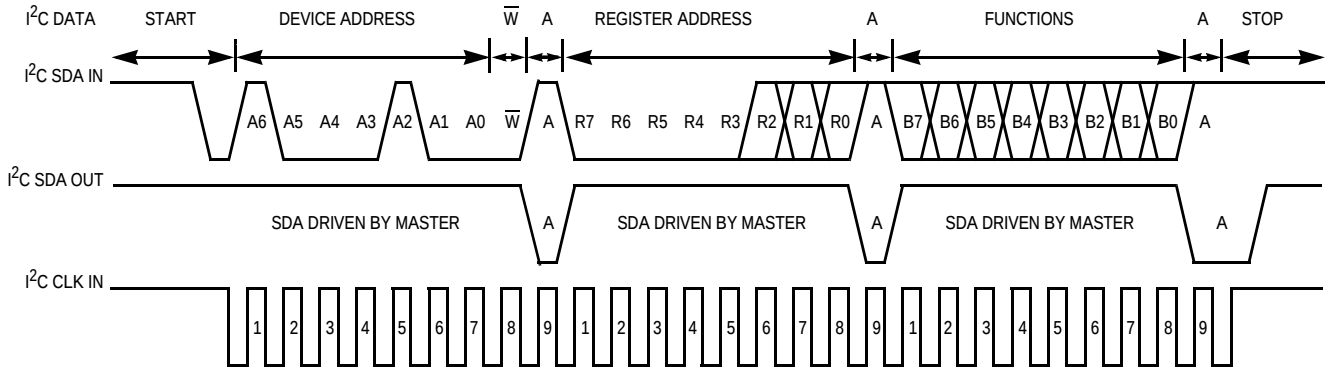


FIGURE 2. I²C WRITE TIMING DIAGRAM SAMPLE

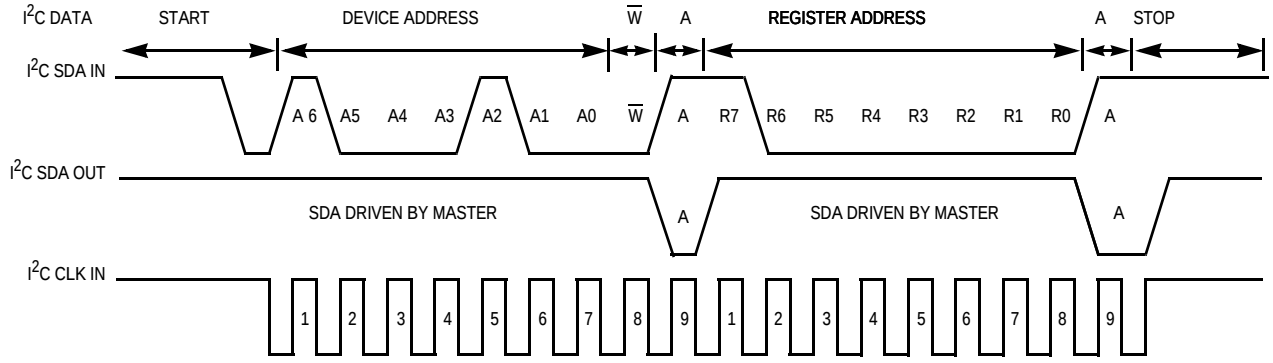


FIGURE 3. I²C SYNC_I²C TIMING DIAGRAM SAMPLE

Register Set

There are three 8-bit registers in the ISL29020. Table 1 summarizes their functions.

TABLE 1. REGISTER SET

ADDR	REG NAME	BIT								DEFAULT
		7	6	5	4	3	2	1	0	
00h	COMMAND	EN	MODE	LIGHT	RES2	RES1	RES0	RANGE1	RANGE0	00h
01h	$DATA_{LSB}$	D7	D6	D5	D4	D3	D2	D1	D0	00h
02h	$DATA_{MSB}$	D15	D14	D13	D12	D11	D10	D9	D8	00h

TABLE 2. WRITE ONLY REGISTERS

ADDRESS	NAME	FUNCTIONS/DESCRIPTION
b1xxx_xxxx	sync_I^2C	Writing a logic 1 to this address bit ends the current ADC-integration and starts another. Used only with External Timing Mode.

Command Register (00 hex)

The Read/Write command register has five functions:

1. Enable: Bit 7. This bit enables the ISL29020 with logic 1 and powers down ISL29020 with logic 0.

TABLE 3. ENABLE

BIT 7	OPERATION
0	Power-down the device
1	Enable the device

2. Measurement Mode: Bit 6. This bit controls the two measurement modes of the device. A logic 0 puts the device in the one-time measurement mode in which the device is automatically shut-down after each measurement. A logic 1 puts the device in the continuous measurement mode in which data is collected continuously.

TABLE 4. MEASUREMENT MODE

BIT 6	OPERATION
0	One-time measurement
1	Continuous measurement

3. Light Sensing: Bit 5. This bit programs the device to do the ambient light or the infrared (IR) light sensing. A logic 0, requests for the ambient light sensing and a logic 1 requests for the IR sensing.

TABLE 5. LIGHT SENSING

BIT 5	OPERATION
0	Ambient light sensing
1	Infrared light sensing

4. Timing Mode and Resolution: Bits 4, 3 and 2. These three bits determine whether the integration time is done internally or externally, and the number of bits for ADC. In Internal Timing Mode, integration time is determined by an internal oscillator (f_{OSC}) and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. In External Timing Mode, the integration time is determined by the time between two consecutive sync_I^2C pulse commands.

TABLE 6. TIMING MODE AND RESOLUTION

BITS 4:3:2	MODE
0:0:0	Internal Timing, 16-bit ADC data output
0:0:1	Internal Timing, 12-bit ADC data output
0:1:0	Internal Timing, 8-bit ADC data output
0:1:1	Internal Timing, 4-bit ADC data output
1:0:0	External Timing, ADC data output
1:0:1	External Timing, Timer data output
1:1:0	Reserved
1:1:1	Reserved

With Bit 4 set to 0, the device is configured to run in the Internal-Timing mode. For example, the command register content should be 1xx000xx to request 16-bit ADC in the internal-timing mode.

With Bit 4 set to 1, the device is configured to run in the External-Timing mode. For the external timing, the command 1xx101xx needs to be sent to request the Timer data, the number of clock cycles counted within the duration between the two sync pulses (refer to Table 2). The Timer count is read from register 01h (LSB) and 02h (MSB). The command 1xx100xx needs to be sent to request the ADC conversion. The ADC data is also read from register 01h (LSB) and 02h (MSB).

Bits 3 and 2 determine the number of clock cycles per conversion in the Internal-Timing mode. Changing the number of clock cycles does more than just change the resolution of the device. It also changes the integration time, which the ADC uses to sample the photodiode current signal for a measurement.

TABLE 7. RESOLUTION/WIDTH

BITS 3:2	NUMBER OF CLOCK CYCLES
0:0	2^{16} = 65,536
0:1	2^{12} = 4,096
1:0	2^{8} = 256
1:1	2^{4} = 16

5. Range: Bits 1 and 0. The Full Scale Range (FSR) can be adjusted via I^2C using Bits 1 and 0. Table 8 lists the possible values of FSR for the 500kΩ R_{EXT} resistor.

TABLE 8. RANGE/FSR LUX

BITS 1:0	k	RANGE(k)	FSR (LUX) @ ALS SENSING	FSR (LUX) @ IR SENSING
0:0	1	Range1	1,000	Refer to page 2
0:1	2	Range2	4,000	Refer to page 2
1:0	3	Range3	16,000	Refer to page 2
1:1	4	Range4	64,000	Refer to page 2

Data Registers (01 hex and 02 hex)

The device has two 8-bit read-only registers to hold a 16-bit data from ADC or Timer. The most significant byte is accessed at 02 hex, and the least significant byte is accessed at 01 hex. The registers are refreshed after every conversion cycle.

TABLE 9. DATA REGISTERS

ADDRESS (hex)	CONTENTS
01	Least-significant byte of most recent ADC or Timer data.
02	Most-significant byte of most recent ADC or Timer data.

Calculating Lux

The ISL29020's ADC output codes, DATA, are directly proportional to lux in the ambient light sensing, as shown in Equation 1.

$$E_{cal} = \alpha \times DATA \quad \text{(EQ. 1)}$$

Here, E_{cal} is the calculated lux reading. The constant α is determined by the Full Scale Range and the ADC's maximum output counts. The constant can also be viewed as the sensitivity: the smallest lux measurement the device can measure, as shown in Equation 2.

$$\alpha = \frac{Range(k)}{Count_{max}} \quad \text{(EQ. 2)}$$

Here, Range(k) is defined in Table 8. $Count_{max}$ is the maximum output counts from the ADC.

The transfer function used for each timing mode becomes:

INTERNAL TIMING MODE

$$E = \frac{Range(k)}{2^n} \times DATA \quad \text{(EQ. 3)}$$

Here, n = 4, 8, 12 or 16. This is the number of ADC bits programmed in the command register. 2^n represents the maximum number of counts possible from the ADC output in Internal-Timing mode. Data is the ADC output stored in the data registers (01 hex and 02 hex).

EXTERNAL TIMING MODE

$$E = \frac{Range(k)}{Timer} \times DATA \quad \text{(EQ. 4)}$$

Here, Timer sets up the ADC's maximum count reading and it is the number of clock cycles accrued in the integration time (set by sync_I^2C pulses) in External-Timing mode. It is stored in the data registers 01h and 02h when the command is coded as 1xx101xx. Data is the ADC output. In this mode, the command has to be sent out again with code 1xx100xx to request the ADC output data from registers 01h and 02h.

External Scaling Resistor R_{EXT} for f_{OSC} and Range

The ISL29020 uses an external resistor R_{EXT} to fix its internal oscillator frequency, f_{OSC} and the light sensing range, Range. f_{OSC} and Range are inversely proportional to R_{EXT}. For user simplicity, the proportionality constant is referenced to 500kΩ:

$$Range = \frac{500k\Omega}{R_{EXT}} \times Range(k) \quad \text{(EQ. 5)}$$

$$f_{OSC} = \frac{500k\Omega}{R_{EXT}} \times 725kHz \quad \text{(EQ. 6)}$$

Integration Time or Conversion Time

Integration time is the period during which the device's analog-to-digital ADC converter samples the photodiode current signal for a measurement. Integration time, in other words, is the time to complete the conversion of analog photodiode current into a digital signal (number of counts).

Integration time affects the measurement resolution. For better resolution, use a longer integration time. For short and fast conversions, use a shorter integration time.

The ISL29020 offers user flexibility in the integration time to balance resolution, speed and noise rejection. Integration time can be set internally or externally by programming the bit 4 of the command register 00(hex).

INTEGRATION TIME IN INTERNAL-TIMING MODE

Most applications will use the Internal-Timing mode. In this mode, f_{OSC} and ADC n-bits resolution determine the integration time, t_{int}, as shown in Equation 7.

$$t_{int} = 2^n \times \frac{1}{f_{OSC}} = 2^n \times \frac{R_{EXT}}{725kHz \times 500k\Omega} \quad \text{(EQ. 7)}$$

where n is the number of bits of resolution and n = 4, 8, 12 or 16. 2^n, therefore, is the number of clock cycles. n can be programmed at the command register 00(hex) bits 3 and 2.

TABLE 10. INTEGRATION TIME OF n-BIT ADC

R_{EXT} (kΩ)	n = 16-BIT	n = 12-BIT	n = 8-BIT	n = 4-BIT
250	50ms	3.2ms	200µs	12.5µs
500**	100ms	6.25ms	390µs	24µs
1000	200ms	12.5ms	782µs	49µs
1500	300ms	18.8ms	1.17ms	73µs
2000	400ms	25ms	1.56ms	98µs

**Recommended R_{EXT} resistor value

INTEGRATION TIME IN EXTERNAL TIMING MODE

The External Timing Mode is recommended when the integration time is needed to synchronize to an external signal, such as a PWM to eliminate noise.

The synchronization can be implemented by using I^2C sync command. The 1st I^2C sync command starts the conversion. The 2nd completes the conversion then starts over again to commence the next conversion. The integration time, t_{int}, is the time interval between the two sync pulses:

$$t_{int} = \frac{Timer}{f_{OSC}} \quad \text{(EQ. 8)}$$

where Timer is the number of internal clock cycles obtained from data registers and f_{OSC} is the internal oscillator frequency.

The internal oscillator, f_{OSC}, operates identically in both the internal and external timing modes. However, in External Timing Mode, the number of clock cycles per integration is no longer fixed at 2^n. The number of clock cycles varies with the chosen integration time, and is limited to 2^{16} = 65,536. In order to avoid erroneous readings the integration time must be short enough not to allow an overflow in the counter register.

$$t_{int} < \frac{65,535}{f_{OSC}} \quad \text{(EQ. 9)}$$

Noise Rejection

In general, integrating type ADCs have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms (k = 1,2...k_i) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal, greatly improves the light sensor output signal in the presence of noise.

Optical Design

Flat Window Lens Design

A window lens will surely limit the viewing angle of the ISL29020. The window lens should be placed directly on top of the device. The thickness of the lens should be kept at minimum to minimize loss of power due to reflection and also to minimize loss due to absorption of energy in the plastic material. A thickness of t = 1mm is recommended for a window lens design. The bigger the diameter of the window lens, the wider the viewing angle is of the ISL29020. Table 11 shows the recommended dimensions of the optical window to ensure both 35° and 45° viewing angle. These dimensions are based on a window lens thickness of 1.0mm and a refractive index of 1.59.

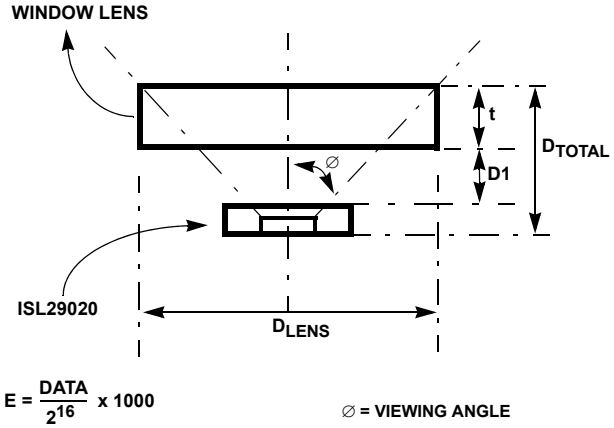


FIGURE 4. FLAT WINDOW LENS

TABLE 11. RECOMMENDED DIMENSIONS FOR A FLAT WINDOW DESIGN

D_{TOTAL}	D1	D_{LENS} @ 35° VIEWING ANGLE	D_{LENS} @ 45° VIEWING ANGLE
1.5	0.50	2.25	3.75
2.0	1.00	3.00	4.75
2.5	1.50	3.75	5.75
3.0	2.00	4.30	6.75
3.5	2.50	5.00	7.75

t = 1	Thickness of lens
D1	Distance between ISL29020 and inner edge of lens
D_{LENS}	Diameter of lens
D_{TOTAL}	Distance constraint between the ISL29020 and lens outer edge

* All dimensions are in mm.

Window with Light Guide Design

If a smaller window is desired while maintaining a wide effective viewing angle of the ISL29020, a cylindrical piece of transparent plastic is needed to trap the light and then focus and guide the light onto the device. Hence, the name light guide or also known as light pipe. The pipe should be placed directly on top of the device with a distance of D1 = 0.5mm to achieve peak performance. The light pipe should have minimum of 1.5mm in diameter to ensure that whole area of the sensor will be exposed. See Figure 5.

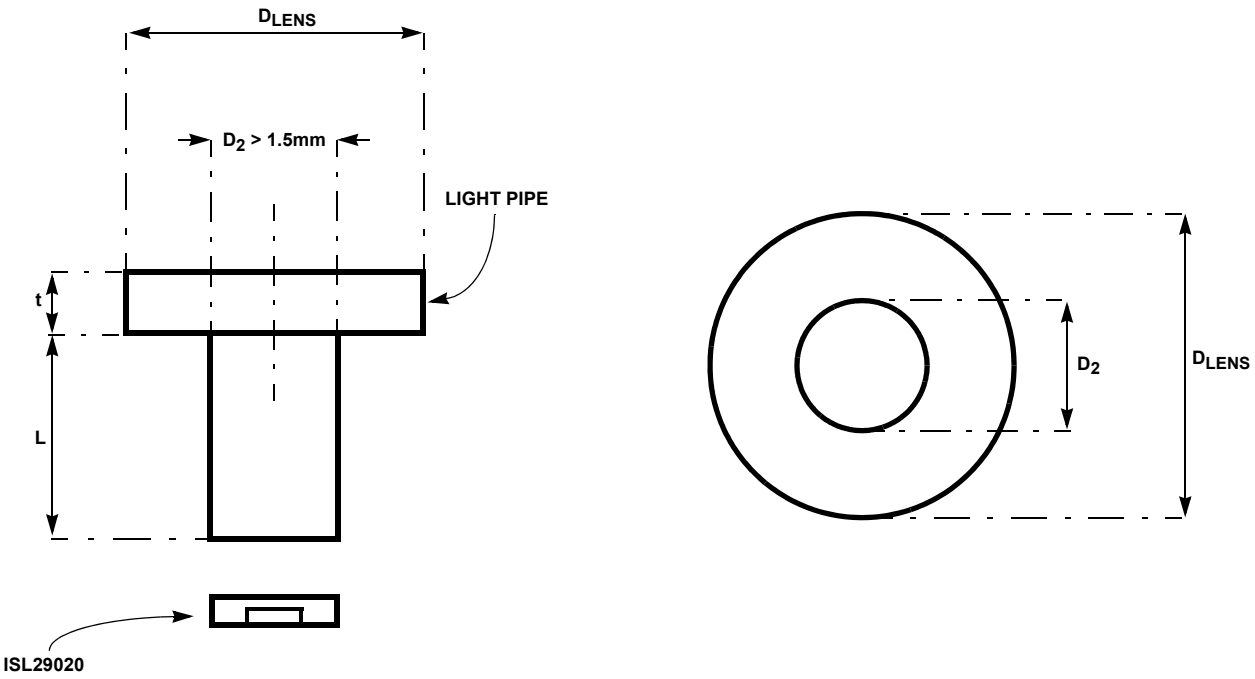


FIGURE 5. WINDOW WITH LIGHT GUIDE/PIPE

Suggested PCB Footprint

It is important that the users check the “Surface Mount Assembly Guidelines for Optical Dual FlatPack No Lead (ODFN) Package” before starting ODFN product board mounting.

http://www.intersil.com/data/tb/TB477.pdf

Layout Considerations

The ISL29020 is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use one 0.01µF power-supply decoupling capacitor, placed close to the device.

Typical Circuit

A typical application for the ISL29020 is shown in Figure 6. The ISL29020’s I^2C address is hardwired as 1000100. The device can be tied onto a system’s I^2C bus together with other I^2C compliant devices.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

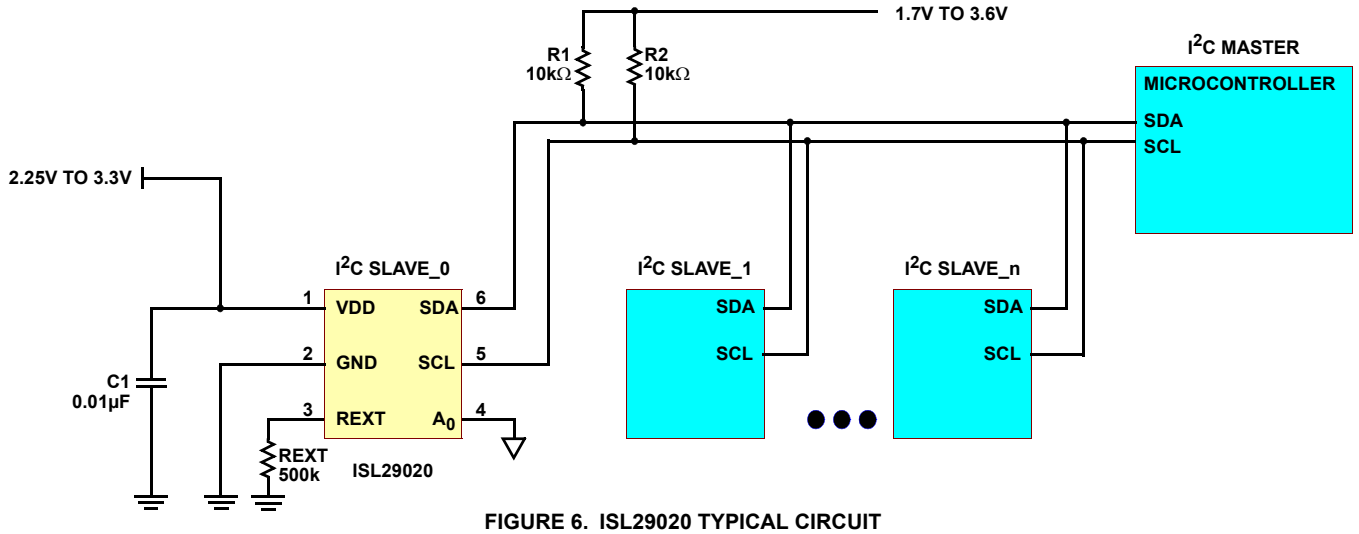


FIGURE 6. ISL29020 TYPICAL CIRCUIT

Typical Performance Curves (V_{DD} = 3V, R_{EXT} = 500kΩ)

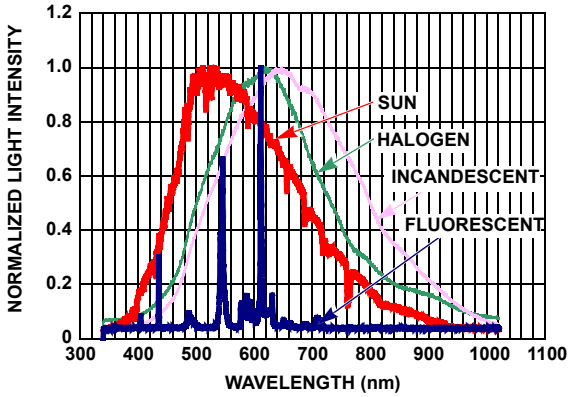


FIGURE 7. SPECTRAL RESPONSE OF LIGHT SOURCES

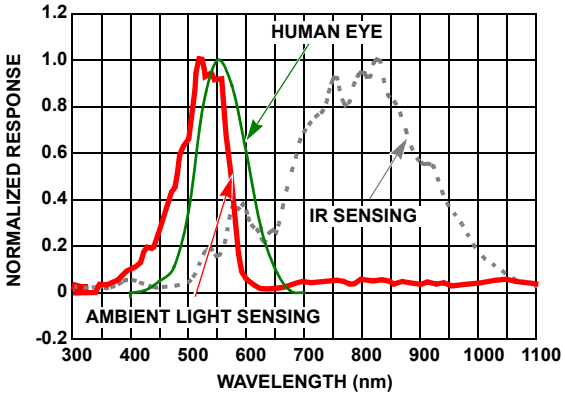


FIGURE 8. SPECTRAL RESPONSE FOR AMBIENT LIGHT SENSING AND IR SENSING

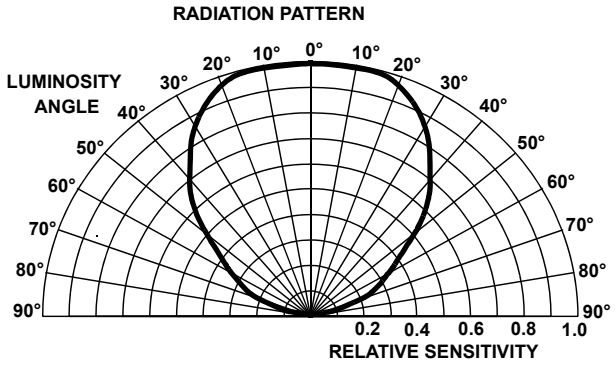


FIGURE 9. RADIATION PATTERN

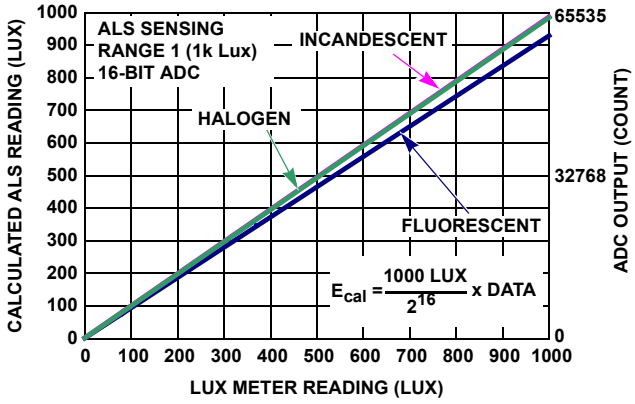


FIGURE 10. SENSITIVITY TO THREE LIGHT SOURCES

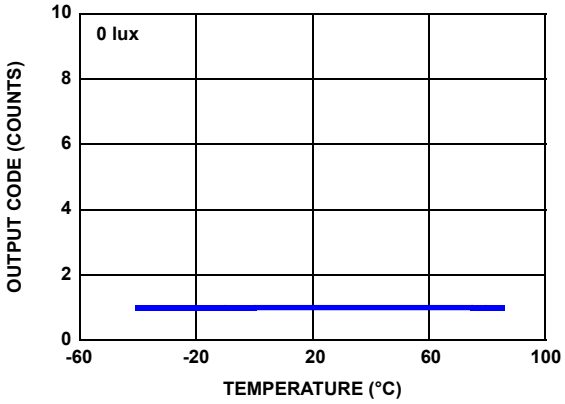


FIGURE 11. OUTPUT CODE FOR 0 LUX vs TEMPERATURE

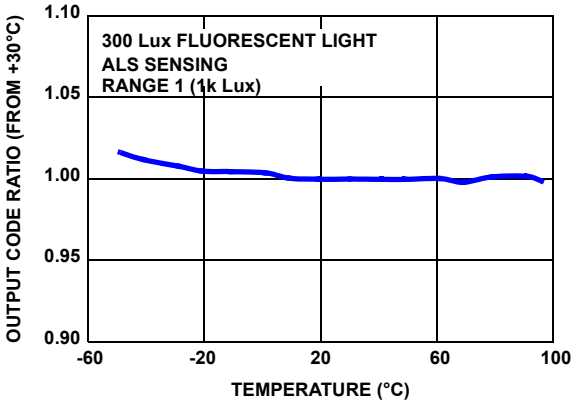


FIGURE 12. OUTPUT CODE vs TEMPERATURE

Typical Performance Curves (V_{DD} = 3V, R_{EXT} = 500kΩ) **(Continued)**

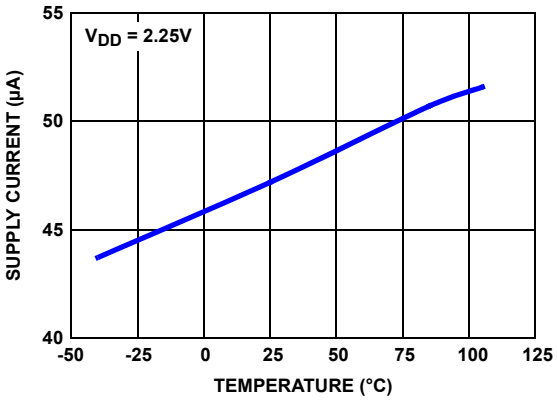


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

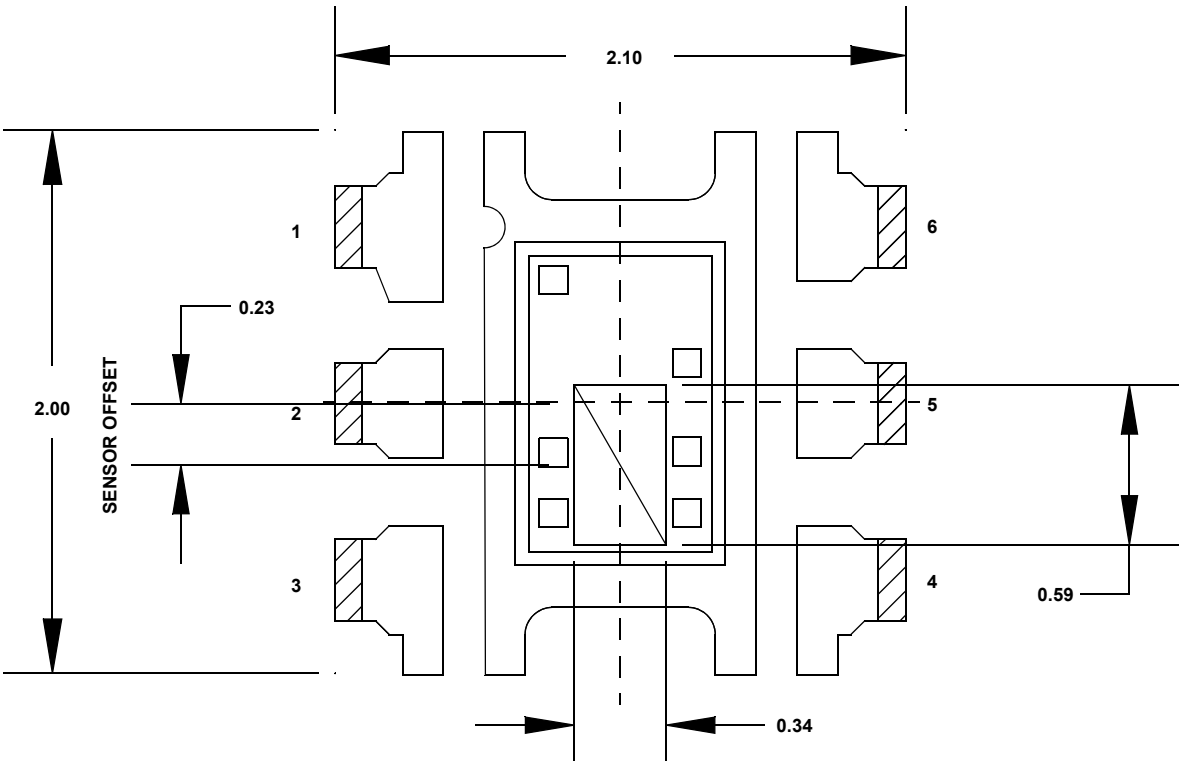
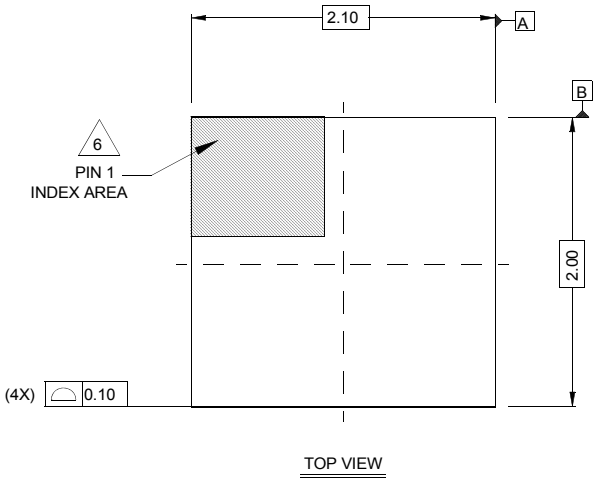


FIGURE 14. SENSOR LOCATION OUTLINE

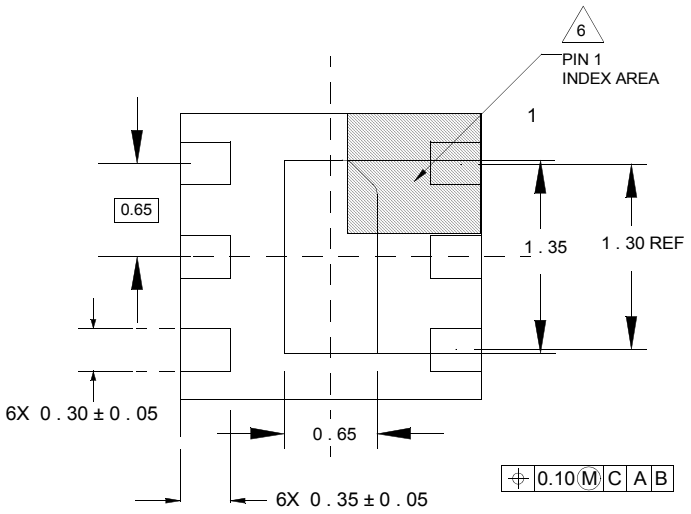
Package Outline Drawing

L6.2x2.1

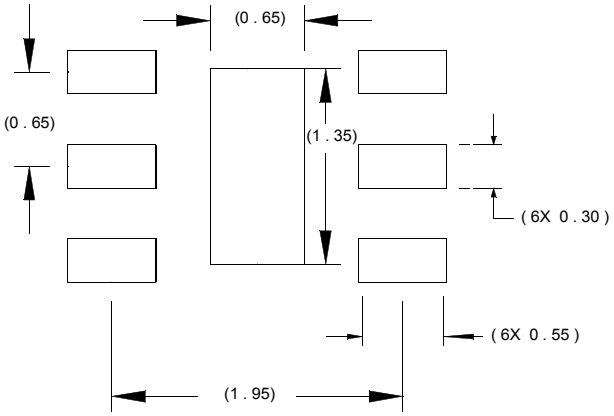
6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)
Rev 0, 9/06



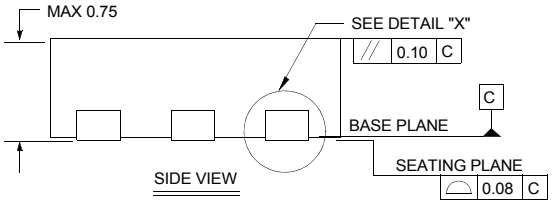
TOP VIEW



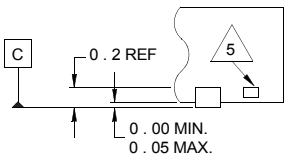
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.