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November 2013

# FQD7N20L

# N-Channel QFET® MOSFET

200 V, 5.5 A, 750 mΩ

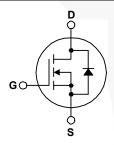
# **Description**

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power • 100% Avalanche Tested factor correction (PFC), and electronic lamp ballasts.

### **Features**

- 5.5 A, 200 V,  $R_{DS(on)}$  = 750 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D = 2.75 A$
- Low Gate Charge (Typ. 6.8 nC)
- Low Crss (Typ. 8.5 pF)
- RoHS Compliant
- · Low Level Gate Drive Requirement Allowing Direct Operating from Logic Drivers





# Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FQD7N20LTM	Unit	
V <sub>DSS</sub>	Drain-Source Voltage	200	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)	5.5	Α	
	- Continuous (T <sub>C</sub> = 100°C)	3.48	Α	
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	22	А	
V <sub>GSS</sub>	Gate-Source Voltage	± 20	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	73	mJ	
I <sub>AR</sub>	Avalanche Current (Note 1)	5.5	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	4.5	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns	
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *	2.5	W	
	Power Dissipation (T <sub>C</sub> = 25°C)	45	W	
	- Derate above 25°C	0.36	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C	
T <sub>L</sub>	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	°C	

### Thermal Characteristics

Symbol	Parameter	FQD7N20LTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. 2.78		
	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD7N20LTM	FQD7N20L	DPAK	Tape and Reel	330 mm	16 mm	2500 units

# **Flectrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Uni
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	200			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		0.17		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			1	μΑ
		V <sub>DS</sub> = 160 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.0		2.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.75 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 2.75 \text{ A}$		0.59 0.62	0.75 0.78	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 2.75 A		5.6		S
Dynam	ic Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		390	500	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		55	70	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			8.5	11	pF
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 6.5 A,		12	35	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25 \Omega$		125	260	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	(Note 4)		20	50	ns
t <sub>f</sub>	Turn-Off Fall Time			65	140	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 160 V, I <sub>D</sub> = 6.5 A,		6.8	9.0	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{GS} = 5 V$ (Note 4)		1.6		nC
Q <sub>gd</sub>	Gate-Drain Charge			3.4		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				5.5	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				22	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 5.5 \text{ A}$			1.5	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } I_{S} = 6.5 \text{ A,}$ $dI_{F} / dt = 100 \text{ A/}\mu\text{s}$		110		ns
Q <sub>rr</sub>	Reverse Recovery Charge			0.44		μС

**Notes:** 1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 3.6 mH, I $_{AS}$  = 5.5 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C. 3. I $_{SD}$  ≤ 6.5 A, di/dt ≤ 300 A/ $\mu$ s, V $_{DD}$  ≤ BV $_{DSS}$ , starting T $_{J}$  = 25°C. 4. Essentially independent of operating temperature.

# **Typical Characteristics**

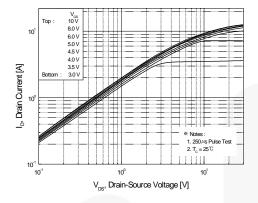


Figure 1. On-Region Characteristics

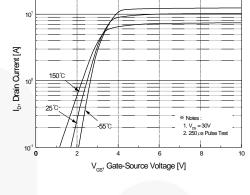


Figure 2. Transfer Characteristics

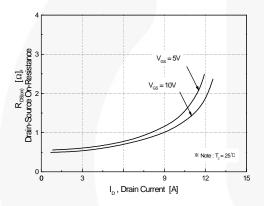


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

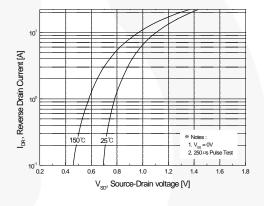


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

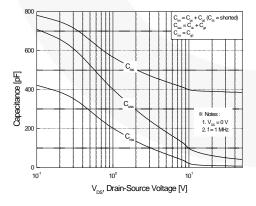


Figure 5. Capacitance Characteristics

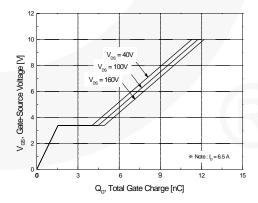


Figure 6. Gate Charge Characteristics

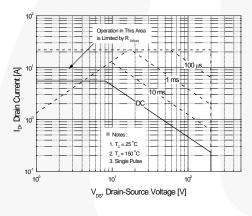
# 1.2 (Nomelized) 1.0 (See ov. 1.1 (Nomelized) 1.0 (See ov. 1.1 (Nomelized) 1.2 (Nomelized) 1.3 (Nomelized) 1.4 (Nomelized) 1.5 (Nomelized) 1.6 (Nomelized) 1.7 (Nomelized) 1.8 (Notes: 1.1 (Nomelized) 1.9 (Notes: 1.1 (Nomelized) 1.0 (No

Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

T<sub>J</sub>, Junction Temperature [°C]

Figure 8. On-Resistance Variation vs. Temperature



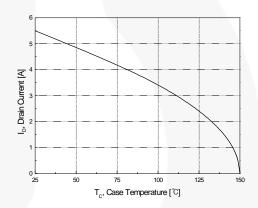


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

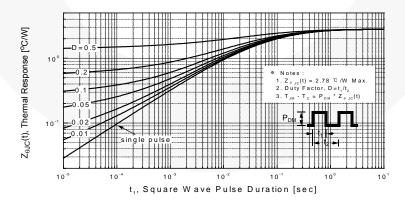


Figure 11. Transient Thermal Response Curve

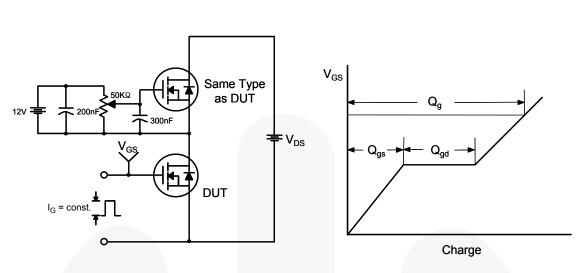


Figure 12. Gate Charge Test Circuit & Waveform

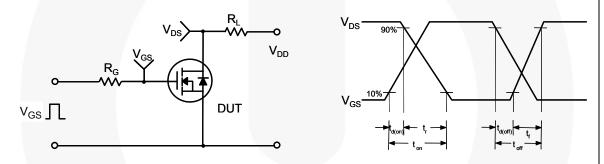


Figure 13. Resistive Switching Test Circuit & Waveforms

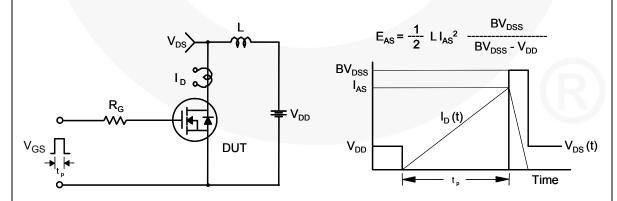
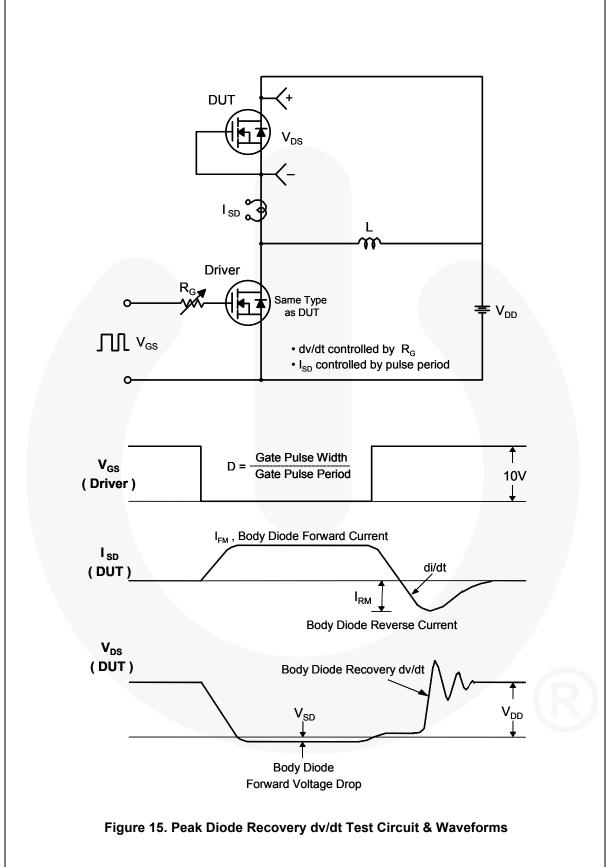


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



## **Mechanical Dimensions**

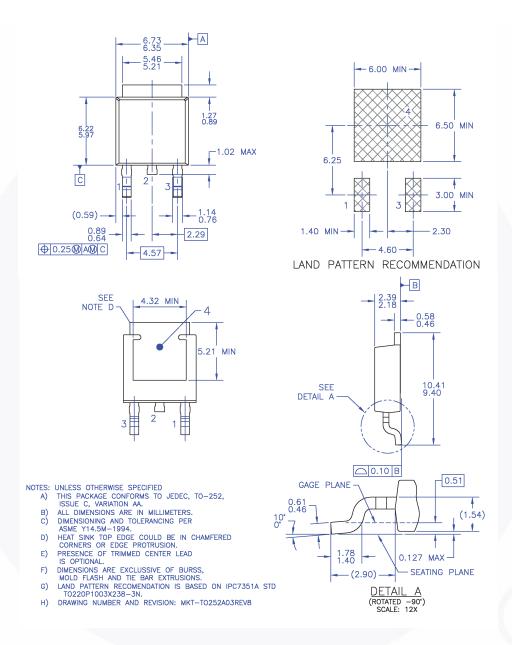


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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