CD74HC4017-Q1
HIGH-SPEED CMOS LOGIC DECADE COUNTER/DIVIDER
WITH 10 DECODED OUTPUTS

- **Qualified for Automotive Applications**
- **Fully Static Operation**
- **Buffered Inputs**
- **Common Reset**
- **Positive Edge Clocking**
- **Typical f_{MAX} = 60 MHz at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 2 V to 6 V**
- **High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V**

M OR PW PACKAGE
(TOP VIEW)

```
        ┌───⌣───┐
   5 [ 1      16 ] V_CC
   1 [ 2      15 ] MR
   0 [ 3      14 ] CP
   2 [ 4      13 ] CE
   6 [ 5      12 ] TC
   7 [ 6      11 ] 9
   3 [ 7      10 ] 4
 GND [ 8       9 ] 8
        └───────┘
```
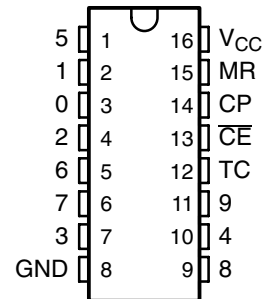
description/ordering information

The CD74HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each of the decoded outputs normally is low and sequentially goes high on the low-to-high transition clock period of the ten-clock-period cycle. The carry (TC) output transitions low to high after output 9 goes from high to low, and can be used in conjunction with the clock enable ($\overline{CE}$) input to cascade several stages. $\overline{CE}$ disables counting when in the high state. A master reset (MR) input also is provided that, when taken high, sets all the decoded outputs, except output 0, to low.

The device can drive up to ten low-power Schottky equivalent loads.

ORDERING INFORMATION[†]

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC – M	Tape and reel	CD74HC4017QM96Q1	HC4017Q
	TSSOP – PW	Tape and reel	CD74HC4017QPWRQ1	HC4017Q

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

FUNCTION TABLE

INPUTS			OUTPUT STATE[†]
CP	$\overline{CE}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H, 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

NOTE: H = high voltage level, L = low voltage level, X = don't care, ↑ = transition from low to high level, ↓ = transition from high to low level

[†] If n < 5, TC = H, otherwise TC = L

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TEXAS INSTRUMENTS

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... –0.5 V to 7 V

Input clamp current, I_{IK} (V_I < –0.5 V or V_I > V_{CC} + 0.5 V) .... ±20 mA

Output clamp current, I_{OK} (V_O < –0.5 V or V_O > V_{CC} + 0.5 V) .... ±20 mA

Source or sink current per output pin, I_O (V_O > –0.5 V or V_O < V_{CC} + 0.5 V) .... ±25 mA

Continuous current through V_{CC} or GND .... ±50 mA

Package thermal impedance, θ_{JA} (see Note 2): M package .... 73°C/W

PW package .... 108°C/W

Maximum junction temperature, T_J .... 150°C

Lead temperature (during soldering):

    At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max .... 300°C

Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
           2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
T_A	Operating free-air temperature		−40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	$T_A = 25°C$		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	−0.02	2 V	1.9		1.9		V
			−0.02	4.5 V	4.4		4.4		
			−0.02	6 V	5.9		5.9		
		TTL loads	−4	4.5 V	3.98		3.7		
			−5.2	6 V	5.48		5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V		0.1		0.1	V
			0.02	4.5 V		0.1		0.1	
			0.02	6 V		0.1		0.1	
		TTL loads	4	4.5 V		0.26		0.4	
			5.2	6 V		0.26		0.4	
I_I	$V_I = V_{CC}$ or GND			6 V		±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V		8		160	μA
C_{IN}	$C_L = 50$ pF					10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			V_{CC}	$T_A = 25°C$		MIN MAX	UNIT
				MIN	MAX		
f_{max}	Maximum clock frequency		2 V	6		4	MHz
			4.5 V	30		20	
			6 V	35		23	
t_w	Pulse duration	CP	2 V	80		120	ns
			4.5 V	16		24	
			6 V	14		20	
		MR	2 V	80		120	
			4.5 V	16		24	
			6 V	14		20	
t_{su}	Setup time	$\overline{CE}$ to CP	2 V	75		110	ns
			4.5 V	15		22	
			6 V	13		19	
		MR inactive	2 V	5		5	
			4.5 V	5		5	
			6 V	5		5	
t_h	Hold time, $\overline{CE}$ to CP		2 V	0		0	ns
			4.5 V	0		0	
			6 V	0		0	

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INSTRUMENTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	MIN	MAX	UNIT
t_{pd}	CP	Decade out	$C_L = 50$ pF	2 V			230		345	ns
				4.5 V			46		69	
				6 V			39		59	
			$C_L = 15$ pF	5 V		19				
		TC	$C_L = 50$ pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			$C_L = 15$ pF	5 V		19				
	$\overline{CE}$	Decade out	$C_L = 50$ pF	2 V			250		375	
				4.5 V			50		75	
				6 V			43		64	
			$C_L = 15$ pF	5 V		21				
		TC	$C_L = 50$ pF	2 V			250		375	
				4.5 V			50		75	
				6 V			43		64	
			$C_L = 15$ pF	5 V		21				
	MR	Decade out	$C_L = 50$ pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			$C_L = 15$ pF	5 V		19				
		TC	$C_L = 50$ pF	2 V			230		345	
				4.5 V			46		69	
				6 V			39		59	
			$C_L = 15$ pF	5 V		19				
t_t		TC, Decade out	$C_L = 50$ pF	2 V		75			110	ns
				4.5 V		15			22	
				6 V		13			19	
f_{max}	CP		$C_L = 15$ pF	5 V		60				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns, C_L = 15 pF

PARAMETER	TYP	UNIT
C_{pd} Power dissipation capacitance (see Note 4)	39	pF

NOTE 4: C_{pd} is used to determine the dynamic power consumption per package.

$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_O)$

f_I = input frequency
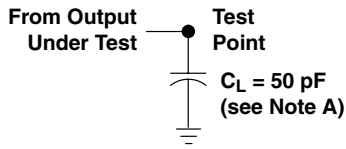f_O = output frequency
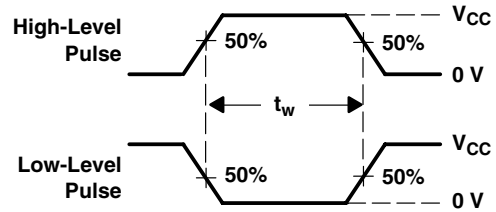C_L = output load capacitance
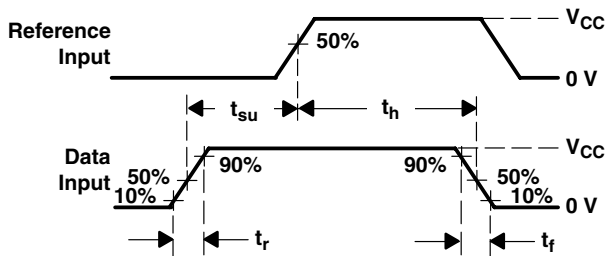V_{CC} = supply voltage

TEXAS INSTRUMENTS
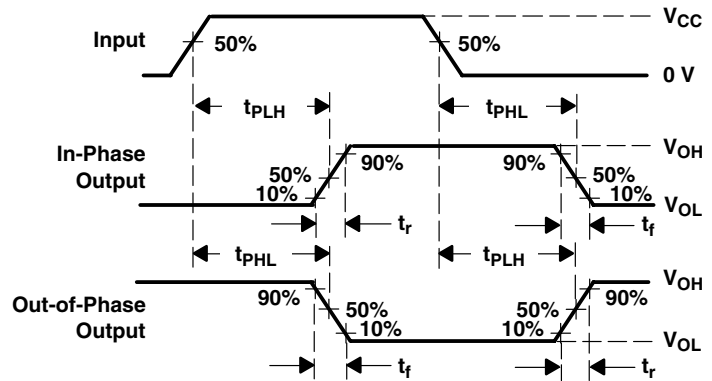
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**

NOTES: A. C_L includes probe and test-fixture capacitance.
     B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
     C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
     D. The outputs are measured one at a time with one input transition per measurement.
     E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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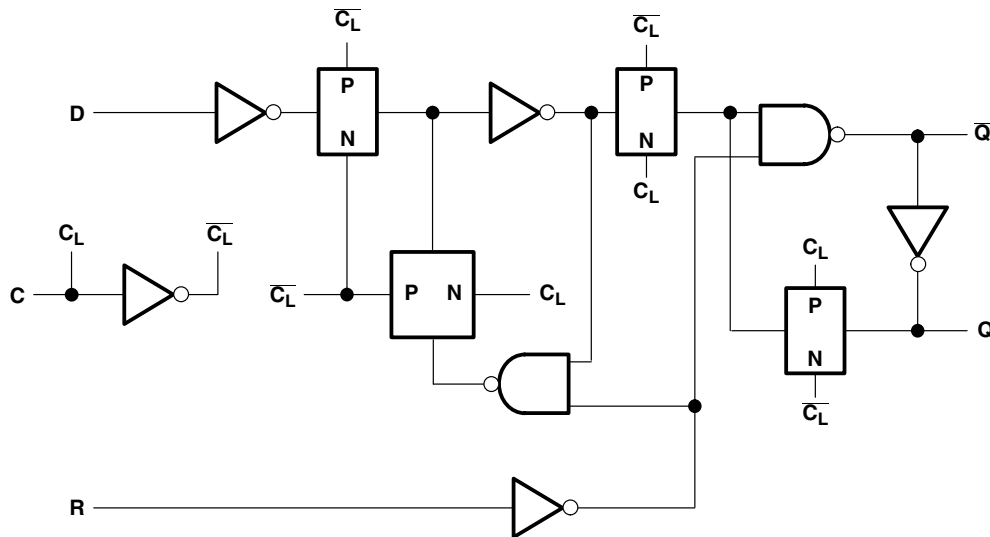
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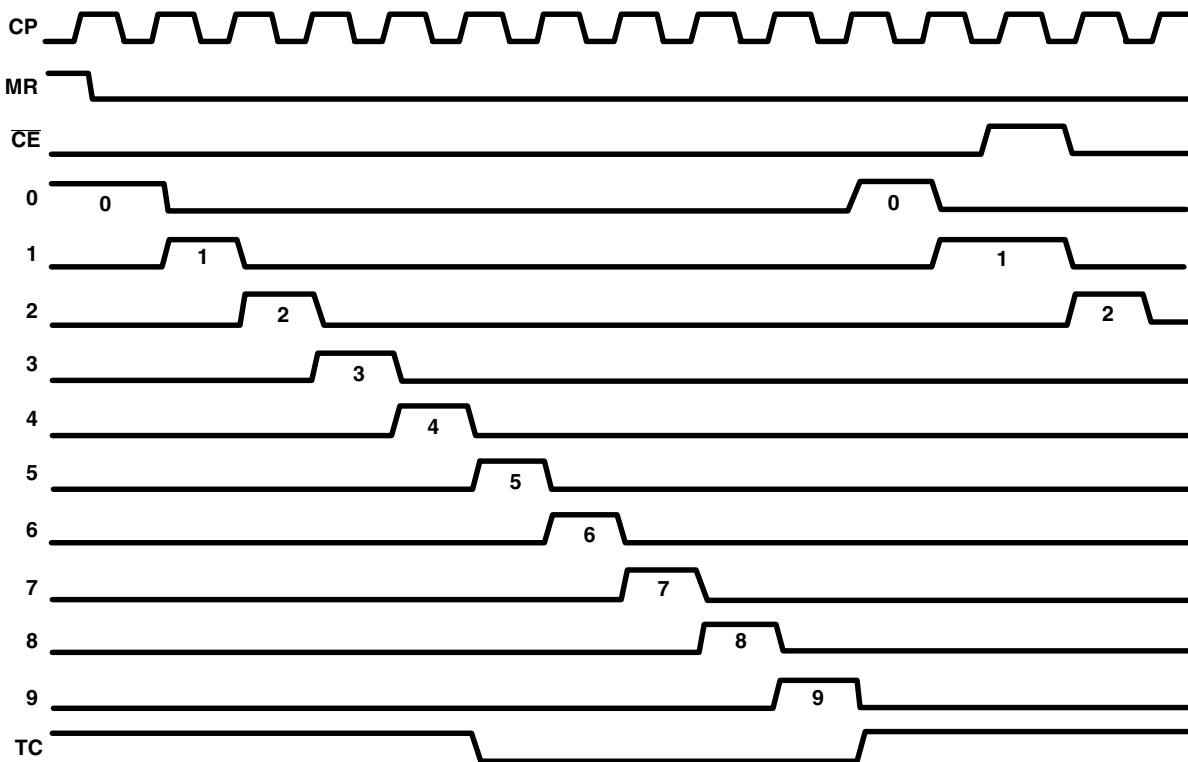
Figure 2. Flip-Flop Detail

Figure 3. Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4017QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4017Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD74HC4017-Q1 :

● Catalog: CD74HC4017

● Enhanced Product: CD74HC4017-EP

● Military: CD54HC4017

NOTE: Qualified Version Definitions:

  ● Catalog - TI's standard catalog product

  ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

  ● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4017QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4017QPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM
₵

1

16X (0.45)

(R0.05) TYP

16

SYMM
₵

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

16X (1.5)
SYMM
(R0.05) TYP
1
16X (0.45)
16
SYMM
14X (0.65)
8
9
(5.8)

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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