# LVPECL AND LVDS REPEATER/TRANSLATOR WITH ENABLE

## FEATURES

- **Low-Voltage PECL Input and Low-Voltage PECL or LVDS Outputs**
- **Signaling Rates to 4 Gbps or Clock Rates to 2 GHz**
  - **120-ps Output Transition Times**
  - **Less than 45 ps Total Jitter**
  - **Less than 630 ps Propagation Delay Times**

- **2.5-V or 3.3-V Supply Operation**
- **2-mm x 2-mm Small-Outline No-Lead Package**

## APPLICATIONS

- **PECL-to-LVDS Translation**
- **Data or Clock Signal Amplification**

## DESCRIPTION

The SN65LVDS20 and SN65LVP20 are a high-speed differential receiver and driver connected as a repeater. The receiver accepts low-voltage positive-emitter-coupled logic (PECL) at signaling rates up to 4 Gbps and repeats it as either an LVDS or PECL output signal. The signal path through the device is differential for low radiated emissions and minimal added jitter.

The outputs of the SN65LVDS20 are LVDS levels as defined by TIA/EIA-644-A. The outputs of the SN65LVDP20 are compatible with low-voltage PECL levels. A low-level input to $\overline{EN}$ enables the outputs. A high-level input puts the output into a high-impedance state. Both outputs are designed to drive differential transmission lines with nominally 100-$\Omega$ characteristic impedance.

Both devices provide a voltage reference ($V_{BB}$) of typically 1.35 V below $V_{CC}$ for use in receiving single-ended PECL input signals. When not used, $V_{BB}$ should be unconnected or open.

All devices are characterized for operation from -40°C to 85°C.
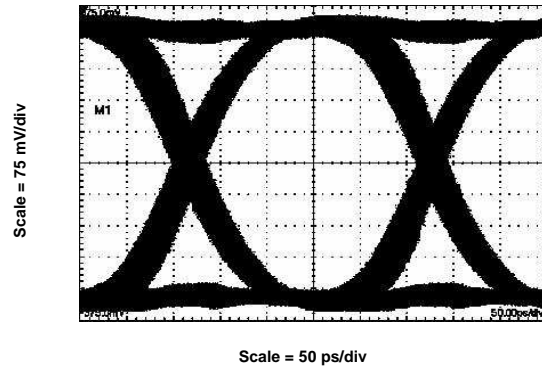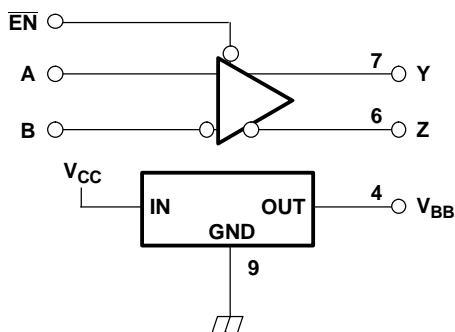
### FUNCTION DIAGRAM





Scale = 50 ps/div

**Figure 1. SN65LVDS20 Output Eye Pattern With 4-Gbps PRBS Input**

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⚠ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS[1]

| INPUT | OUTPUT | PART NUMBER | PART MARKING |
|---|---|---|---|
| Differential | LVDS | SN65LVDS20 | E8 |
| Differential | LVPECL | SN65LVP20 | E7 |

(1)  For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

| | | UNIT |
|---|---|---|
| $V_{CC}$ | Supply voltage [2] | -0.5 V to 4 V |
| $V_I$ | Input voltage | -0.5 V to $V_{CC}$ + 0.5 V |
| $V_O$ | Output voltage | -0.5 V to $V_{CC}$ + 0.5 V |
| $I_O$ | $V_{BB}$ output current | ±0.5 mA |
| | HBM electrostatic discharge[3] | ±3 kV |
| | CDM electrostatic discharge[4] | ±1500 V |
| | Continuous power dissipation | See Power Dissipation Ratings Table |

(1)  Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)  All voltage values, except differential voltages, are with respect to network ground (see Figure 2).
(3)  Tested in accordance with JEDEC Standard 22, Test Method A114-A-7
(4)  Tested in accordance with JEDEC Standard 22, Test Method C101

## DISSIPATION RATINGS

| PACKAGE | $T_A$ < 25°C POWER RATING | OPERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 85°C POWER RATING |
|---|---|---|---|
| DRF | 403 mW | 4.0 mW/°C | 161 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.375 | 2.5 or 3.3 | 3.6 | V |
| $V_{IC}$ | Common-mode input voltage $(V_{IA} + V_{IB})/2$ | 1.2 | | $V_{CC}$ - $(V_{ID}/2)$ | V |
| $|V_{ID}|$ | Differential input voltage magnitude, $|V_{IA} - V_{IB}|$ | 0.08 | | 1 | V |
| $V_{IH}$ | High-level input voltage, $\overline{EN}$ | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage, $\overline{EN}$ | 0 | | 0.8 | V |
| $I_O$ | Output current to $V_{BB}$ | -400[1] | | 400 | μA |
| $R_L$ | Differential load resistance | 90 | | 132 | Ω |
| $T_A$ | Operating free-air temperature | -40 | | 85 | °C |

(1)  The algebraic convention, where the least positive (more negative) value is designated minimum, is used in this data sheet.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | $R_L$ = 100 Ω, $\overline{EN}$ at 0 V, Other inputs open | | 35 | 45 | mA |
| | | Outputs unloaded, $\overline{EN}$ at 0 V, Other inputs open | | 19 | 24 | |
| $P_D$ | Device power dissipation, SN65LVDS20 | $R_L$ = 100 Ω, $\overline{EN}$ at 0 V, 2-GHz 50%-duty-cycle square-wave input | | 116 | 160 | mW |
| | Device power dissipation, SN65LVP20 | 50 Ω from Y and Z to $V_{CC}$ - 2 V, $\overline{EN}$ at 0 V, 2-GHz 50%-duty-cycle square-wave input | | 63 | 86 | |
| $V_{BB}$ | Reference voltage | $I_{BB}$ = ±400 µA | $V_{CC}$ - 1.44 | $V_{CC}$ - 1.35 | $V_{CC}$ - 1.25 | V |
| $I_{IH}$ | High-level input current, $\overline{EN}$ | $V_I$ = 2 V | -20 | | 20 | µA |
| $I_{IAH}$ or $I_{IBH}$ | High-level input current, A or B | $V_I$ = $V_{CC}$ | -20 | | 20 | |
| $I_{IL}$ | Low-level input current, $\overline{EN}$ | $V_I$ = 0.8 V | -20 | | 20 | |
| $I_{IAL}$ or $I_{IBL}$ | Low-level input current, A or B | $V_I$ = GND | -20 | | 20 | |
| **SN65LVDS20 OUTPUT CHARACTERISTICS (see Figure 2)** | | | | | | |
| $|V_{OD}|$ | Differential output voltage magnitude, $|V_{OY}$ - $V_{OZ}|$ | See Figure 2 | 247 | 340 | 454 | mV |
| $\Delta|V_{OD}|$ | Change in differential output voltage magnitude between logic states | | | | 50 | |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage (see Figure 3) | | 1.125 | | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state com-mon-mode output voltage between logic states | See Figure 3 | -50 | | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | 50 | 100 | |
| $I_{OYZ}$ or $I_{OZZ}$ | High-impedance output current | $\overline{EN}$ at $V_{CC}$, $V_O$ = 0 V or $V_{CC}$ | -1 | | 1 | µA |
| $I_{OYS}$ or $I_{OZS}$ | Short-circuit output current | $\overline{EN}$ at 0 V, $V_{OY}$ or $V_{OZ}$ = 0 V | -62 | | 62 | mA |
| $I_{OS(D)}$ | Differential short-circuit output current, $|I_{OY}$ - $I_{OZ}|$ | $\overline{EN}$ at 0 V, $V_{OY}$ = $V_{OZ}$ | -12 | | 12 | |
| **SN65LVP20 OUTPUT CHARACTERISTICS (see Figure 2)** | | | | | | |
| $V_{OYH}$ or $V_{OZH}$ | High-level output voltage | 3.3 V; 50 Ω from Y and Z to $V_{CC}$ - 2 V | $V_{CC}$ - 1.05 | | $V_{CC}$ - 0.82 | V |
| $V_{OYL}$ or $V_{OZL}$ | Low-level output voltage | | $V_{CC}$ - 1.83 | | $V_{CC}$ - 1.57 | |
| $V_{OYL}$ or $V_{OZL}$ | Low-level output voltage | 2.5 V; 50 Ω from Y and Z to $V_{CC}$ - 2 V | $V_{CC}$ - 1.88 | | $V_{CC}$ - 1.57 | |
| $|V_{OD}|$ | Differential output voltage magnitude, $|V_{OH}$ - $V_{OL}|$ | | 0.6 | 0.8 | 1 | |
| $I_{OYZ}$ or $I_{OZZ}$ | High-impedance output current | $\overline{EN}$ at $V_{CC}$, $V_O$ = 0 V or $V_{CC}$ | -1 | | 1 | µA |

(1) Typical values are at room temperature and with a $V_{CC}$ of 3.3 V.

# SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Differential propagation delay time, low-to-high-level output | See Figure 2 and Figure 4 | 300 | 450 | 630 | ps |
| $t_{PHL}$ | Differential propagation delay time, high-level-to-low-level output | | 300 | 450 | 630 | |
| $t_{SK(P)}$ | Pulse skew, $|t_{PLH} - t_{PHL}|$ | | | | 20 | |
| $t_{SK(PP)}$ | Part-to-part skew [2] | $V_{CC}$ = 3.3 V | | | 80 | ps |
| | | $V_{CC}$ = 2.5 V | | | 130 | |
| $t_r$ | 20%-to-80% differential signal rise time | LVDS, See Figure 2 and Figure 4 | | 85 | 115 | ps |
| | | LVPECL, See Figure 2 and Figure 4 | | 92 | 120 | |
| $t_f$ | 20%-to-80% differential signal fall time | LVDS, See Figure 2 and Figure 4 | | 85 | 115 | ps |
| | | LVPECL, See Figure 2 and Figure 4 | | 92 | 120 | |
| $t_{jit(per)}$ | RMS period jitter[3] | 2-GHz 50%-duty-cycle square-wave input, See Figure 5 | | 2 | 3 | ps |
| $t_{jit(cc)}$ | Peak cycle-to-cycle jitter [4] | | | 13 | 16 | |
| $t_{jit(p-p)}$ | Peak-to-peak jitter | LVDS; 4 Gbps PRBS, $2^{23}$- 1 run length, See Figure 5 | | 37 | 45 | ps |
| $t_{jit(ph)}$ | Intrinsic phase jitter | 155.52 MHz | | 0.62 | | ps |
| | | 622.08 MHz | | 0.14 | | |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | See Figure 2 and Figure 6 | | | 30 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | | 30 | |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | | | | 30 | |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | | 30 | |

(1) Typical values are at room temperature and with a $V_{CC}$ of 3.3 V.
(2) Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles, over a random sample of 1,000 adjacent cycle pairs.

## PARAMETER MEASUREMENT INFORMATION
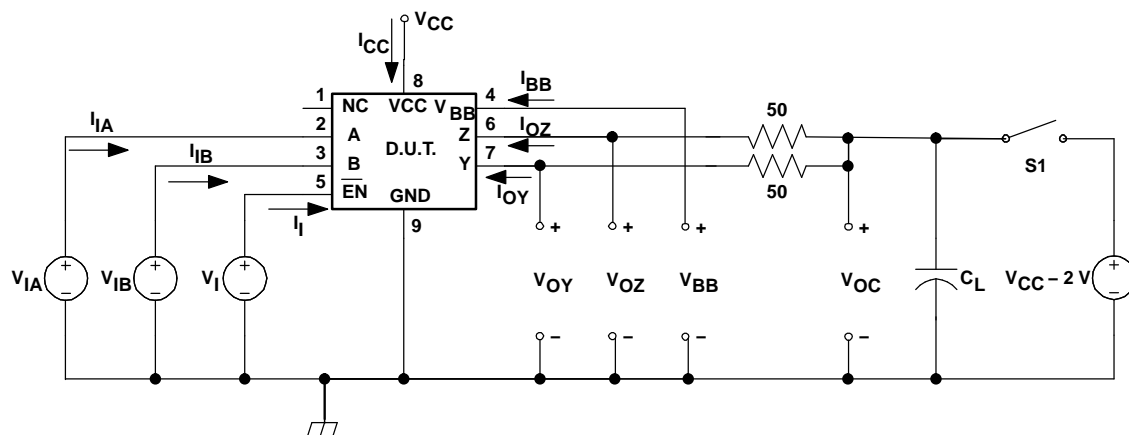


(1) $C_L$ is the instrumentation and test fixture capacitance.
(2) S1 is open for the SN65LVDS20 and closed for the SN65LVP20.

**Figure 2. Output Voltage Test Circuit and Voltage and Current Definitions**

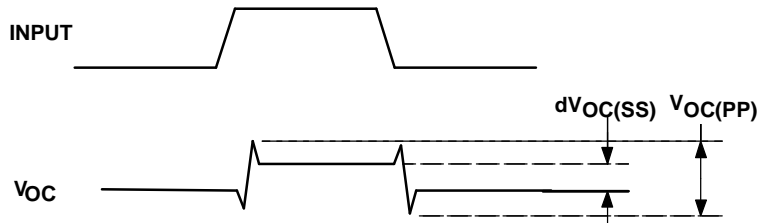## PARAMETER MEASUREMENT INFORMATION (continued)
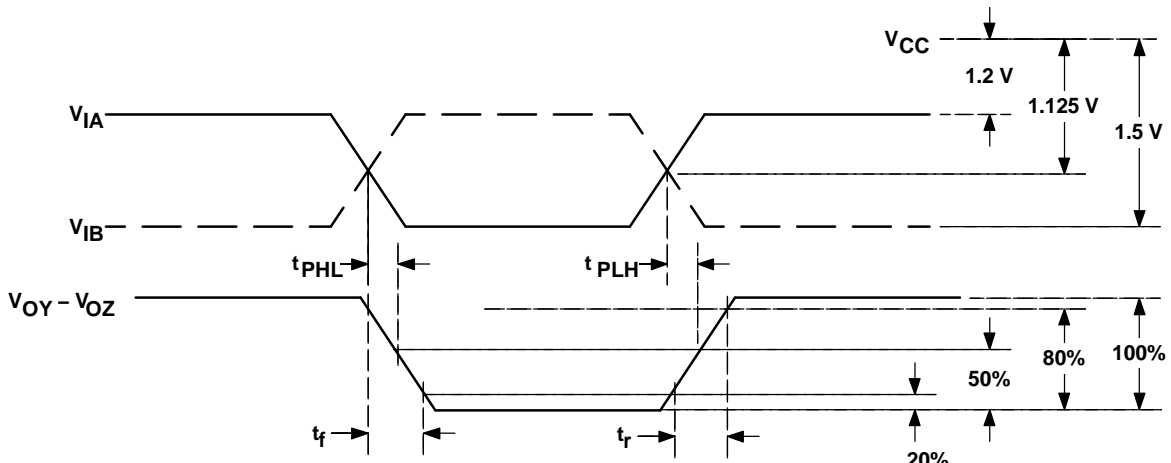


Figure 3. $V_{OC}$ Definitions



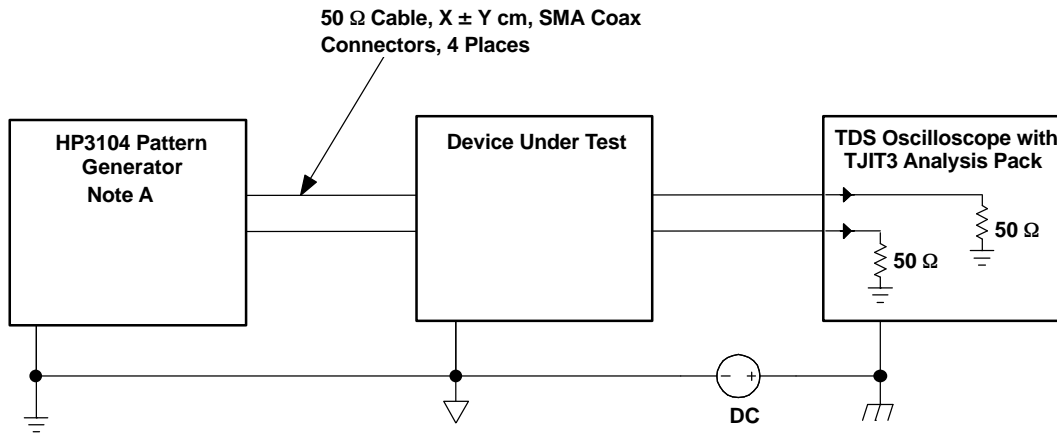Figure 4. Propagation Delay and Transition Time Test Waveforms



Figure 5. Jitter Measurement Setup
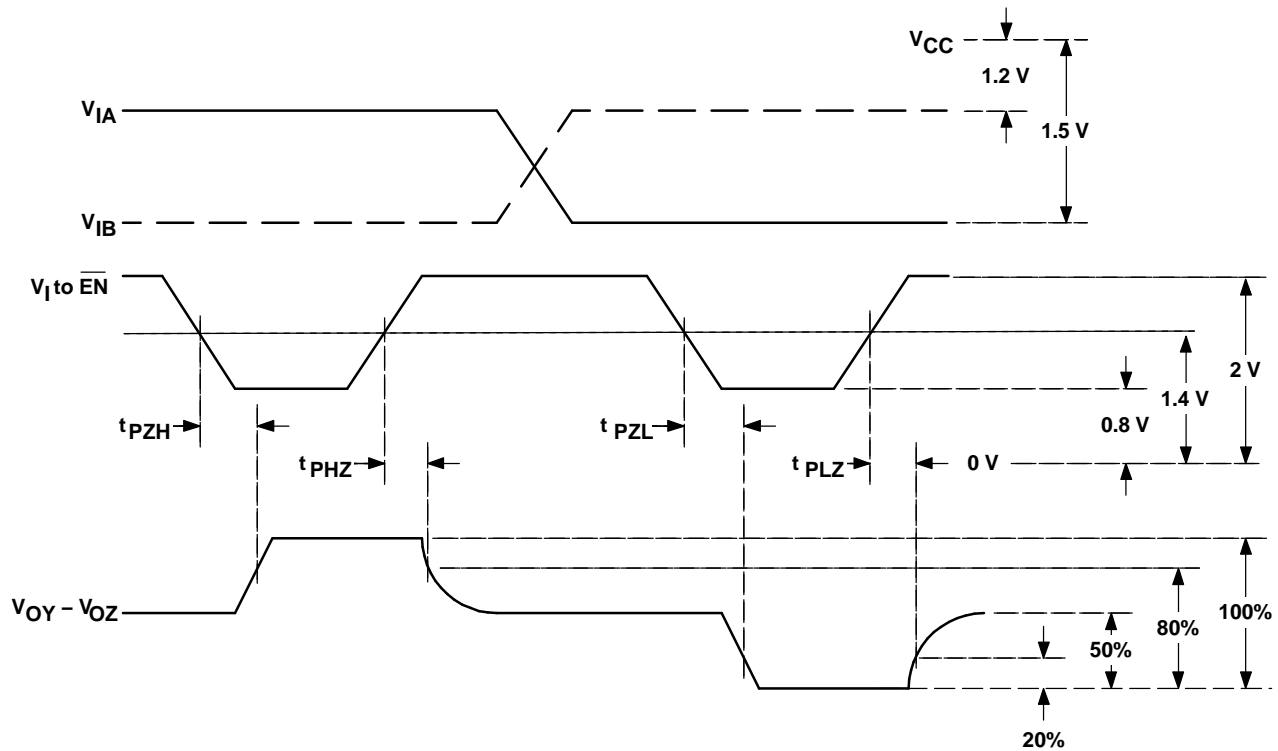
## PARAMETER MEASUREMENT INFORMATION (continued)
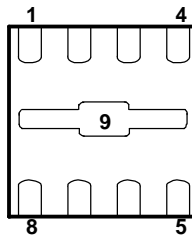


**Figure 6. Enable and Disable Time Test Waveforms**

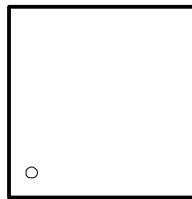## DEVICE INFORMATION

### FUNCTION TABLE[1]

| A | B | $\overline{\text{EN}}$ | Y | Z |
|---|---|---|---|---|
| H | H | L | ? | ? |
| L | H | L | L | H |
| H | L | L | H | L |
| L | L | L | ? | ? |
| X | X | H | Z | Z |
| Open | Open | L | ? | ? |
| X | X | Open | ? | ? |

(1)   H = high, L = low, Z = high
      impedance, ? = indeterminate

**TOP VIEW**

**BOTTOM VIEW**

## Package Pin Assignments - Numerical Listing

| PIN | SIGNAL | PIN | SIGNAL |
|-----|--------|-----|--------|
| 1 | NC | 6 | Z |
| 2 | A | 7 | Y |
| 3 | B | 8 | $V_{CC}$ |
| 4 | $V_{BB}$ | 9 | GND |
| 5 | $\overline{EN}$ | | |

## Package Pin Assignments - Alphabetical Listing

| SIGNAL | PIN | SIGNAL | PIN |
|--------|-----|--------|-----|
| A | 2 | $V_{BB}$ | 4 |
| B | 3 | $V_{CC}$ | 8 |
| $\overline{EN}$ | 5 | Y | 7 |
| GND | 9 | Z | 6 |
| NC | 1 | | |

# TYPICAL CHARACTERISTICS

**SUPPLY CURRENT**
**vs**
**FREQUENCY**



Figure 7.

**SUPPLY CURRENT**
**vs**
**FREE-AIR TEMPERATURE**



Figure 8.

**DIFFERENTIAL OUTPUT VOLTAGE**
**vs**
**FREQUENCY**



Figure 9.

**LVDS20 RISE/FALL TIME**
**vs**
**FREE-AIR TEMPERATURE**



Figure 10.

**LVP20 RISE/FALL TIME**
**vs**
**FREE-AIR TEMPERATURE**



Figure 11.

**LVDS20 PROPAGATION DELAY TIME**
**vs**
**FREE-AIR TEMPERATURE**
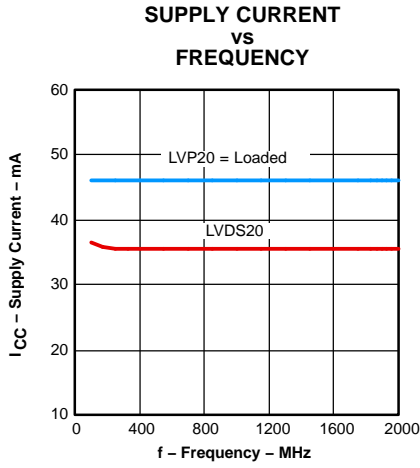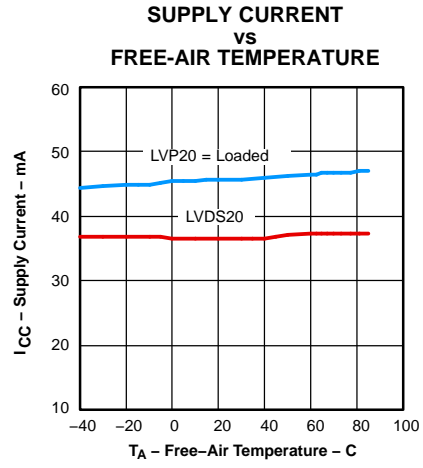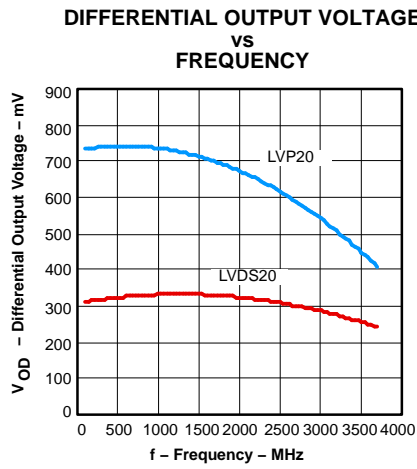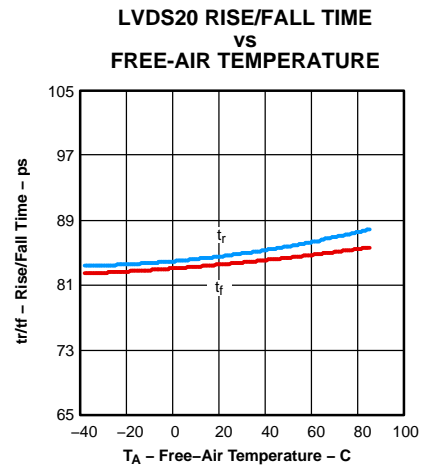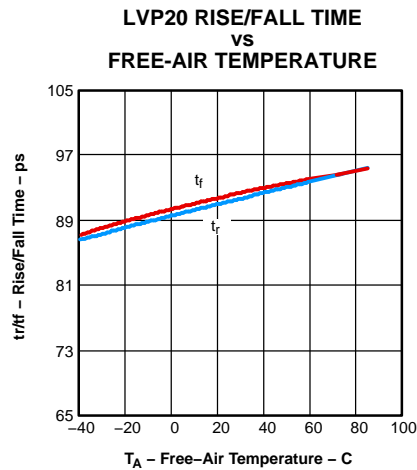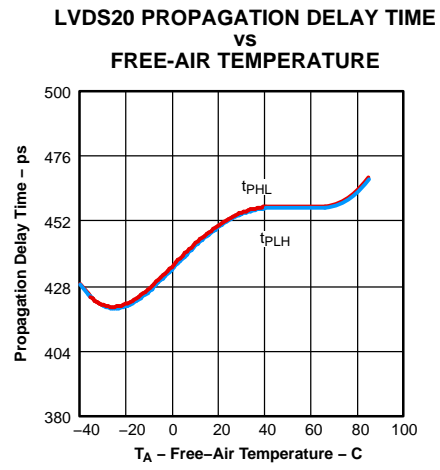


Figure 12.

## TYPICAL CHARACTERISTICS (continued)

**LVP20 PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**



Figure 13.

**PERIOD JITTER
vs
FREQUENCY**



Figure 14.

**PEAK-TO-PEAK JITTER
vs
FREQUENCY**



Figure 15.

**PEAK-TO-PEAK JITTER
vs
DATA RATE**



Figure 16.



Scale = 50 ps/div
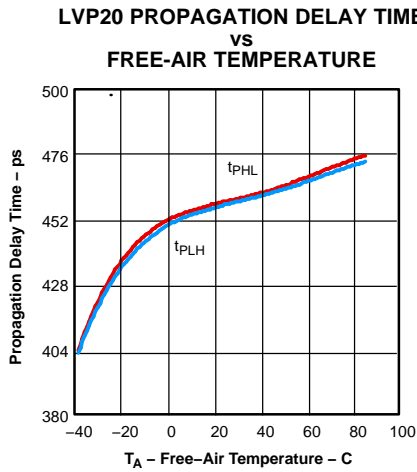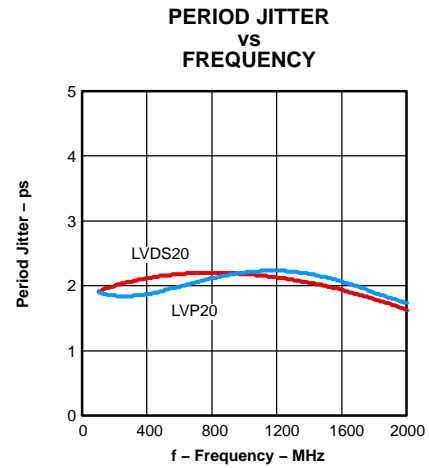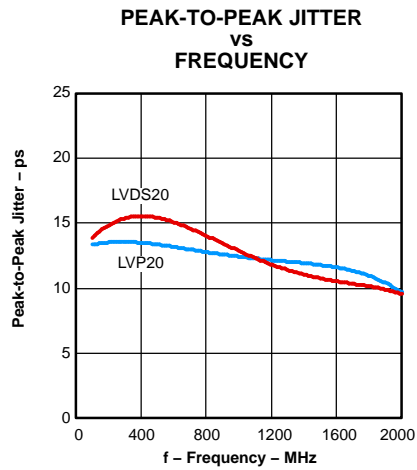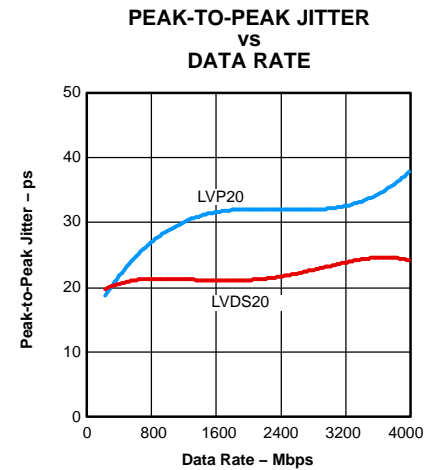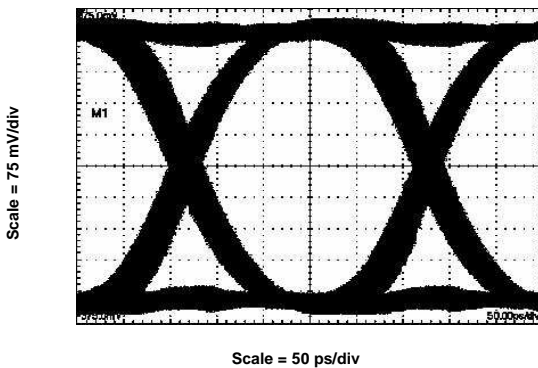
Figure 17. LVDS20 4-Gbps, $2^{23}$ - 1 PRBS



Scale = 50 ps/div

Figure 18. LVP20 4-Gbps, $2^{23}$ - 1 PRBS

## TYPICAL CHARACTERISTICS (continued)

**PHASE NOISE OF SN65LVP20**



Figure 19. Frequency Offset From 155.52 MHz Carrier

**PHASE NOISE OF SN65LVP20**



Figure 20. Frequency Offset From 622.08 MHz Carrier

# EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

**OUTPUT LVP20**

**OUTPUT LVDS20**

**ENABLE**

**INPUT**

**OUTPUT**

## PACKAGING INFORMATION

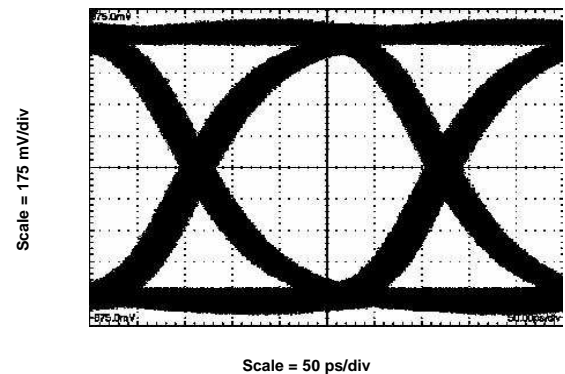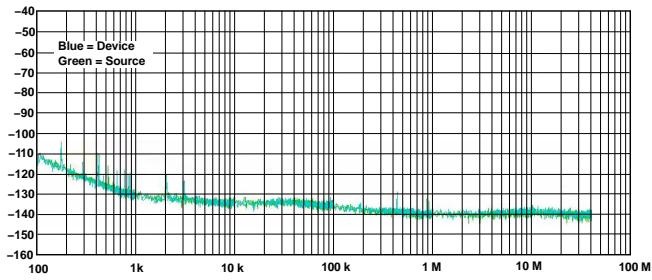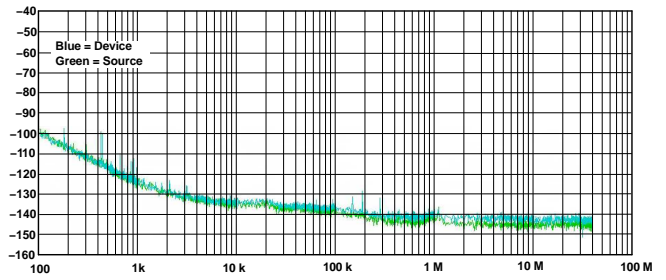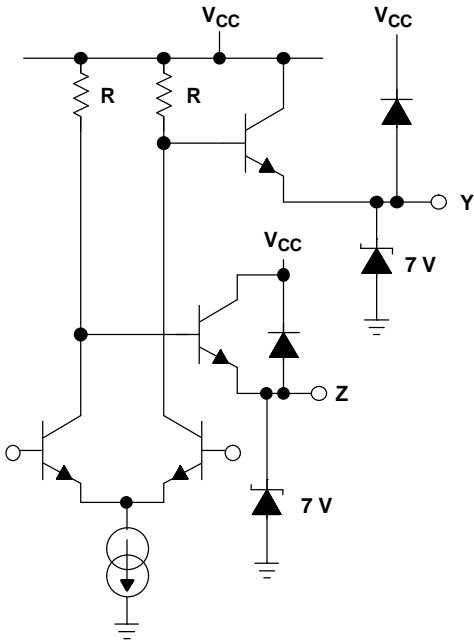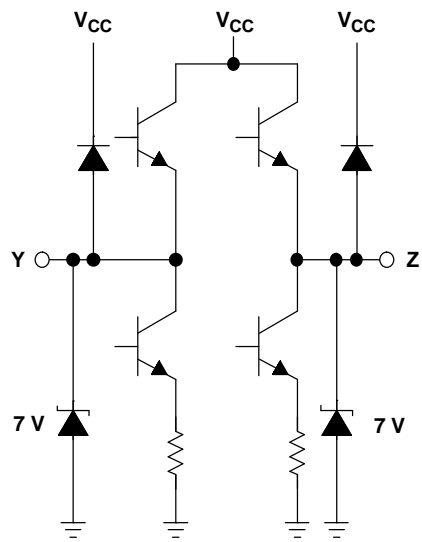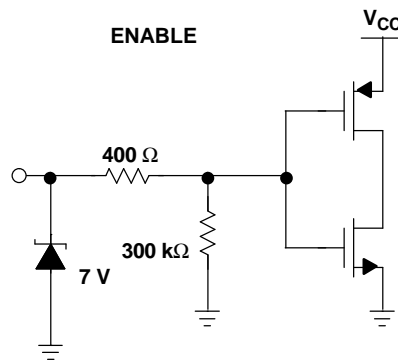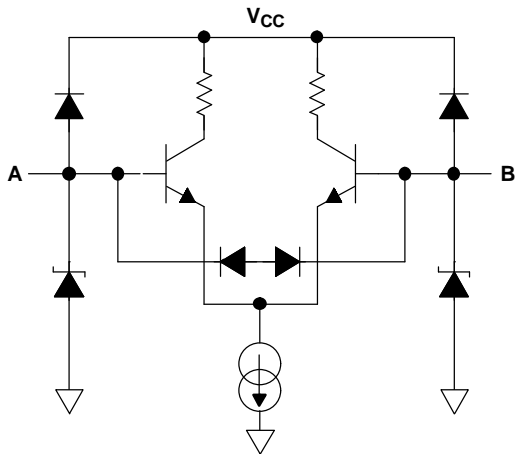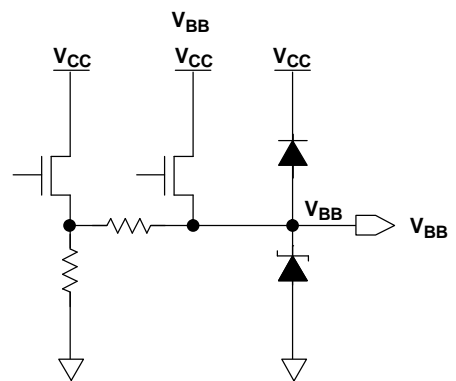| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDS20DRFR | ACTIVE | WSON | DRF | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | E8 | Samples |
| SN65LVDS20DRFRG4 | ACTIVE | WSON | DRF | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | E8 | Samples |
| SN65LVDS20DRFT | ACTIVE | WSON | DRF | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | E8 | Samples |
| SN65LVDS20DRFTG4 | ACTIVE | WSON | DRF | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | E8 | Samples |
| SN65LVP20DRFR | ACTIVE | WSON | DRF | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | E7 | Samples |
| SN65LVP20DRFT | ACTIVE | WSON | DRF | 8 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | E7 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|-------------|----------------|------|------|------|------|------|------|------|------|------|------|
| SN65LVDS20DRFR | WSON | DRF | 8 | 3000 | 330.0 | 8.8 | 2.3 | 2.3 | 1.0 | 4.0 | 8.0 | Q2 |
| SN65LVDS20DRFT | WSON | DRF | 8 | 250 | 330.0 | 8.8 | 2.3 | 2.3 | 1.0 | 4.0 | 8.0 | Q2 |
| SN65LVP20DRFR | WSON | DRF | 8 | 3000 | 330.0 | 8.8 | 2.3 | 2.3 | 1.0 | 4.0 | 8.0 | Q2 |
| SN65LVP20DRFT | WSON | DRF | 8 | 250 | 330.0 | 8.8 | 2.3 | 2.3 | 1.0 | 4.0 | 8.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**
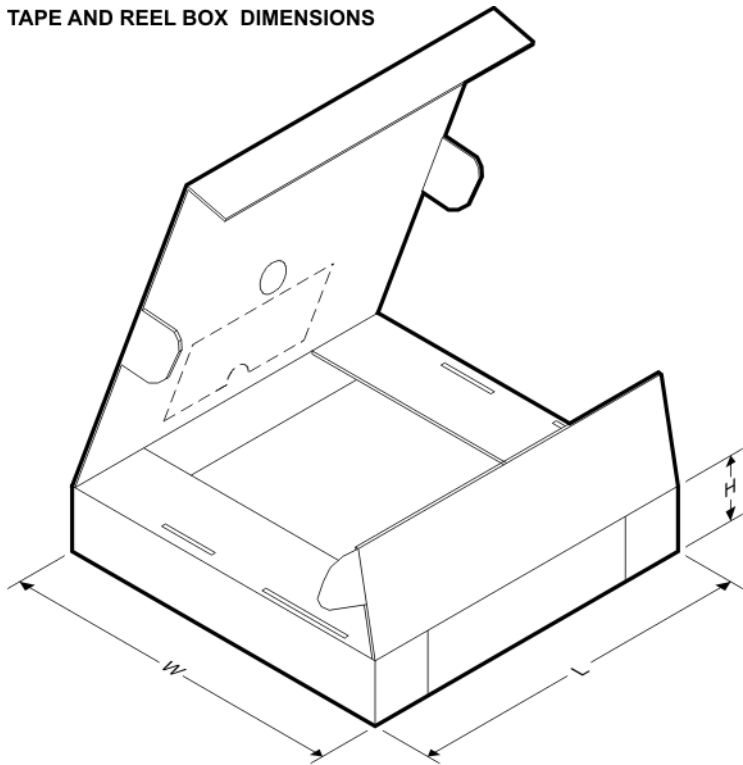


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LVDS20DRFR | WSON | DRF | 8 | 3000 | 337.0 | 343.0 | 29.0 |
| SN65LVDS20DRFT | WSON | DRF | 8 | 250 | 337.0 | 343.0 | 29.0 |
| SN65LVP20DRFR | WSON | DRF | 8 | 3000 | 337.0 | 343.0 | 29.0 |
| SN65LVP20DRFT | WSON | DRF | 8 | 250 | 337.0 | 343.0 | 29.0 |

DRF (S−PWSON−N8)                    PLASTIC SMALL OUTLINE NO−LEAD

$\dfrac{2,10}{1,90}$

8

$\dfrac{2,10}{1,90}$

1

PIN 1 INDEX AREA
TOP AND BOTTOM

$\dfrac{0,80}{0,70}$

0,20 REF.

SEATING PLANE

0,05

$\dfrac{0,05}{0,00}$

8X $\dfrac{0,45}{0,35}$

1            4

EXPOSED THERMAL PAD
⟁D

8            5

8X $\dfrac{0,30}{0,18}$

0,50

1,50

| ⊕ | 0,10 ⓂC A B |
|---|---|
|  | 0,05 ⓂC |

4205287/E 10/10
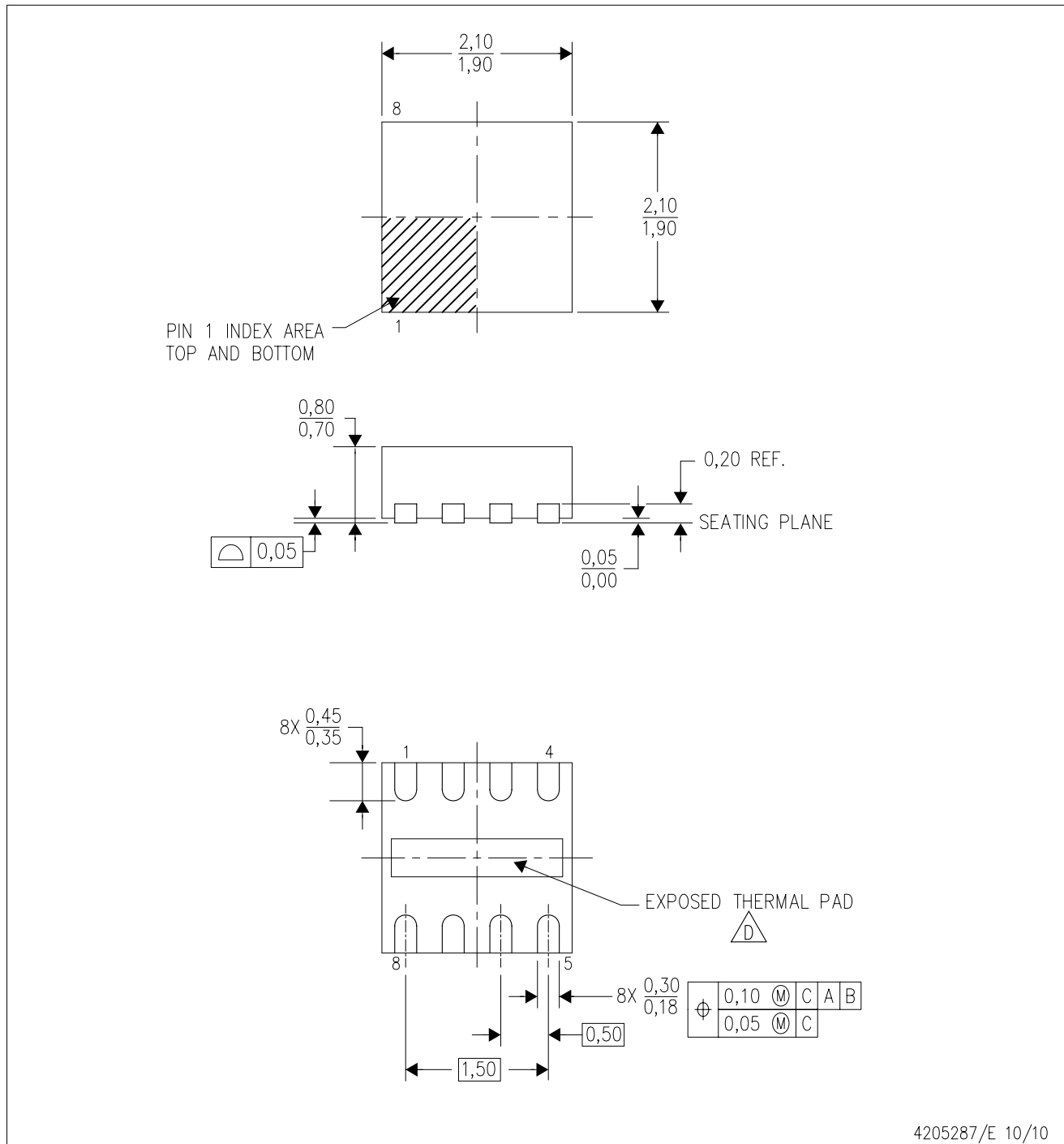
NOTES:  A.  All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B.  This drawing is subject to change without notice.
        C.  Quad Flatpack, No−Leads (QFN) package configuration.
       ⟁D  The Package thermal pad must be soldered to the board for thermal and mechanical performance.
            See product data sheet for details regarding the exposed thermal pad dimensions.
        E.  Falls within JEDEC MO−229.

**TEXAS INSTRUMENTS**
www.ti.com

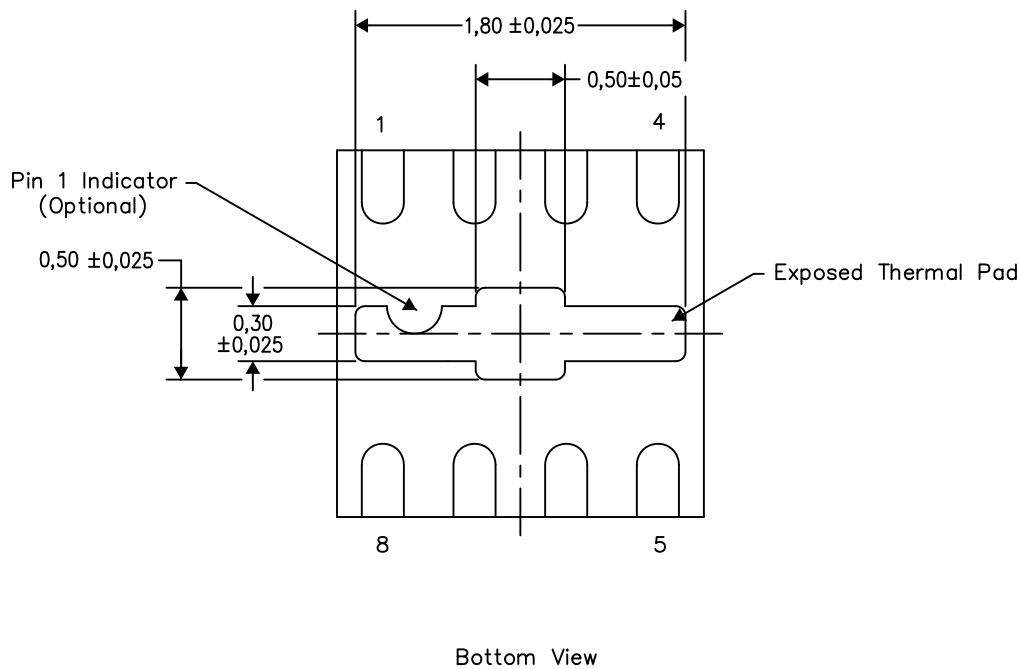DRF (S−PWSON−N8)                    PLASTIC SMALL OUTLINE NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
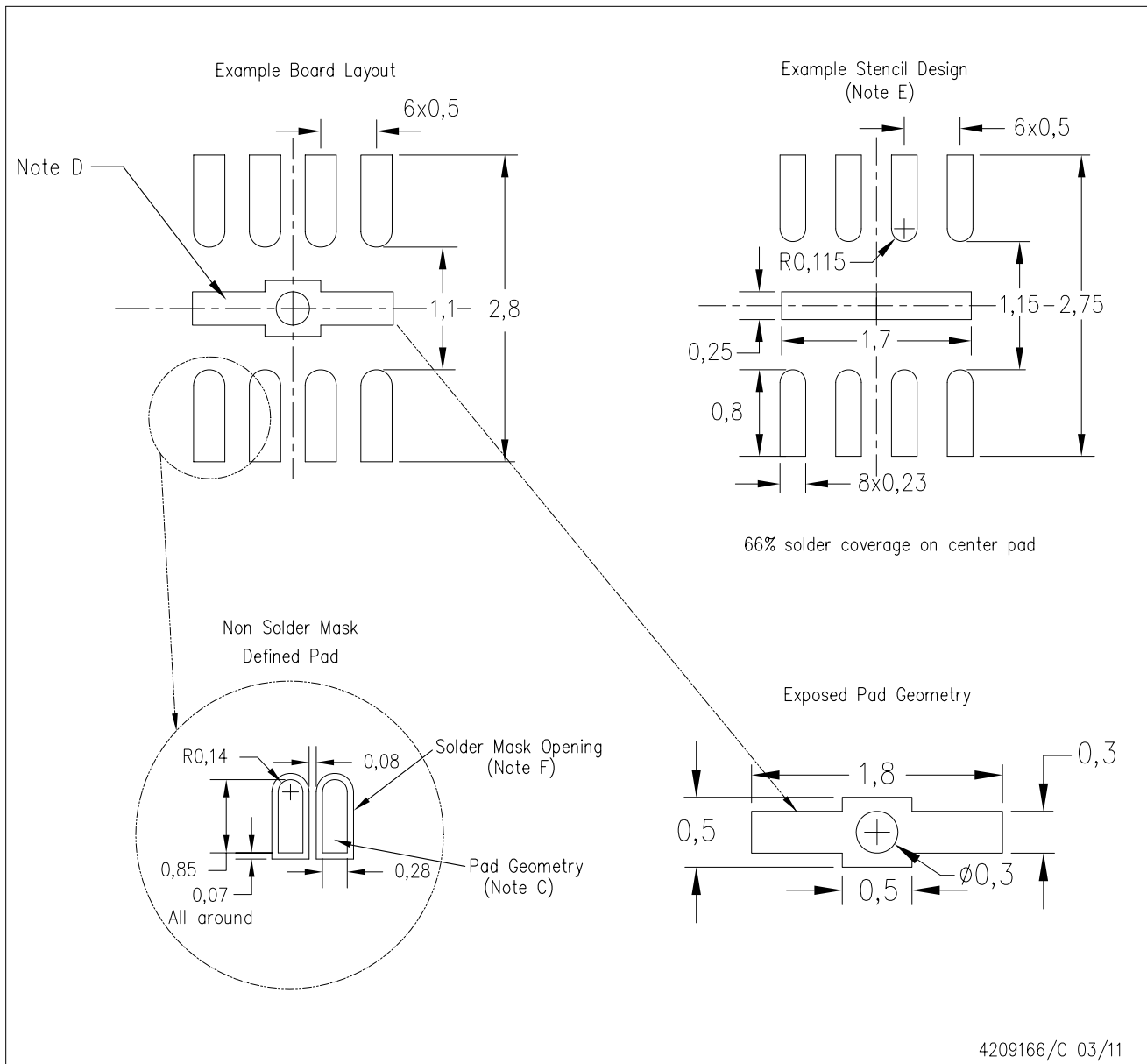


Bottom View

Exposed Thermal Pad Dimensions

4206840/H  12/14

NOTE:   A.   All linear dimensions are in millimeters

DRF (S−PWSON−N8)          PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

6x0,5

Note D

1,1— 2,8

Non Solder Mask
Defined Pad

R0,14          0,08          Solder Mask Opening
(Note F)

0,85

0,07          0,28          Pad Geometry
(Note C)

All around

Example Stencil Design
(Note E)

6x0,5

R0,115

0,25          1,7          1,15—2,75

0,8

8x0,23

66% solder coverage on center pad

Exposed Pad Geometry

1,8          0,3

0,5          ⌀0,3

0,5

4209166/C 03/11

NOTES:    A.    All linear dimensions are in millimeters.
          B.    This drawing is subject to change without notice.
          C.    Publication IPC−7351 is recommended for alternate designs.
          D.    This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat−Pack
                Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
                for specific thermal information, via requirements, and recommended board layout.  These documents are available at
                www.ti.com <http://www.ti.com>.
          E.    Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
                contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
          F.    Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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