HIGH-SPEED 3.3V 1K X 8 DUAL-PORT STATIC RAM
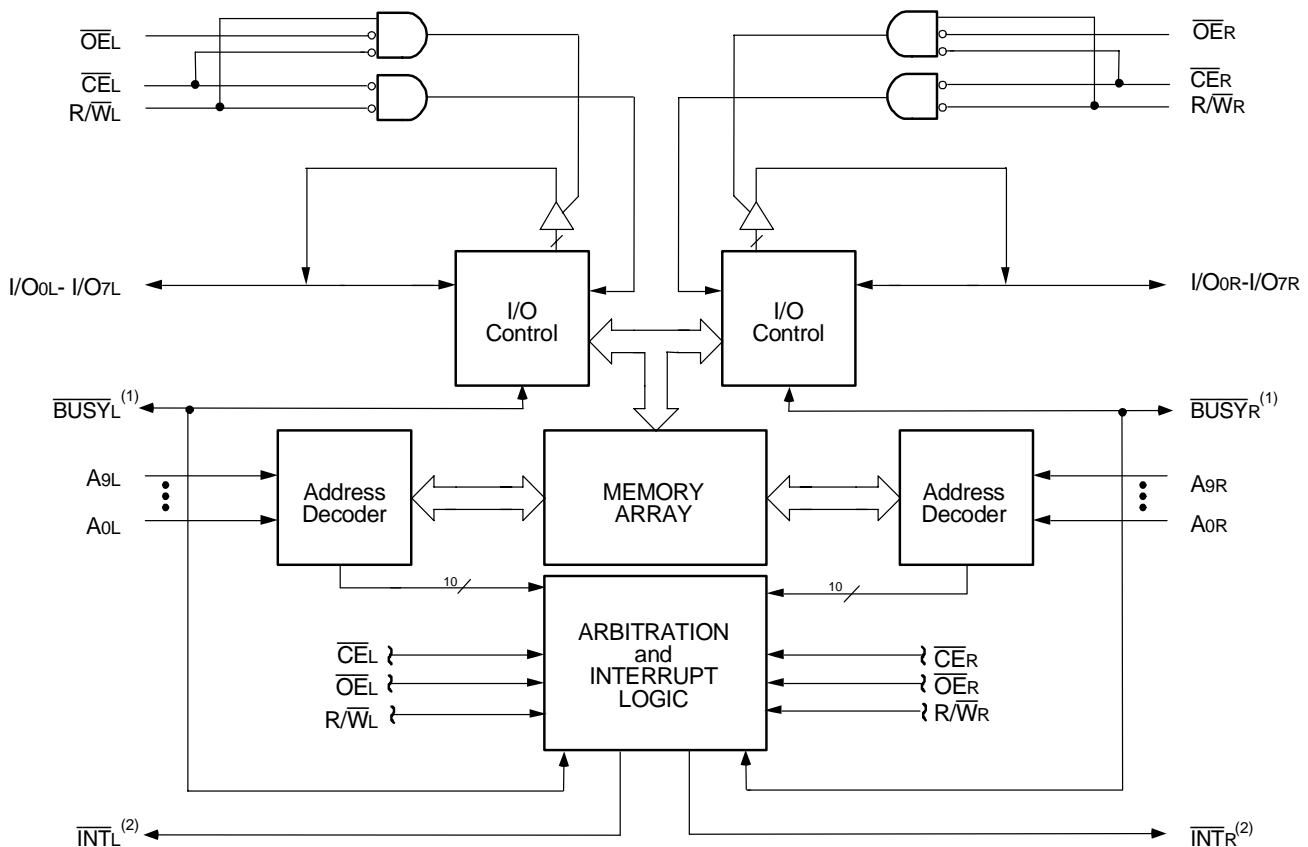
IDT71V30S/L

Features

- **High-speed access**
  - *Commercial: 25/35/55ns (max.)*
  - *Industrial 35ns (max.)*
- **Low-power operation**
  - *IDT71V30S*
    Active: 375mW (typ.)
    Standby: 5mW (typ.)
  - *IDT71V30L*
    Active: 375mW (typ.)
    Standby: 1mW (typ.)
- **On-chip port arbitration logic**
- **Interrupt flags for port-to-port communication**
- **Fully asynchronous operation from either port**
- **Battery backup operation, 2V data retention (L Only)**
- **TTL-compatible, single 3.3V ±0.3V power supply**
- **Industrial temperature range (-40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram

3741 drw 01

NOTES:
1. IDT71V30: $\overline{BUSY}$ outputs are non-tristatable push-pulls.
2. $\overline{INT}$ outputs are non-tristable push-pull output structure.

DECEMBER 2017

1

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Description

The IDT71V30 is a high-speed 1K x 8 Dual-Port Static RAM. The IDT71V30 is designed to be used as a stand-alone 8-bit Dual-Port SRAM.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 375mW of power. Low-power (L) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200μW from a 2V battery.

The IDT71V30 devices are packaged in 64-pin STQFPs.

Pin Configurations[1,2,3]

IDT71V30TF
PP64[4]

64-Pin STQFP
Top View[5]

3741 drw 03
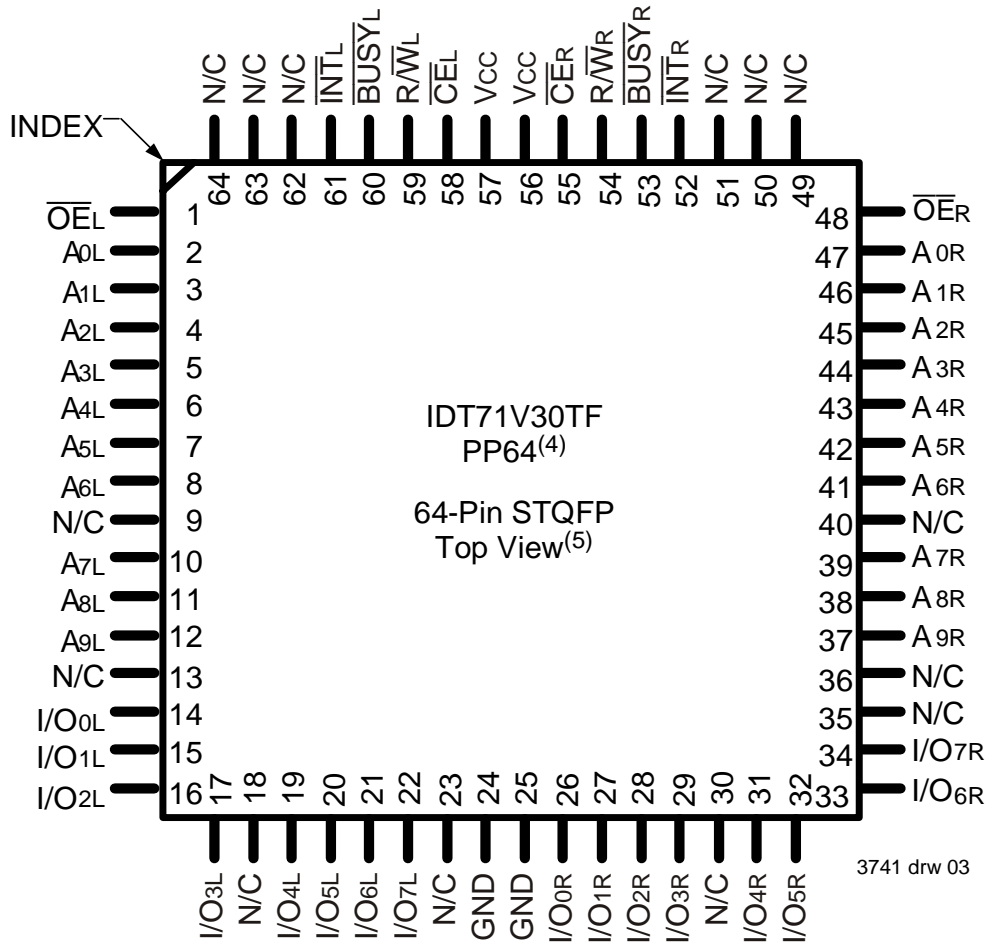
NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 10mm x 10mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate the orientation of the actual part-marking.

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l & Ind	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.60	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}[3]	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

3741 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 0.3V.
3. This is the absolute maximum junction temperature for the device. No DC Bias.

Capacitance[1] (T_A = +25°C, f=1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 3dV	10	pF

3741 tbl 04

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC}+0.3V	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

3741 tbl 02

NOTE:
1. V_{IL} (min.) = -1.5V for pulse width less than 20ns.

Maximum Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3
Industrial	-40°C to +85°C	0V	3.3V ± 0.3

3741 tbl 03

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.
2. Industrial temperature: for specific speeds, packages and powers, contact your sales office.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	71V30S Min.	71V30S Max.	71V30L Min.	71V30L Max.	Unit
$|I_{LI}|$	Input Leakage Current[1]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	μA
$|I_{LO}|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	μA
V_{OL}	Output Low Voltage (I/O0-I/O7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3741 tbl 05

NOTE:
1. At $V_{CC} \leq$ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,6,7] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		71V30X25 Com'l Only Typ.[2]	71V30X25 Com'l Only Max.	71V30X35 Com'l & Ind Typ.[2]	71V30X35 Com'l & Ind Max.	71V30X55 Com'l Only Typ.[2]	71V30X55 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled f = f_{MAX}[3]	COM'L	S L	75 75	150 120	75 75	145 115	75 75	135 105	mA
			IND	S L	— —	— —	— 75	— 145	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, f = f_{MAX}[3]	COM'L	S L	20 20	50 35	20 20	50 35	20 20	50 35	mA
			IND	S L	— —	— —	— 20	— 50	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[3]	COM'L	S L	30 30	105 75	30 30	100 70	30 30	90 60	mA
			IND	S L	— —	— —	— 30	— 100	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	COM'L	S L	1.0 0.2	5.0 3.0	1.0 0.2	5.0 3.0	1.0 0.2	5.0 3.0	mA
			IND	S L	— —	— —	— 1.0	— 5.0	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled f=f_{MAX}[3]	COM'L	S L	30 30	90 75	30 30	85 70	30 30	75 60	mA
			IND	S L	— —	— —	— 30	— 85	— —	— —	

3741 tbl 06

NOTES:
1. 'X' in part number indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 70mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Refer to chip enable Truth Table I.
7. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Data Retention Characteristics (L Version Only)

| Symbol	Parameter	Test Condition		71V30L Min.	71V30L Typ.[1]	71V30L Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V, $\overline{CE}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V	Ind.	—	100	1000	µA
			Com'l.	—	100	500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

3741 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

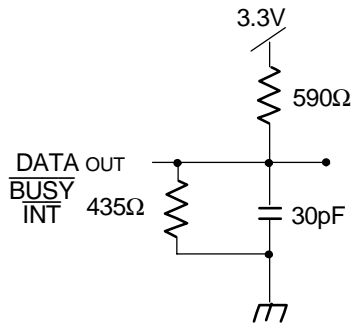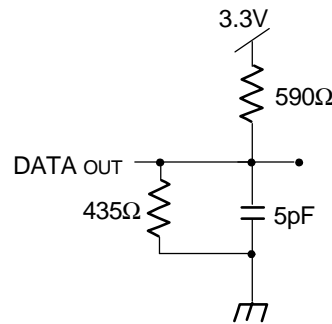3741 tbl 08

Data Retention Waveform
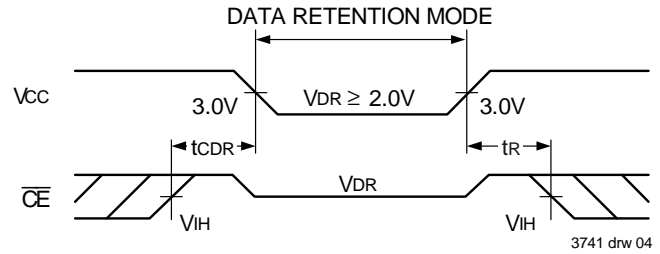
3741 drw 04

Figure 1. AC Output Test Load

3741 drw 05

Figure 2. Output Test Load
(For t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})
* Including scope and jig.

AC Electrical Characteristics Over the
## Operating Temperature and Supply Voltage Range[3,4]

Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25	—	35	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time	—	25	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	12	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns

3741 tbl 09

NOTES:
1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (S or L).
4. Industrial temperature: for specific speeds, packages and power contact your sales office.

## Timing Waveform of Read Cycle No. 1, Either Side[1]
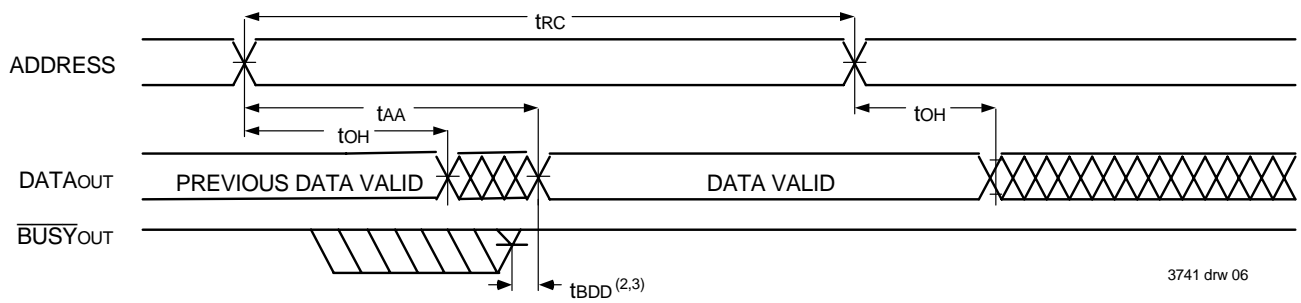
3741 drw 06

NOTES:
1. R/$\overline{W}$ = V$_{IH}$, $\overline{CE}$ = V$_{IL}$, and is $\overline{OE}$ = V$_{IL}$. Address is valid prior to the coincidental with $\overline{CE}$ transition LOW.
2. t$_{BDD}$ delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultaneous read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last t$_{AOE}$, t$_{ACE}$, t$_{AA}$, and t$_{BDD}$.

Timing Waveform of Read Cycle No. 2, Either Side[3]
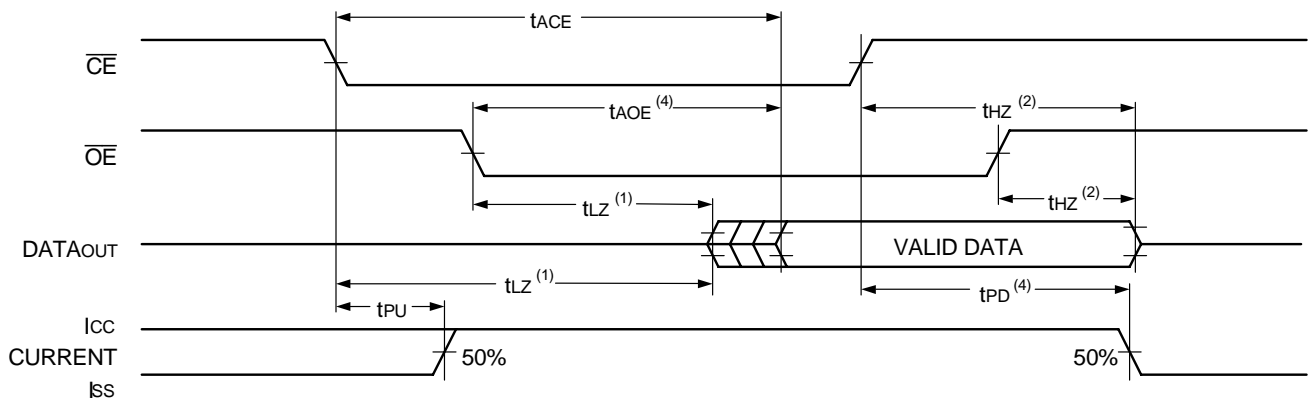
3741 drw 07

NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is desserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V$_{IH}$ and the address is valid prior to or coincidental with $\overline{CE}$ transition LOW.
4. Start of valid data depends on which timing becomes effective last t$_{AOE}$, t$_{ACE}$, and t$_{BDD}$.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[4,5]

| Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	20	—	20	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	30	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	15	—	15	—	30	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	0	—	0	—	0	—	ns

3741 tbl 10

NOTES:
1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the SRAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. 'X' in part number indicates power rating (S or L).
5. Industrial temperatures: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Write Cycle No. 1,(R/$\overline{W}$ Controlled Timing)[1,5,8]
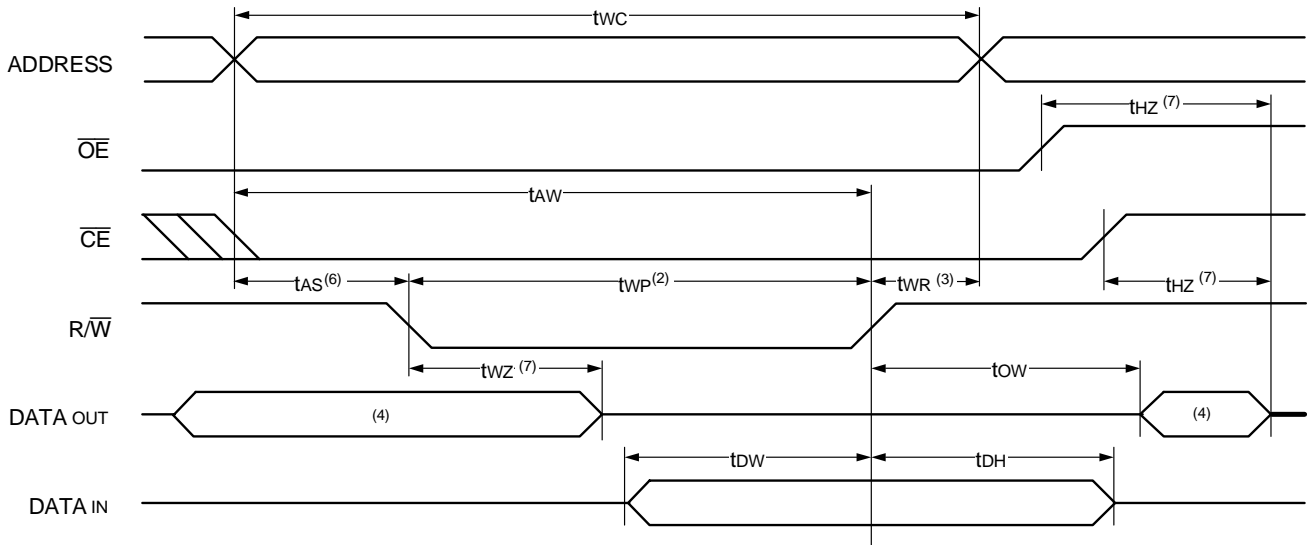
3741 drw 08

Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing[1,5]
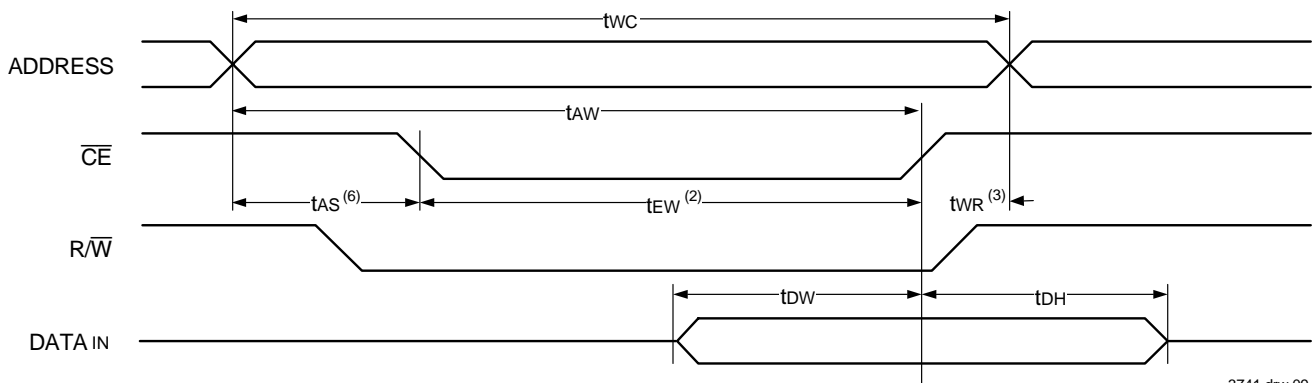
3741 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of $\overline{CE}$ = V_{IL} and R/$\overline{W}$= V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6,7]

Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/S=V$_{IH}$)								
t$_{BAA}$	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	—	30	ns
t$_{BDA}$	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	—	30	ns
t$_{BAC}$	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	30	ns
t$_{BDC}$	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	30	ns
t$_{WH}$	Write Hold After $\overline{BUSY}$[5]	20	—	30	—	40	—	ns
t$_{WDD}$	Write Pulse to Data Delay[1]	—	50	—	60	—	80	ns
t$_{DDD}$	Write Data Valid to Read Data Delay[1]	—	35	—	45	—	65	ns
t$_{APS}$	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
t$_{BDD}$	$\overline{BUSY}$ Disable to Valid Data[3]	—	30	—	30	—	45	ns

3741 tbl 11

NOTES:
1. Port-to-port delay through SRAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read with BUSY".
2. To ensure that the earlier of the two ports wins.
3. t$_{BDD}$ is a calculated parameter and is the greater of 0, t$_{WDD}$ – t$_{WP}$ (actual) or t$_{DDD}$ – t$_{DW}$ (actual).
4. To ensure that the Write Cycle is inhibited on Port "B" during contention on Port "A".
5. To ensure that the Write Cycle is completed on Port "B" after contention on Port "A".
6. 'X' in part number indicates power rating (S or L).
7. Industrial temperature: for specific speeds, packages and powers contact your sales office.

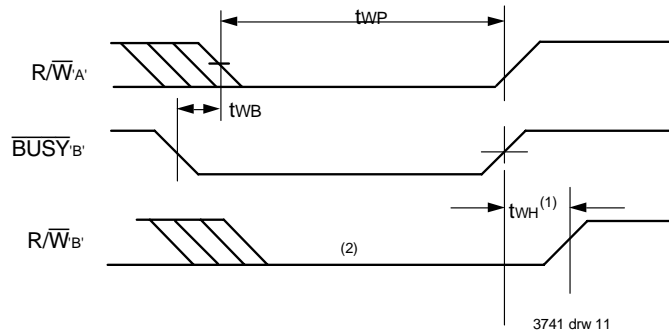## Timing Waveform of Write with Port-to-Port Read with $\overline{BUSY}$[1,2,3,4]
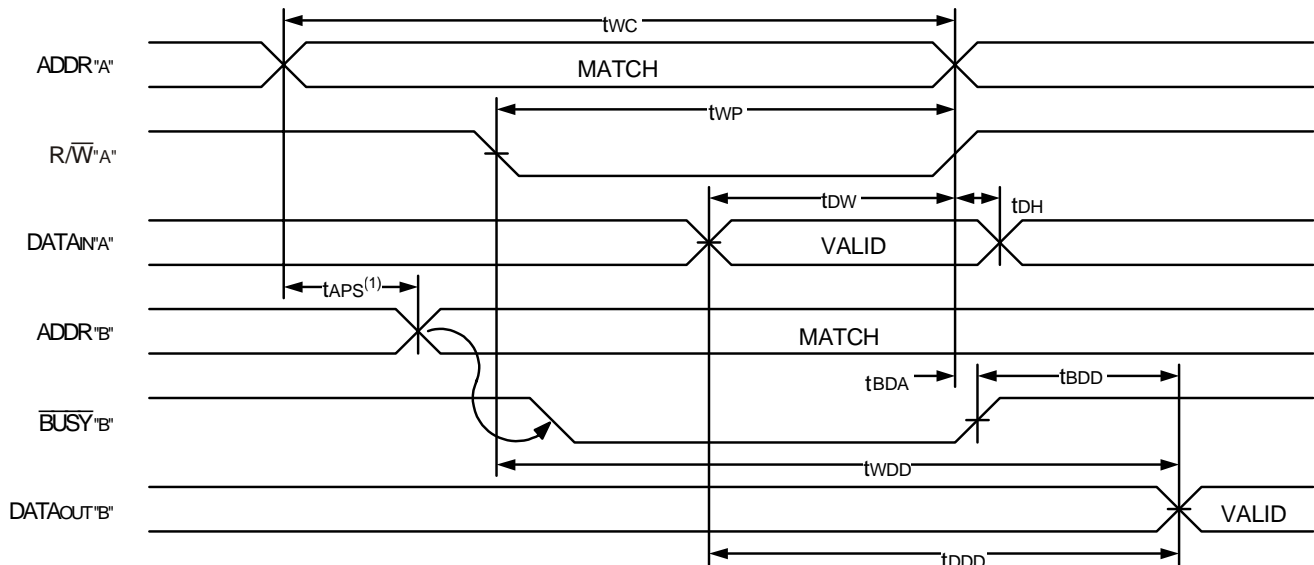
3741 drw 10

NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}$L = $\overline{CE}$R = V$_{IL}$
3. $\overline{OE}$ = V$_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

Timing Waveform of Write with $\overline{BUSY}$[3]

3741 drw 11

NOTES:
1. t_{WH} must be met for $\overline{BUSY}$.
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/$\overline{W}$'B', until $\overline{BUSY}$'B' goes HIGH.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".
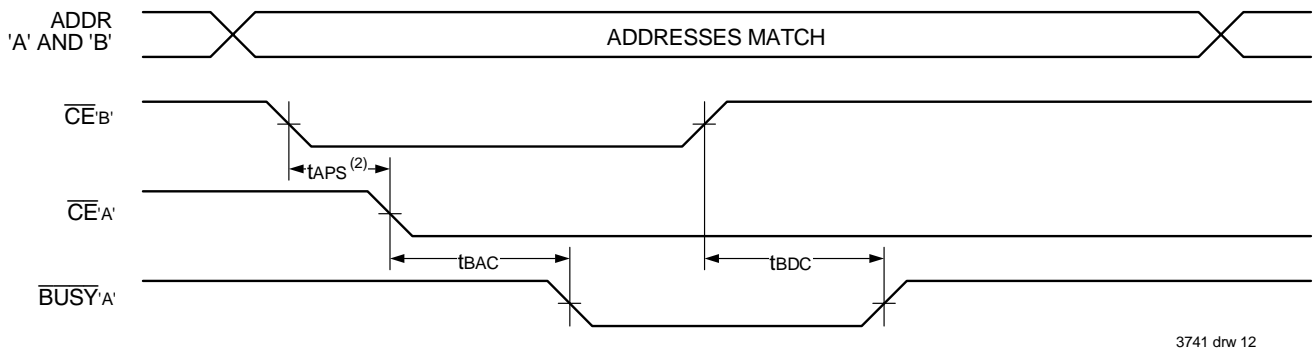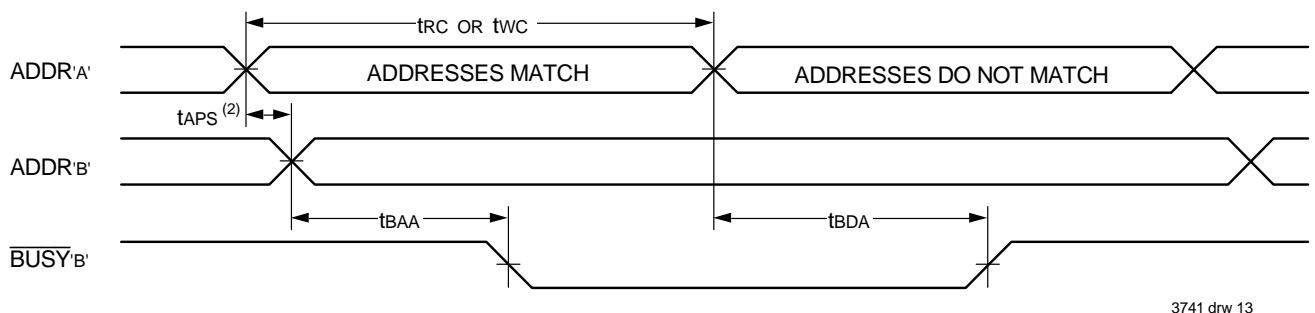
Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing[1]

3741 drw 12

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If t_{APS} is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

Timing Waveform of $\overline{BUSY}$ Arbitration Controlled Address Match Timing[1]

3741 drw 13

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If t_{APS} is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,2]

| Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	25	—	45	ns
t_{INR}	Interrupt Reset Time	—	25	—	25	—	45	ns

3741 tbl 12

NOTES:
1. 'X' in part number indicates power rating (S or L).
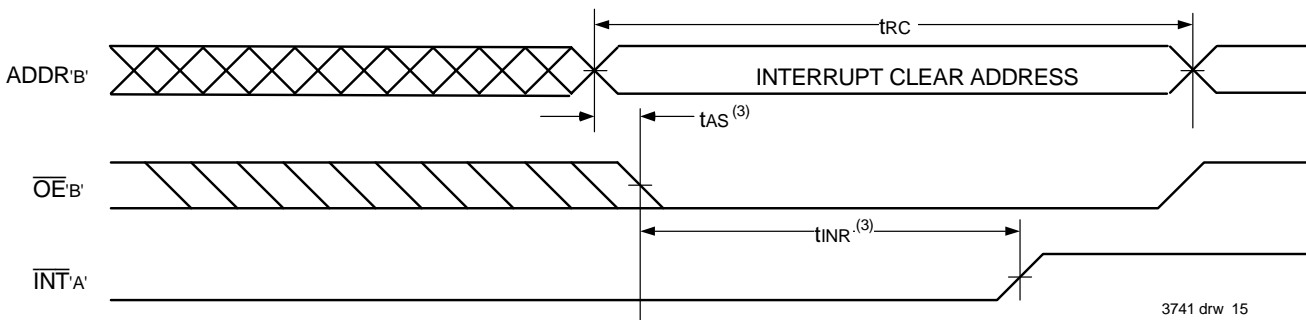2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Interrupt Mode[1]
$\overline{\text{INT}}$ Sets
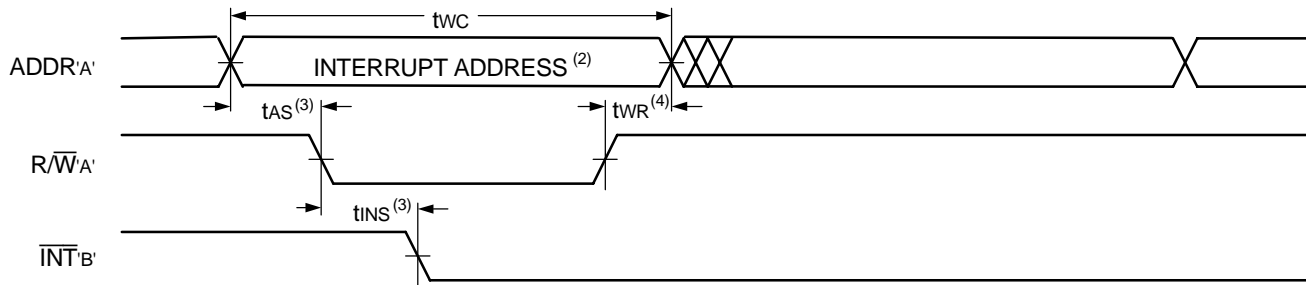
3741 drw 14

$\overline{\text{INT}}$ Clears

3741 drw 15

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal ($\overline{\text{CE}}$ or R/$\overline{\text{W}}$) is asserted last.
4. Timing depends on which enable signal ($\overline{\text{CE}}$ or R/$\overline{\text{W}}$) is de-asserted first.

Truth Tables

Table I — Non-Contention Read/Write Control[4]

Left or Right Port [1]				Function
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATA$_{IN}$	Data on Port Written Into Memory[2]
H	L	L	DATA$_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

3741 tbl 13

NOTES:
1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

Table II — Interrupt Flag[1,4]

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{9L}-A_{0L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{9R}-A_{0R}$	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

3741 tbl 14

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH,' 'L' = LOW,' 'X' = DON'T CARE

Table III — Address $\overline{BUSY}$ Arbitration

Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	$A_{0L}-A_{9L}$ $A_{0R}-A_{9R}$	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

3741 tbl 15

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT71V30. $\overline{BUSY}_X$ outputs on the IDT71V30 are non-tristatable push-pull.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Functional Description

The IDT71V30 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71V30 has an automatic power down feature controlled by CE. The CE controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V$_{IH}$). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V$_{IL}$ per Truth Table II. The left port clears the interrupt by accessing address location 3FE access with $\overline{CE}_R$ = $\overline{OE}_R$ = V$_{IL}$, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must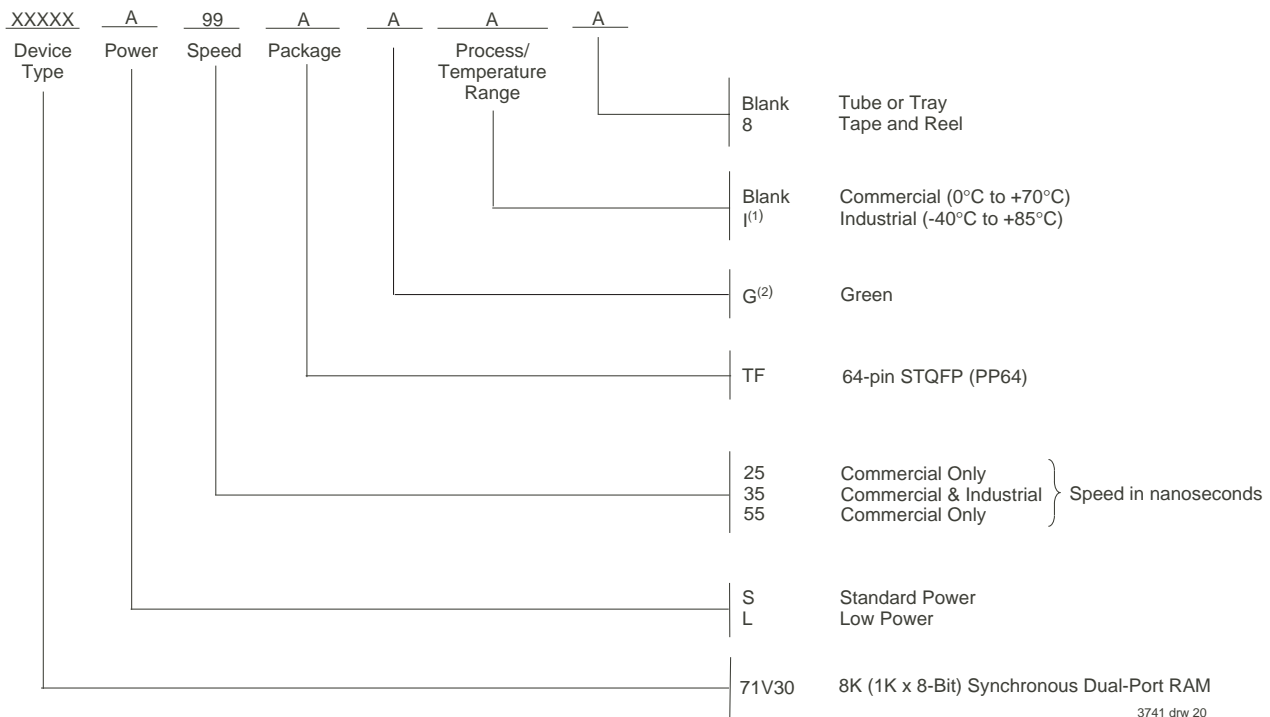 access the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, and are part of the random access memory. Refer to Table II for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the SRAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the SRAM is "Busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation.

Ordering Information

XXXXX   A   99   A   A   A   A

Device Type | Power | Speed | Package | Process/Temperature Range

Blank	Tube or Tray
8	Tape and Reel

Blank	Commercial (0°C to +70°C)
I[1]	Industrial (-40°C to +85°C)

G[2]	Green

TF	64-pin STQFP (PP64)

25	Commercial Only	
35	Commercial & Industrial	Speed in nanoseconds
55	Commercial Only	

S	Standard Power
L	Low Power

71V30	8K (1K x 8-Bit) Synchronous Dual-Port RAM

3741 drw 20

NOTES:
1. Industrial temperature range is available. For specific speeds, packages and powers contact your sales office.
2. Green parts available. For specific speeds, packages and powers contact your sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

12/9/98:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Added additional notes to pin configurations
6/15/99:	Changed drawing format
8/3/99:	Page 2 Fixed typographical error
9/1/99:	Removed Preliminary
11/12/99:	Replaced IDT logo
1/17/01:	Pages 1 and 2 Moved all of "Description" to page 2 and adjusted page layouts
	Page 3 Increased storage temperature parameters
	Clarified T$_A$ parameter
	Page 4 DC Electrical parameters–changed wording from "open" to "disabled"
	Changed ±200mV to 0mV in notes
3/14/05:	Page 1 Added green availability to features
	Page 17 Added green indicator to ordering information
	Page 1 & 17 Replaced old TM logo with new TM logo
7/16/07:	Page 3 Added Junction Temperature spec values to the Absolute Maximum Rating table
	Added footnote 3 for additional clarification of Junction Temperature

Datasheet Document History (con't)

10/23/08:	Page 14	Removed "IDT" from orderable part number
11/25/09:	Page 4	In order to correct the DC Chars table for the 71V30L35 speed grade and to the Data Retention Chars table, I Temp values have been added to each table respectively. In addition, all of the AC tables and the ordering information also now reflect this I temp correction
06/22/15:	Page 2	Removed IDT in reference to fabrication
	Page 2 & 14	The package code PP64-1 changed to PP64 to match standard package codes
	Page 14	Added Tape and Reel indicator to Ordering Information
07/23/15:	Entire datasheet	Removed the 55ns Industrial speed offering. 55ns speed only offered in commercial grade
12/20/17:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018

IDT.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-284-2794
DualPortHelp@idt.com