

High-Performance Synchronous Buck EVM Using the TPS51117

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1 Hardware

1.1 Operating Specification, TPS51117

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range(V5IN)			4.5		5.5	V
Input voltage range(Vbat)			6		21	V
VOUT	Output voltage	Configuration (of EVM)		1.05		V
	Operating frequency	TON : adjustable		350k	400k	Hz
	Output current				10	A
	Current limit			15		A

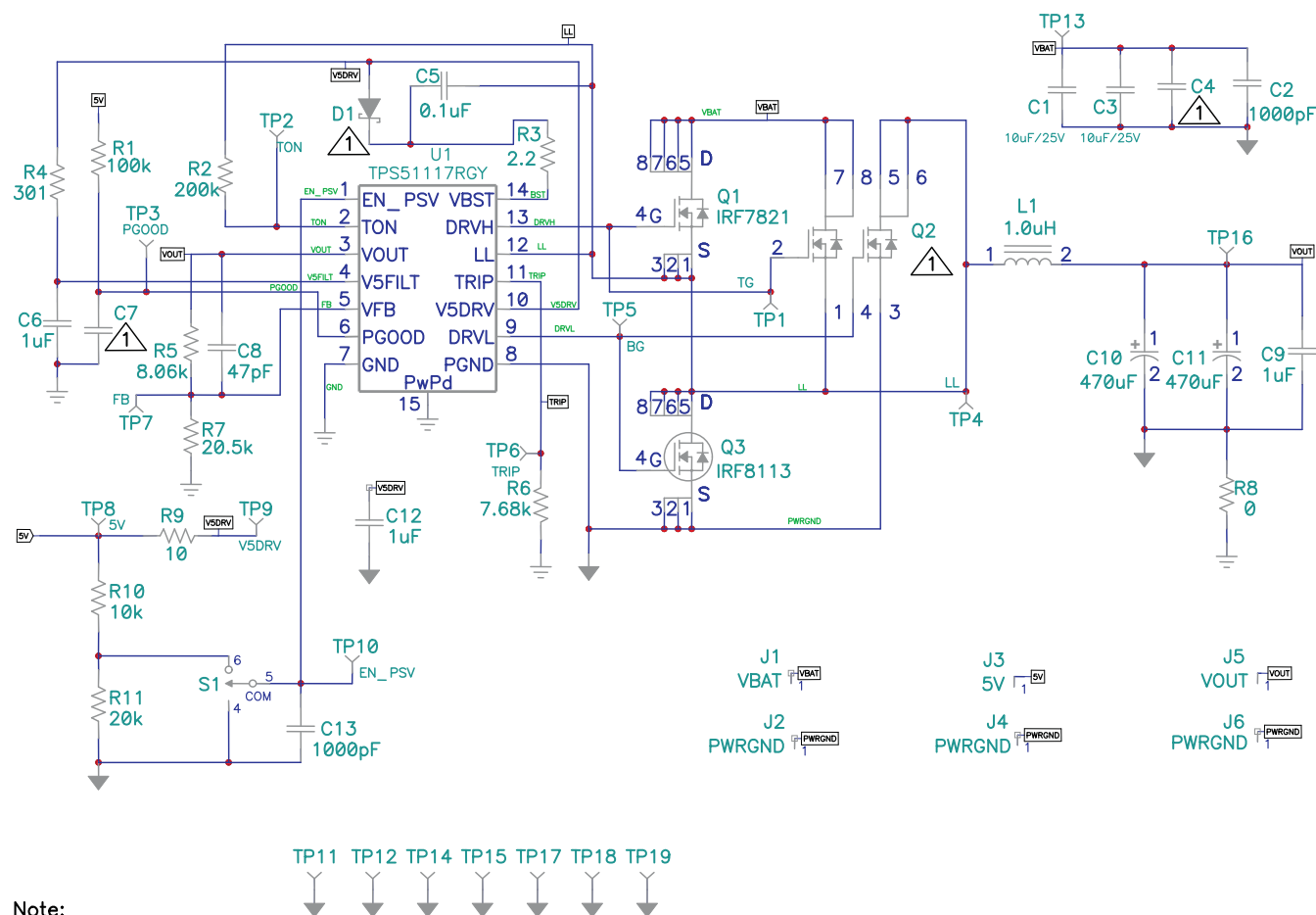
1.2 Features

The TPS51117 evaluation module (EVM) is designed to evaluate the performance and characteristics of TI's cost optimized, D-CAP™ mode, synchronous buck controller, TPS51117. The three main features of this evaluation module follow.

1. Multiple footprint designs support multiple MOSFET configurations.
2. Abundant test points provide users with great convenience. See test point summary table.
3. Although two TPS51117 package styles are available, the EVM is designed to demonstrate the QFN14 package.

D-CAP is a trademark of Texas Instruments.

1.3 Schematic



Note:

 Do not install component.

Figure 1. TPS51117RGY Evaluation Module (1.05 V at 10 A) Schematic Diagram

1.4 Bill of Materials

Table 1 presents The TPS51117EVM bill of materials.

Table 1. TPS51117EVM Bill of Materials

RefDes	Pattern Name	Value	Part Number	MFR
EVM Configuration 1.05 V at 10 A BOM				
C5	C603	0.1µF	VJ0603Y104KXXAC	Vishay
C12, C6	C603	1µF, 16V	C1608X7R1C105K	TDK
C8	C603	47pF	VJ0603A470JXAAC	Vishay
C2, C13	C603	1000pF	VJ0603Y102KXAAC	Vishay
C4	C603	Not Installed	VJ0603Y102KXAAC	Vishay
C7	C603	Not Installed	VJ0603Y103KXAAC	Vishay
C9	C0805	1µF, 25V	C2012X7R1E105K	TDK
C1, C3	C1206	10µF, 25V	ECJ-3YB1E106K	Panasonic
C10, C11	CAP_POSCAP_D	470µF	2R5TPE470MC	Sanyo
J3	HEADER_8952	5V	1582-2	Keystone

Table 1. TPS51117EVM Bill of Materials (continued)

RefDes	Pattern Name	Value	Part Number	MFR
J2	HEADER_8952	PWRGND	1582-2	Keystone
J4	HEADER_8952	PWRGND	1582-2	Keystone
J6	HEADER_8952	PWRGND	1582-2	Keystone
J1	HEADER_8952	VBAT	1582-2	Keystone
J5	HEADER_8952	VOUT	1582-2	Keystone
D1	SOD-123	Not Installed	MBR0530Tx	On Semi
Q2	SO8	Not Installed	Si4944DY	Siliconix
L1	IND_IHLP-5050	1.0 μ H	IHLP5050CEER1R0M01	Vishay
Q1	SO8	IRF7821	IRF7821	IR
Q3	SO8	IRF8113	IRF8113	IR
R8	R603	0	STD	Vishay
R3	R603	2.21	STD	Vishay
R6	R603	7.68k	STD	Vishay
R5	R603	8.06k	STD	Vishay
R9	R603	10	STD	Vishay
R4	R603	301	STD	Vishay
R10	R603	10k	STD	Vishay
R11	R603	20k	STD	Vishay
R7	R603	20.5k	STD	Vishay
R1	R603	100k	STD	Vishay
R2	R603	200k	CRCW06032003FKTA	Vishay
S1	SW_1P3T	G13AP	G13AP	NKK
U1	QFN14	TPS51117RGY	TPS51117RGY	TI
Test Points Summary				
TP1	TP-SMALL	TG	5002	Keystone
TP2	TP-SMALL	Not Installed	5002	Keystone
TP3	TP-SMALL	PGOOD	5002	Keystone
TP4	TP-SMALL	LL	5002	Keystone
TP5	TP-SMALL	BG	5002	Keystone
TP6	TP-SMALL	Not Installed	5002	Keystone
TP7	TP-SMALL	Not Installed	5002	Keystone
TP8	TP-SMALL	5V	5002	Keystone
TP9	TP-SMALL	V5DRV	5002	Keystone
TP10	TP-SMALL	EN_PSV	5002	Keystone
TP11	TP-SMALL	Not Installed	5002	Keystone
TP12	TP-SMALL	GND	5002	Keystone
TP13	TP-SMALL	VBAT	5002	Keystone
TP14	TP-SMALL	GND	5002	Keystone
TP15	TP-SMALL	GND	5002	Keystone
TP16	TP-SMALL	VOUT	5002	Keystone
TP17	TP-SMALL	GND	5002	Keystone
TP18	TP-SMALL	GND	5002	Keystone
TP19	TP-SMALL	Not Installed	5002	Keystone
Hardware Summary				
Standoff	0.44x0.20 Black Bumpons (Self adhesive polyurethane)	Attach to 4 bottom corners	SJ5003-0	3M (Digi-Key)

1.5 Board Layout Using TPS5117RGY (QFN 14)

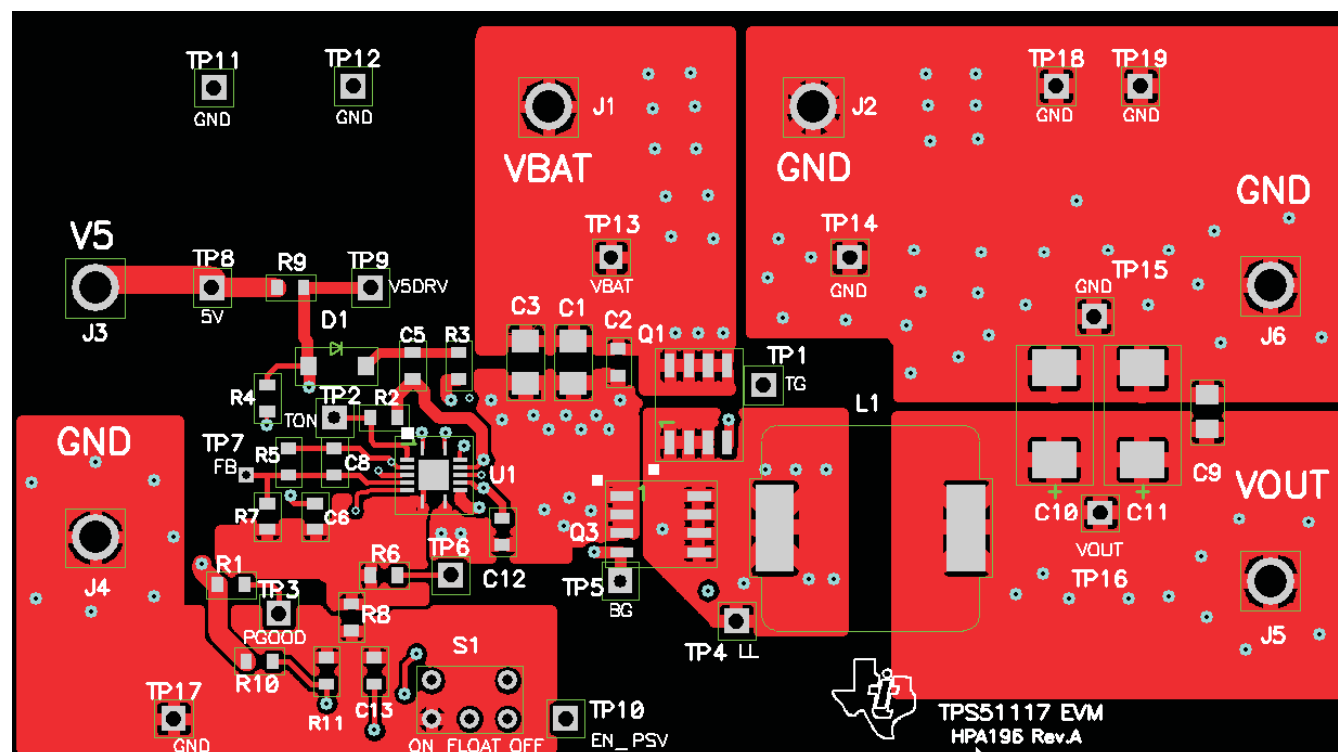


Figure 2. Top Layer Copper

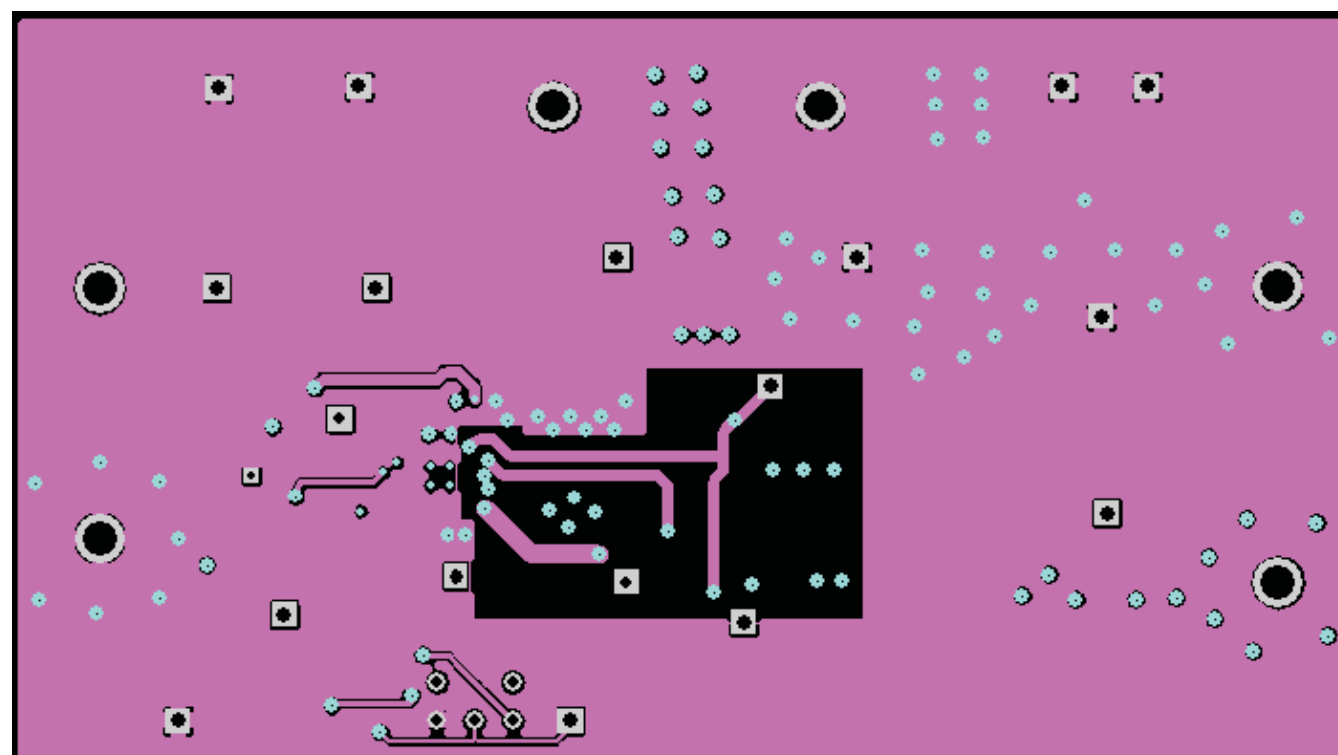


Figure 3. Layer 2 (Internal 1) Copper

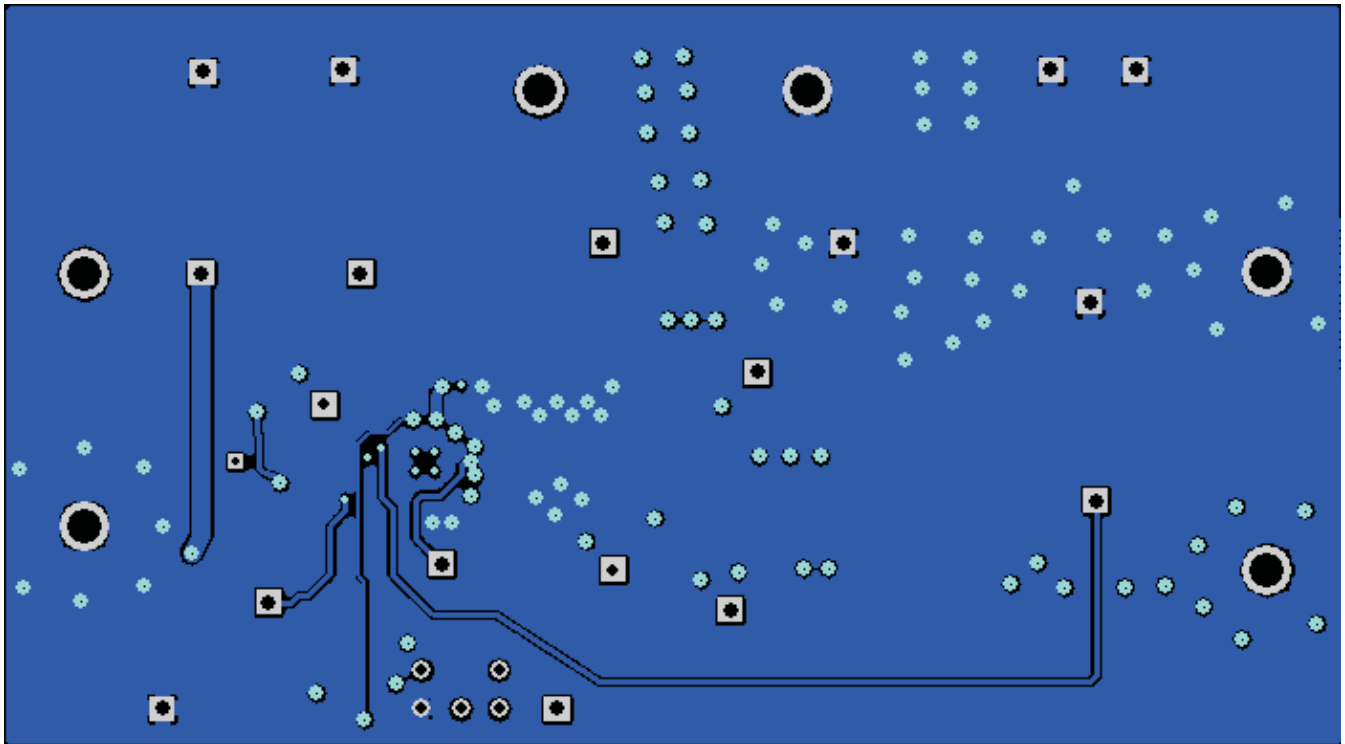


Figure 4. Layer 3 (Internal 2) Copper

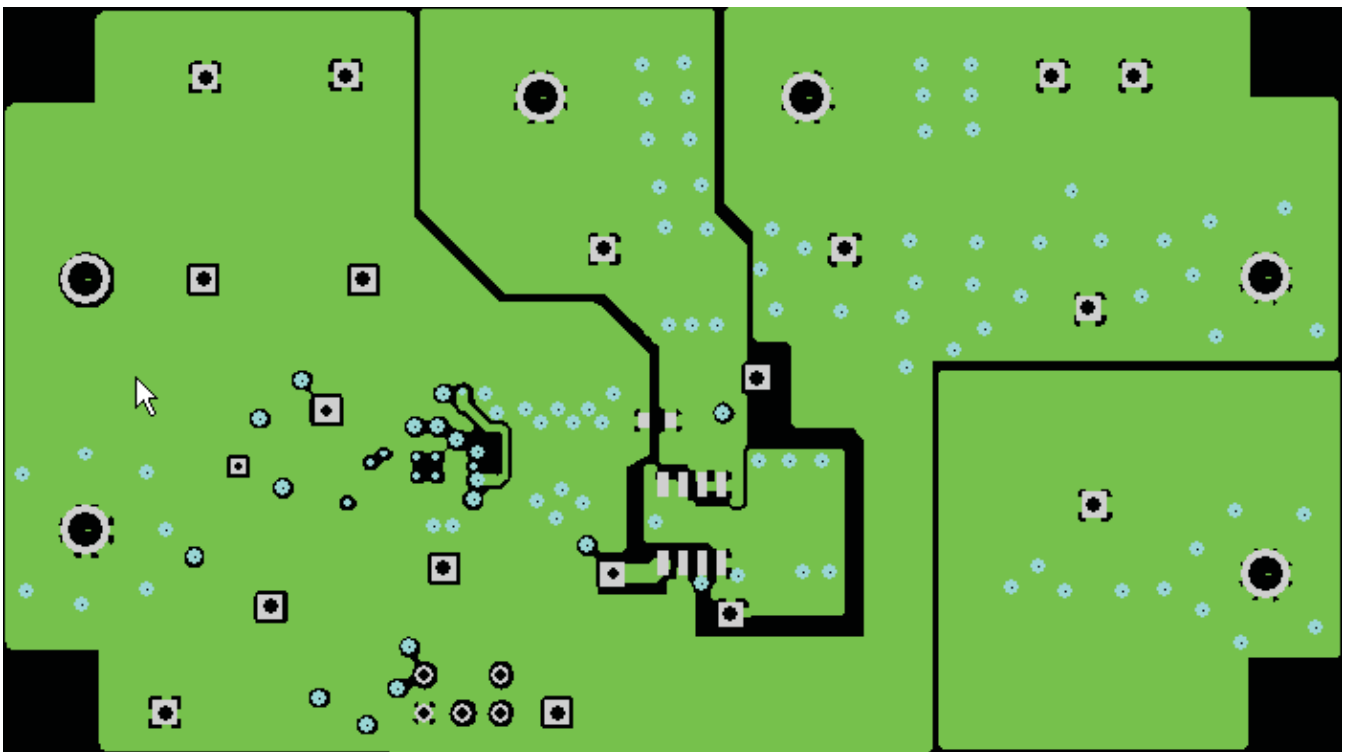


Figure 5. Bottom Layer Copper

1.6 Test Setup and Procedures

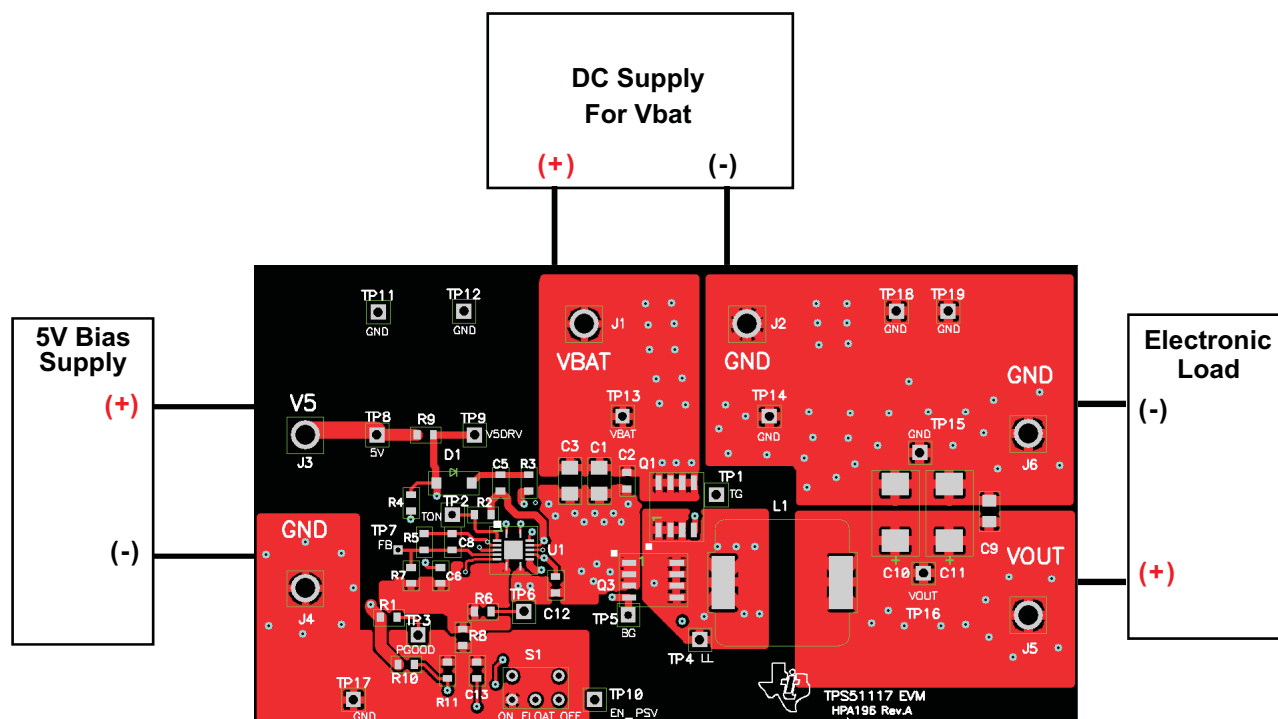


Figure 6. Test Setup

- **Standard Test Procedures**

- *Required Equipment:*
2 x Bench power supplies (5-V supply should be able to source ~ 1 A while Vbat supply ~ 5 A) + electronic load
- *EN_PSV Setting:*
EN_PSV = OFF, Converter is off.
EN_PSV = FLOAT, Converter is operating in forced PWM mode.
EN_PSV = ON, Converter is operating in Skip mode.
- *Bootstrap Diode:*
Bootstrap diode D1 is not populated on the current evaluation module because TPS51117 has a built-in bootstrap diode. In order to further improve the efficiency, D1 can be added.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 6 V to 21 V and the output voltage range of 0.75 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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