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FAIRCHILD SEMICONDUCTOR®

July 2012

FAB3103
2.3 Watt Class-D Audio Amplifier with Integrated Boost Regulator and Automatic Gain Control

Features

- High Output, Low Distortion Class-D Mono Speaker Amplifier
  - o 2.3W into 8Ω from 3.6V Supply (10% THD+N)
  - o 1.85W into 8Ω from 3.6V Supply (1% THD+N)
  - o 0.01% THD+N into 8Ω (100mW)
- High-Efficiency Boost Regulator Provides Higher Output Power Over Li-Ion Battery Voltages
  - o 85% Total Efficiency (3.6V, 8Ω, P_O = 1.0W)
- Adaptive Boost Shutdown at Lower Output Power Increases Efficiency and Reduces Quiescent Current Consumption:
  - o I_{DD} = 2.7mA from 3.6V Supply
- Automatic Gain Control (AGC) Monitors Battery Voltage and Dynamically Adjusts Gain, Extending Battery Runtime
- Reduced Noise Floor Enhances Audio Playback
  - o 38µV Output Noise (A-Weighted)
  - o 100dB SNR (A-Weighted)
- Low-EMI Design Allows Filterless Operation
- High-Power Supply Ripple Rejection:
  - o 88dB PSRR (f_{RIPPLE} = 217Hz, Boost Enabled)
  - o 70dB PSRR (f_{RIPPLE} = 217Hz, Boost Bypassed)
- High Noise Rejection Using Differential Audio Inputs:
  - o 75dB CMRR (f_{IN} = 1kHz)
  - o 71dB CMRR (f_{IN} = 217Hz)
- Short-Circuit Protection
- Under-Voltage Protection
- "Click and Pop" Suppression
- Available in 12-Bump, 0.5mm Pitch, WLCSP
  - o Space-Saving 1.86mm x 1.44mm Package

Description

The FAB3103 is a mono Class-D audio amplifier with an integrated boost regulator that achieves high output audio over a power supply range of 2.5V to 5.2V.

Automatic Boost Shutdown dynamically shuts down the boost regulator at low output power for greater efficiency and lower quiescent current consumption.

Automatic Gain Control (AGC) monitors the battery and reduces gain as the battery voltage drops to limit maximum current consumption, extending battery runtime and preventing mobile device shutdown.

Applications

- Smart Phones, Feature Phones
- Tablets, Portable Gaming Devices
- GPS, Active Speakers

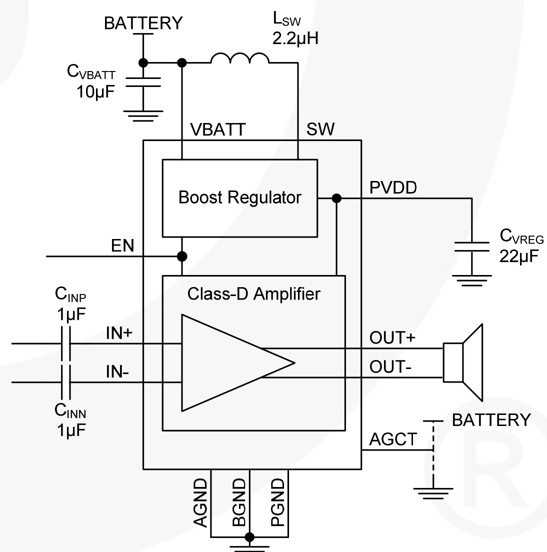


Figure 1. Typical Application Circuit

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAB3103UCX	-40°C to +85°C	12-Bump, 0.5mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	3000 Units on Tape & Reel

Pin Configuration

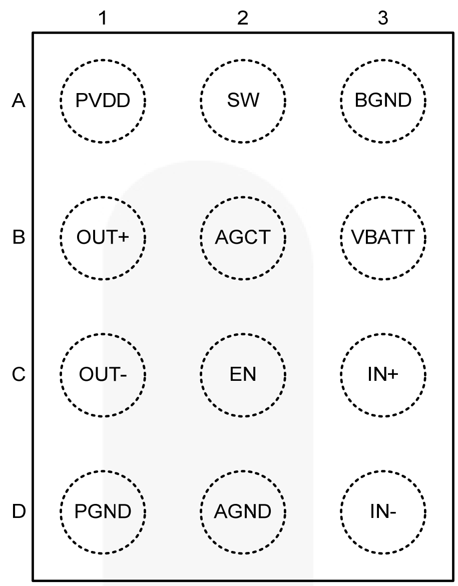


Figure 2. Pin Assignments (Top View)

Pin Definitions

WLCSP	Name	Type	Description
B1	OUT+	Output	Positive audio output
C1	OUT-	Output	Negative audio output
C3	IN+	Analog Input	Positive audio input
D3	IN-	Analog Input	Negative audio input
C2	EN	CMOS Input	Shutdown signal for boost regulator and amplifier: VBATT=enabled, PGND=shutdown (internal 300KΩ pull-down)
B2	AGCT	Analog Input	AGC trip-point setting
B3	VBATT	Power	Supply voltage
A2	SW	Power	Boost regulator switching node
A1	PVDD	Power	Boost regulator output
A3	BGND	Ground	Boost regulator ground – connect to PGND and AGND with a ground plane.
D1	PGND	Ground	Power ground – connect to BGND and AGND with a ground plane.
D2	AGND	Ground	Analog ground – connect to BGND and PGND with a ground plane.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{BATT}	Voltage on VBATT Pin	-0.3	6.0	V
V_{OUT}	Voltage on OUT-, OUT+ Pins	-0.3	V_{BSTOUT} + 0.3	V
V_{IN}	Voltage on IN+, IN-, SW, EN, AGCT Pins	-0.3	V_{BATT} + 0.3	V
V_{INDIFF}	Differential Voltage Across IN+, IN- Pins While Enabled	-1.5	1.5	V_{rms}
P_D	Power Dissipation		Internally Limited	

Dissipation Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature Range	-65		150	°C
T_L	Lead Temperature (Soldering, 10s)			300	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		77		°C/W

Electrostatic Discharge Protection

Symbol	Parameter	Condition	Level	Unit
ESD	Human Body Model (HBM)	EIA/JESD22-A114	±3	KV
	Charged Device Model (CDM)	According to "EIA/JESD22-C101 Level III" Compatible with "IEC61340-3-3 Level C4" or "ESD-STM5.3.1-1999 Level C4"	±1	KV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		85	°C
V_{BATT}	VBATT Supply Voltage Range	2.5		5.2	V
L_{SW}	Inductor (at Peak Inductor Current: 1.5A)	1.4[(1)]	2.2		µH
C_{VBATT}	VBATT Capacitor	4.7[(1)]	10.0		µF
C_{PVDD}	PVDD Capacitor	6.8[(1)]	22.0		µF
C_{AGCT}	Capacitive Load on AGCT			10	pF
R_L	Load Resistance	6[(2)]	8		Ω

Notes:

1. Capacitors experience degradation over time and this is accelerated with increased temperature. It is therefore recommended to use the stated typical values.
2. The FAB3103 is optimized to drive an 8Ω speaker impedance. The 8Ω speaker should remain at ≥6Ω over the entire audio frequency range.

Electrical Characteristics

Unless otherwise noted: AGCT=GND, R_L=8Ω + 33µH, f=1KHz, and audio measurement bandwidth=22Hz to 20KHz (AES17). Typical values are at V_{BATT}=3.6V, T_A=25°C, with typical external component values.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{DD}	Quiescent Current	Inputs AC Grounded, EN=HIGH			2.7		mA
I_{SD}	Shutdown Current	EN=PGND, Inputs AC Grounded			0.1	2.0	µA
t_{WU}	Wake-Up Time	From LOW to HIGH EN Transition to Full Operation			5	12	ms
$f_{SW(AMP)}$	Class-D Switching Frequency				300		KHz
V_{OS}	Differential Output Offset Voltage	Inputs AC Grounded			1.67	5.00	mV
A_V	Gain	AGC Inactive		9.5	10.0	10.5	V/V
R_{IN}	Input Resistance	Gain=10V/V (AGC Inactive)	Differential	24	30	36	KΩ
			Single-Ended	12	15	18	
R_{STD}	Single-Ended Input Impedance During Shutdown	EN=PGND, AC-Coupled Inputs, V_{INx} < 2V_{rms} per Input		80			KΩ
V_{STD}	Maximum Single-Ended Input Voltage Swing During Shutdown	EN=PGND, AC-Coupled Inputs		2			V_{rms}
	THD+N Added to Audio Signal at Inputs During Shutdown	EN=PGND, AC-Coupled Inputs, Source Impedance < 1Ω				0.02	%
THD+N	Total Harmonic Distortion Plus Noise	P_{OUT}=100mW			0.01		%
		P_{OUT}=500mW			0.02		
P_O	Output Power	THD+N ≤ 10%			2.3		W
		THD+N ≤ 1%			1.85		
I_{DLMT}	Class-D Output Current Limit				1.4		A
PSRR	Power Supply Rejection Ratio	Inputs Shorted, AC Grounded, Output Referred; V_{RIPPLE}=200mV_{P-P} Square Centered Around V_{BATT}=3.8V, 50% Duty Cycle, 10µs Rise/Fall Time	f_{RIPPLE}=1KHz, Boost Enabled		85		dB
			f_{RIPPLE}=217Hz, Boost Enabled		88		
			f_{RIPPLE}=1KHz, Boost Bypassed		77		
			f_{RIPPLE}=217Hz, Boost Bypassed		70		
CMRR	Common-Mode Rejection Ratio	Output Referred, V_{RIPPLE}=200m V_{P-P} Square, 50% Duty Cycle, 10µs Rise/Fall Time, Inputs Shorted and AC-Coupled to V_{RIPPLE}	f_{RIPPLE}=1KHz		75		dB
			f_{RIPPLE}=217Hz		71		
V_{BIAS}	IN+, IN- Bias Voltage				1.2		V
η	Efficiency	R_L=8Ω + 33µH , P_{OUT}=1.0W			85		%
SNR	Signal-To-Noise Ratio	P_{OUT}=1.85W, A-Weighted			100		dB
		P_{OUT}=1.85W, Unweighted			97		

Continued on the following page...

Electrical Characteristics

Unless otherwise noted: AGCT=GND, R_L=8Ω + 33μH, f=1KHz, and audio measurement bandwidth=22Hz to 20KHz (AES17). Typical values are at V_{BATT}=3.6V, T_A=25°C, with typical external component values.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Output Noise	A-Weighted		38		μV_{rms}
		Unweighted		51		
T_{STD}	Thermal Shutdown	Junction Temperature		165		°C
T_{HYS}	Thermal Shutdown Hysteresis	Junction Temperature		25		°C
V_{ULVO}	V_{BATT} Under-Voltage Shutdown		1.8	2.1	2.3	V
V_{HYS}	V_{BATT} Under-Voltage Hysteresis			120	300	mV
$f_{SW(REG)}$	Boost Converter Switching Frequency			1.2		MHz
$I_{LIMIT(SU)}$	Boost Converter Inrush Current Limit	PV_{DD} Rising from 0V to V_{BATT}			600	mA
t_{INRUSH}	Boost Converter Inrush Time	PV_{DD} Rising from 0V to V_{BATT}			1000	μs
	Auto Boost Startup Current Ramp Rate	PV_{DD} Rising from V_{BATT} to 5.6V		15		mA/μs
I_{BOOST}	Boost Converter Peak Input Current Limit	Open-Loop Limit	1100	1600	2100	mA
V_{BSTOUT}	Boost Converter Output Voltage		5.55	5.65	5.75	V
V_{BSTSTD}	Auto Boost Shutdown Threshold Voltage			2		V_{pk}
t_{HOLD}	Auto Boost Shutdown Hold Time			125		ms
V_{AGC}	AGC Trip Point	AGCT=Floating	3.190	3.250	3.283	V
		AGCT=GND	3.480	3.550	3.586	
		AGCT=VBATT	3.680	3.750	3.788	
	Output Power with AGC	AGCT=GND, V_{IN}=0.4V_{pk}, 1KHz Sine Wave; V_{BATT}=3.4V		0.79		W
		AGCT=GND, V_{IN}=0.4V_{pk}, 1KHz Sine Wave; V_{BATT}=3.0V		0.45		
t_A	AGC Attack Time			20		μs/dB
t_R	AGC Release Time			1600		ms/dB
	AGC Step Size			0.5		dB
	AGC Maximum Attenuation			10		dB
V_{IH}	EN Logic Input High Voltage		1.1			V
V_{IL}	EN Logic Input Low Voltage				0.45	V
C_{IN}	EN Capacitance			10		pF
R_{PD}	EN Pull-Down Resistance			300		KΩ

Typical Performance Characteristics

Unless otherwise noted: AGCT = GND, R_L = 8Ω + 33μH, f = 1KHz, audio measurement bandwidth 22Hz to 20KHz (AES17), V_{BATT} = 3.6V, T_A = 25°C, typical external component values.

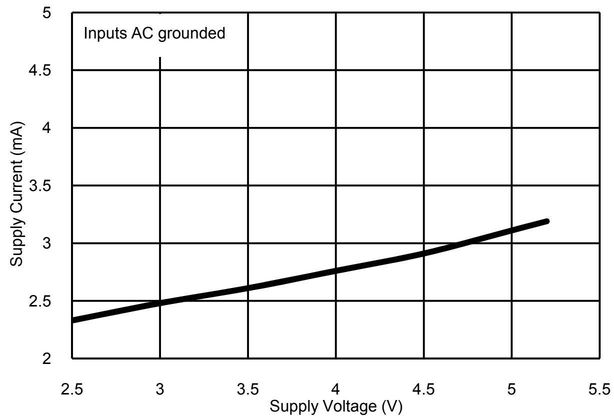


Figure 3. Quiescent Supply Current vs. Supply Voltage

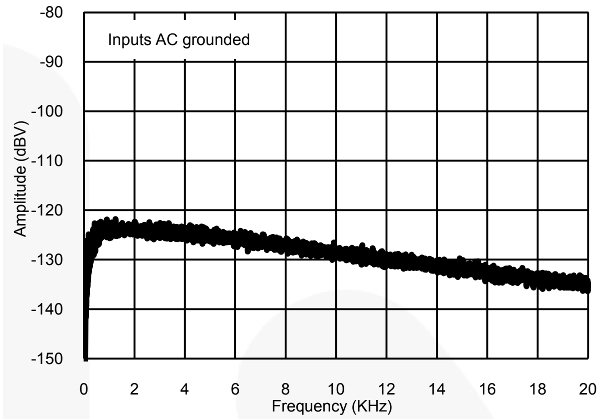


Figure 4. A-Weighted Output Noise vs. Frequency

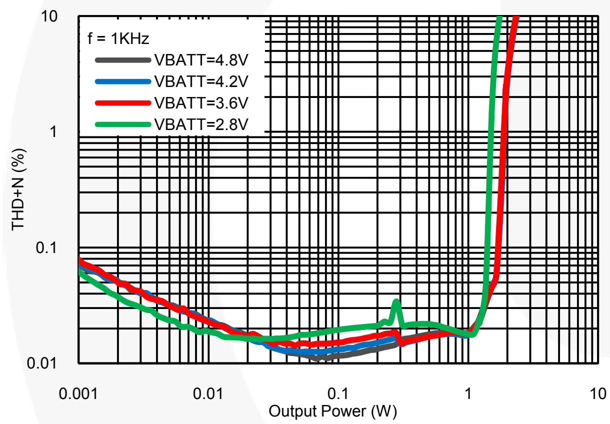


Figure 5. Total Harmonic Distortion + Noise vs. Output Power

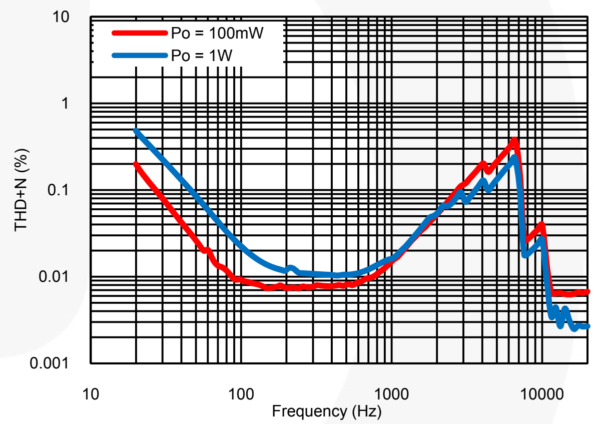


Figure 6. Total Harmonic Distortion + Noise vs. Frequency

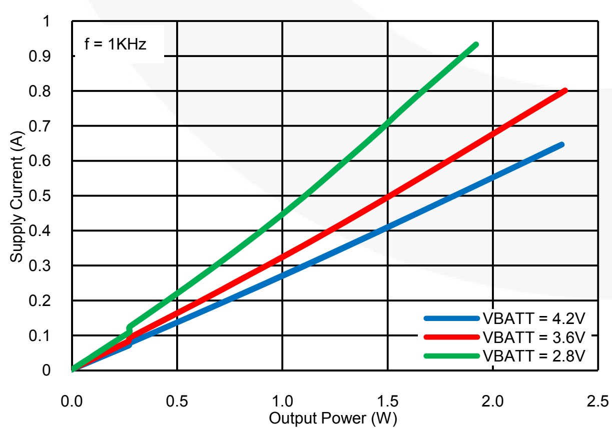


Figure 7. Supply Current vs. Output Power

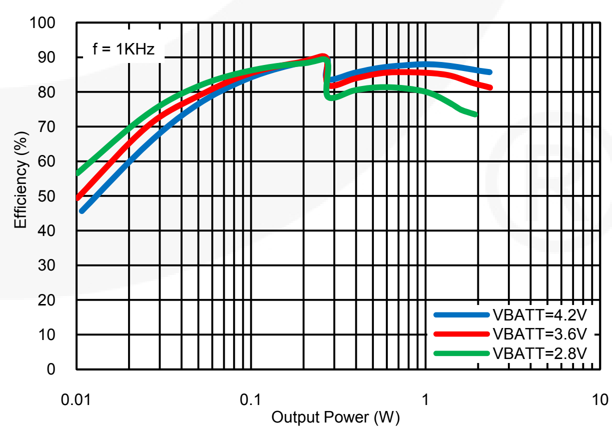


Figure 8. Efficiency vs. Output Power

Detailed Description

Signal Path

The FAB3103 features a fully differential signal path for noise rejection. The low-EMI design allows the OUT+ and OUT- pins to be connected directly to a speaker without an output filter.

The input section includes an 80KHz low-pass filter for removing out-of-band noise from audio sources, such as sigma delta DACs.

Shutdown

If EN is grounded, the Class-D amplifier and the boost regulator are turned off. IN+ and IN- are high impedance. Audio signals present at IN+ and IN- with amplitude less than the maximum differential input voltage swing are not distorted by the FAB3103 (*see Electrical Characteristics*).

When EN transitions from LOW to HIGH during the wake-up time *(see Electrical Characteristics),* the FAB3103 charges the input DC blocking capacitors to the Common Mode voltage before enabling the Class-D amplifier. To minimize click and pop during turn-on, audio signals should not be present during the wake-up period. Other devices that are connected to the same input signal, if not muted, may experience a pop due to this capacitor charging.

There is no limitation on the length of shutdown. Remaining charge on the PVDD capacitor at startup (for example, if EN is LOW for only a short period) does not affect startup behavior.

The EN pin has an internal 300KΩ pull-down resistor. EN must be LOW when V_{BATT} is lower than the V_{BATT} under-voltage shutdown voltage *(see Electrical Characteristics)*. EN must remain LOW for at least 100µs after V_{BATT} rises above the V_{BATT} under-voltage shutdown voltage.

Class-D Amplifier Over-Current Protection

If the output current of the Class-D amplifier exceeds limits *(see the Electrical Characteristics)*, the amplifier is disabled for approximately one second. (Other systems, such as the boost regulator and AGC, remain active.) After one second, the amplifier is re-enabled. If the fault condition still exists, the amplifier is disabled again. This cycle repeats until the fault condition is removed.

Speaker Size

The FAB3103 was designed for use with small speakers found in mobile applications. The back EMF in larger speakers can cause PVDD to peak above safe levels. To check safe operation, monitor PVDD while driving a dynamic signal (such as music) at maximum levels. If PVDD peaks above 6.2V, connect a 6V Zener diode between PVDD and PGND.

Low EMI

To minimize EMI, edge-rate control for the boost regulator and Class-D amplifier can be employed.

The boost regulator's edge-rate control is disabled by default. For devices with 20ns boost edge rates or 10ns boost edge rates, contact a Fairchild Representative. This is a factory option that cannot be changed in the application, but is available from Fairchild.

The Class-D amplifier's edge-rate control is disabled by default. For devices with 20ns Class-D edge rates, contact a Fairchild Representative. This is a factory option that cannot be changed in the application, but is available from Fairchild..

Automatic Boost Shutdown

Automatic boost shutdown changes the Class-D amplifier supply voltage as a function of audio output level. At audio output levels above $2V_{pk}$, the boost converter generates 5.65V from the input battery voltage. If the output level is below $2V_{pk}$ for more than 125ms, the boost converter is switched off and the Class-D amplifier is supplied directly from the battery. As a result, efficiency is improved at low audio output levels and quiescent current consumption is reduced.

Figure 9 shows an example of an auto boost startup event. At first, the boost converter is off and PVDD is the same voltage as VBATT. At 20µs, a large audio signal is presented at the inputs, which causes the boost converter to start up. From 20µs to 120µs, battery current is ramped up. The auto boost startup current ramp rate is 15mA/µs. This ramp is enforced to avoid sudden current draw spikes from the battery.

At 120µs, after PV_{DD} has reached the Boost Converter Output Voltage, the ramp is released and battery current falls to a level capable of sustaining the speaker amplifier's outputs. At 160µs, the input signal begins to rise, which increases battery current. At 180µs, the boost converter peak input current limit is enforced and battery current levels off, which causes PV_{DD} to droop.

The boost regulator should not be used to drive any loads other than the Class-D amplifier.

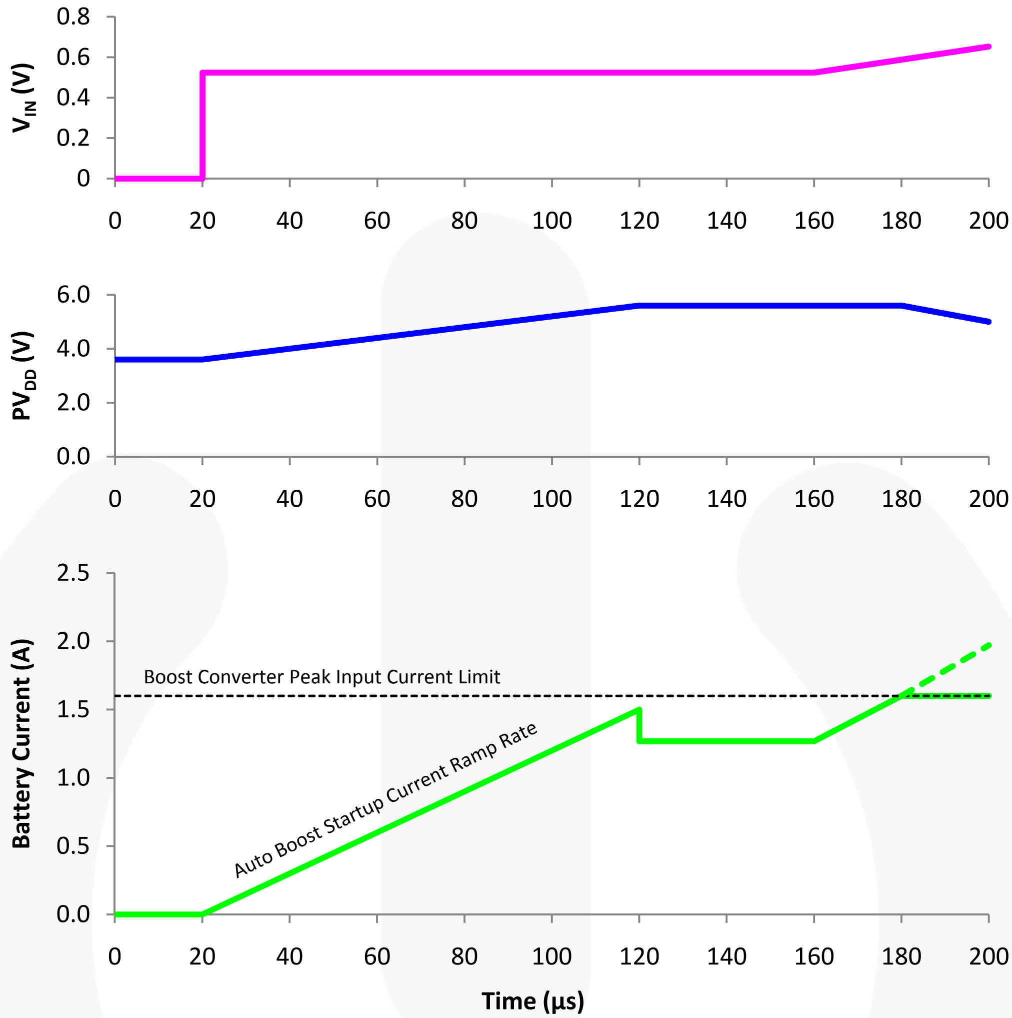


Figure 9. Auto Boost Startup

Automatic Gain Control

Due to constant output power, the amount of VBATT current needed to maintain a given output amplitude is inversely proportional to VBATT voltage. This produces very large current requirements at low V_{BATT}. The AGC eases low-V_{BATT} current demands by reducing the gain when VBATT voltage drops below a trip point. One of three different trip points may be selected by shorting AGCT to VBATT, shorting AGCT to PGND, or floating *AGCT (see Electrical Characteristics)*.

The trip point is determined upon power-on and when EN transitions from LOW to HIGH. If AGCT is changed during operation, the new value is not read until power or EN is cycled.

When V_{BATT} is above the trip point, the AGC has no effect on the signal path.

When V_{BATT} is at or below the trip point, target gain is reduced in 0.5dB steps according to the equation:

$$G_{target} = G_I - S_L G_I \left(\frac{V_T - V_{batt}}{V_{out\,max}} \right) \quad (1)$$

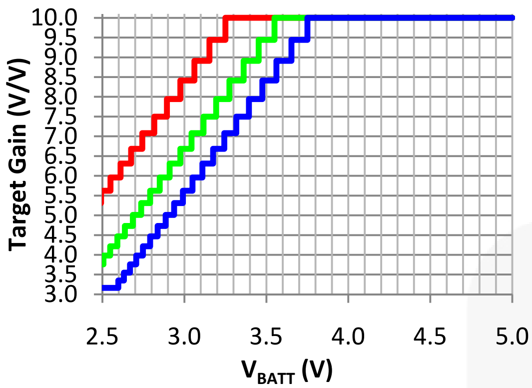
where:

G_I = Initial gain (10V/V);
S_L = 3V/V slope;
V_{OUTMAX} = 5.2V;
V_T = AGC trip point set by the AGCT pin; and
V_{BATT} = Voltage at the VBATT pin.

Target gain can be reduced by as much as 10dB.

Note that the state of auto boost shutdown has no effect on the AGC.

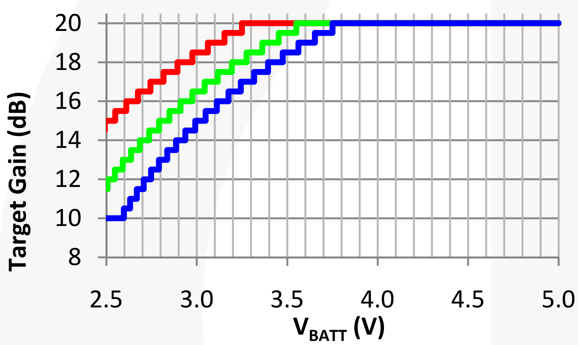
Figure 10 shows target gain vs. battery voltage.



Line Color	AGCT Configuration	AGC Trip Point (V)
Red	Float	3.25
Green	Ground	3.55
Blue	V_{BATT}	3.75

Figure 10. Target Gain vs. Battery Voltage

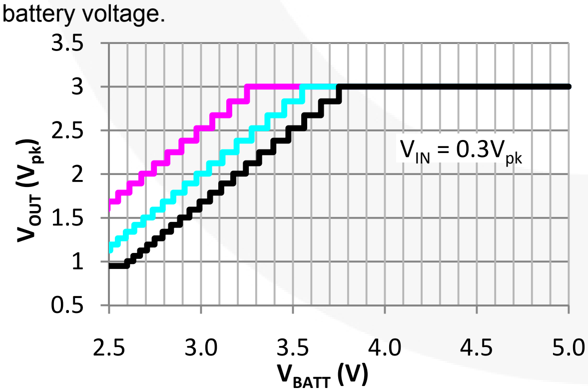
Figure 11 is similar to Figure 10 except that the target gain is expressed in dB rather than V/V.



Line Color	AGCT Configuration	AGC Trip Point (V)
Red	Float	3.25
Green	Ground	3.55
Blue	V_{BATT}	3.75

Figure 11. Target Gain vs. Battery Voltage

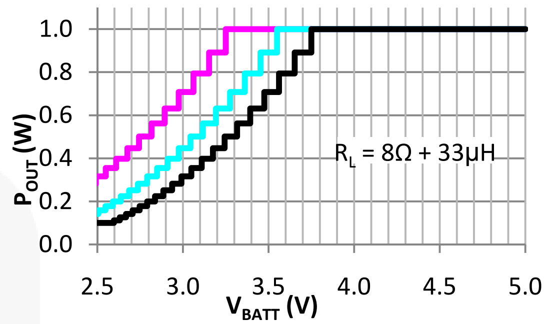
Figure 12 shows examples of peak output voltage vs. battery voltage.



Line Color	AGCT Configuration	AGC Trip Point (V)	Input Voltage (V_{pk})
Magenta	Float	3.25	0.3
Cyan	Ground	3.55	0.3
Black	V_{BATT}	3.75	0.3

Figure 12. Output Voltage vs. Battery Voltage

Figure 13 shows examples of output power vs. battery voltage with a 0.4V_{pk} sinusoidal input signal.



Line Color	AGCT Configuration	AGC Trip Point (V)	Input Voltage (V_{pk})
Magenta	Float	3.25	0.3
Cyan	Ground	3.55	0.3
Black	V_{BATT}	3.75	0.3

Figure 13. Output Power vs. Battery Voltage Examples (V_{IN}=0.4V_{pk} Sine)

The speed at which gain can change is limited *(see Electrical Characteristics)*; therefore, the actual gain may lag the target gain if V_{BATT} voltage changes quickly.

Figure 14 and Figure 15 show examples of AGC changes over time. In these examples, AGCT is grounded, so the AGC trip point is 3.55V.

1. Initially, V_{BATT} is 3.6V and gain is 10V/V (20dB).
2. A narrow V_{BATT} drop of less than 2µs is ignored by the AGC.
3. The next V_{BATT} drop lasts longer and the AGC is tripped. The initial 0.5dB gain reduction occurs 3.9µs after V_{BATT} crosses below the 3.55V trip point.
4. V_{BATT} is now 3.1V, so target gain is 10V/V – 3V/V × 10V/V × [(3.55V – 3.1V) / 5.2V]=7.40V/V=17.4dB.
5. Gain continues to drop by 0.5dB every 10µs until it is below the target gain, where it settles at 17.0dB.
6. When V_{BATT} rises above the trip point, gain increases by 0.5dB. If more than 800ms has passed since the last gain change, gain rises immediately, as shown in Figure 14. Otherwise, gain does not rise until after 800ms has passed, as shown in Figure 15.
7. While V_{BATT} remains above the trip point, gain continues to increase by 0.5dB every 800ms until it returns to 20dB.

The intent of the AGC circuitry is to limit current draw from the battery to extend runtime. This is particularly important for handsets that incorporate advanced shutdown algorithms to measure battery voltage. The AGC circuit dynamically adjusts the amplifier gain based on the trip point used. Even though the amplifier gain is reduced in response to lower battery voltages, two conditions result in continued higher current draw: 1) the handset volume is turned up in an attempt to maintain the same loudness, or 2) the input signal is increased. If one or both of these conditions exist, even though the amplifier gain is reduced in response to lower battery voltage, current draw remains elevated, eventually resulting in handset shutdown.

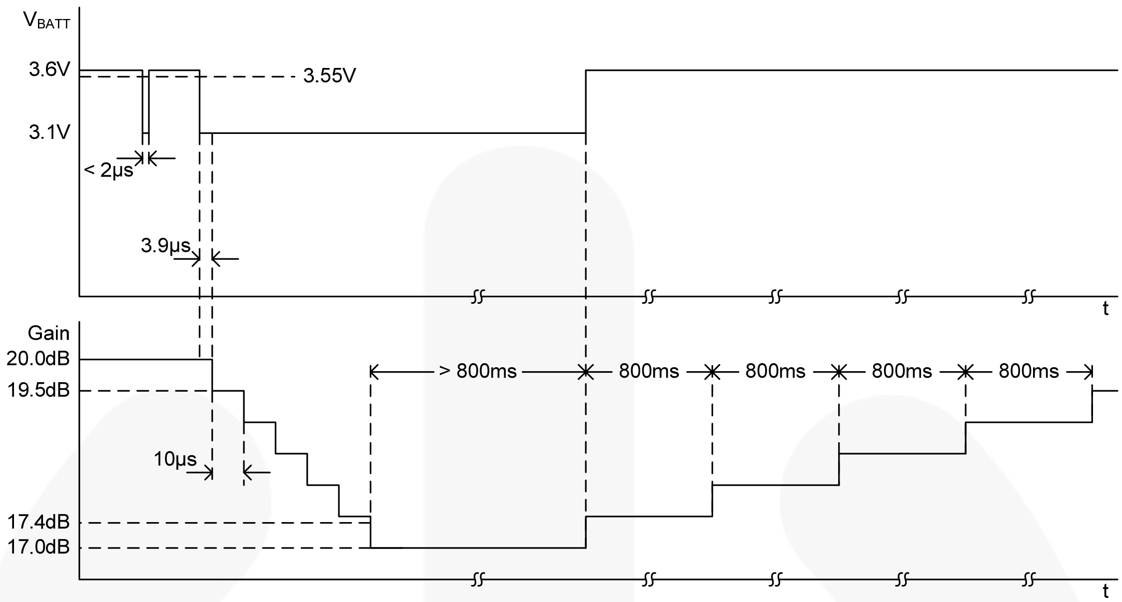


Figure 14. AGC Changes vs. Time, Example 1

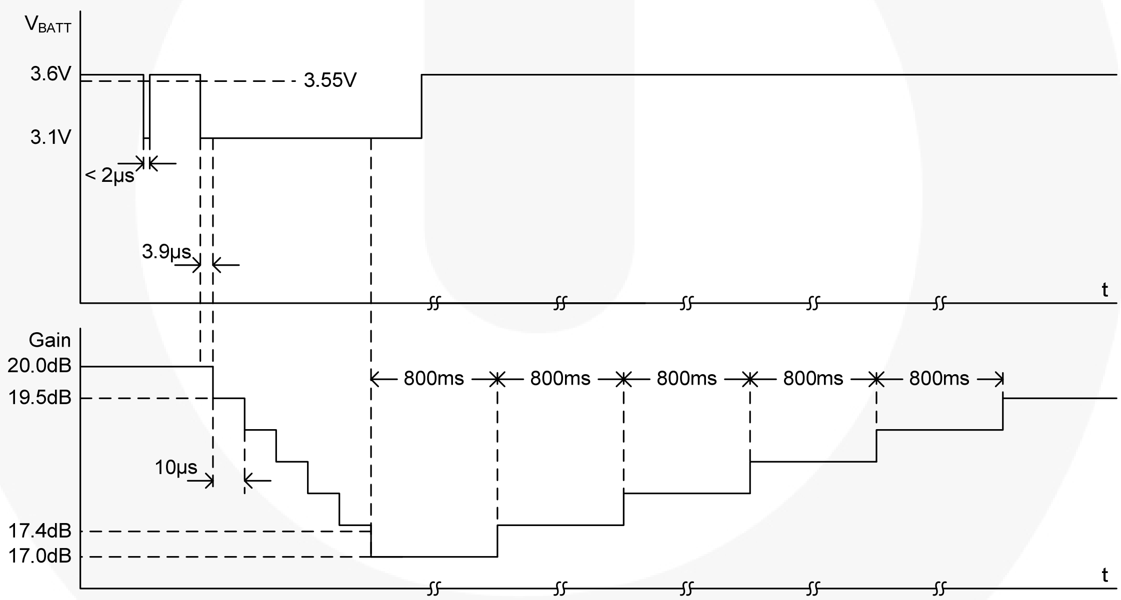


Figure 15. AGC Changes vs. Time, Example 2

Applications Information

Layout Considerations

General layout and supply bypassing play a major role in analog performance and thermal characteristics. Fairchild offers an evaluation board to guide layout and aid device evaluation. Contact a Fairchild representative for information about evaluation boards. Following the recommended layout configuration (shown in Figure 16) provides optimum performance for the device. For best results, follow the steps and recommended routing rules listed below.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Traces must run on top of the ground plane.
- Avoid routing at 90° angles.
- Place bypass capacitors within 2.54mm (0.1 inches) of the device power pin.
- Minimize all trace lengths to reduce series inductance.
- Connect BGND, PGND, and AGND together using a single ground plane.

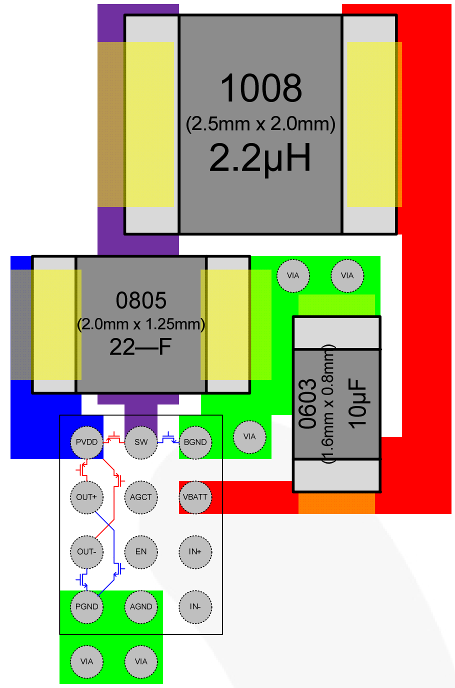


Figure 16. Recommended PCB Layout

Table 1 – Recommended Passive Components

Component	Vendor	Part Number	Value
L_{SW}	Murata	LQM2HPN2R2NJCL	2.2µH
C_{PVDD}	Murata	GRM21AR60J226UE80K	22µF
C_{VBATT}	Murata	GRM188R60J106UE82J	10µF

Physical Dimensions

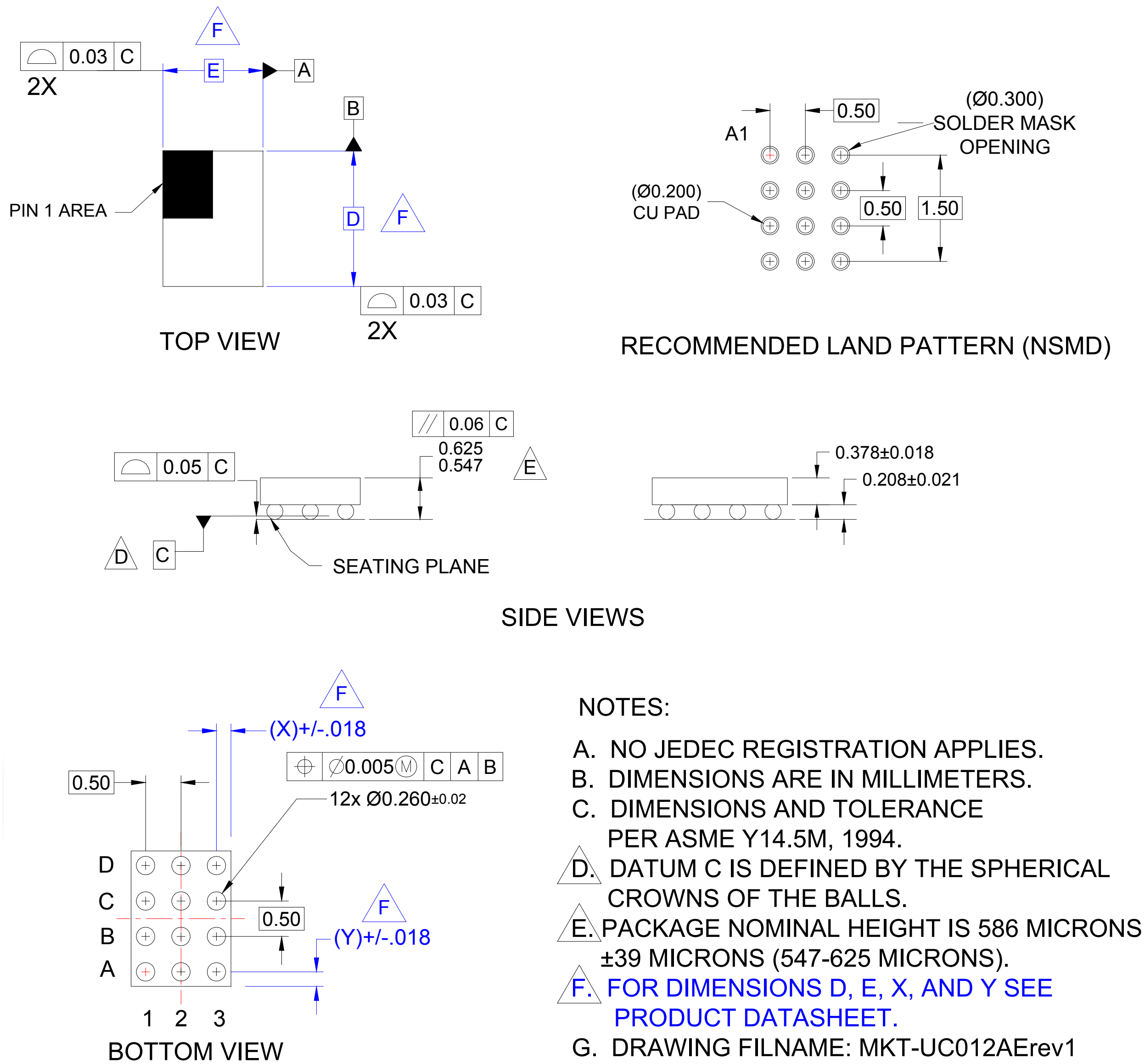


Figure 17. 12-Ball WLCSP, 3x4 Array, 0.5mm Pitch, 250µm Ball

Product Dimensions

Product	D	E	X	Y
FAB3103UCX	1.86mm	1.44mm	0.22mm	0.18mm

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