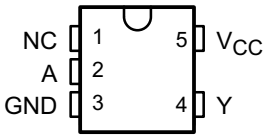
SINGLE SCHMITT-TRIGGER INVERTER GATE

Check for Samples: SN74AHCT1G14

FEATURES

- **Operating Range 4.5-V to 5.5-V**
- **Max t_{pd} of 8 ns at 5-V**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±8-mA Output Drive at 5-V**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DBV OR DCK PACKAGE
(TOP VIEW)



NC – No internal connection

See mechanical drawings for dimensions.

DESCRIPTION

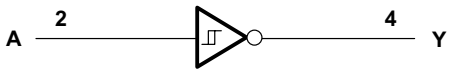
description/ordering information The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function $Y = \overline{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

FUNCTION TABLE

INPUTS	OUTPUT
A	Y
H	L
L	H

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range, V_{CC}		–0.5 to 7	V
Input voltage range, V_I(2)		–0.5 to 7	V
Output voltage range, V_O(2)		–0.5 to V_{CC} + 0.5	V
Input clamp current, I_{IK} (V_I < 0)		–20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})		±20	mA
Continuous output current, I_O (V_O = 0 to V_{CC})		±25	mA
Continuous current through V_{CC} or GND		±50	mA
Package thermal impedance, θ_{JA}(3)	DBV package	206	°C/W
	DCK package	252	
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		Recommended T_A = –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		4.5 V	0.9		2	0.9		0.9	2.0	V
		5.5 V	1.1		2	1.1		1.1	2.0	
$V_{T–}$ Negative-going input threshold votlage		4.5 V	0.5		1.6	0.5		0.5	1.6	V
		5.5 V	0.6		1.5	0.6		0.6	1.5	
ΔV_T Hysteresis ($V_{T+} – V_{T–}$)		4.5 V	0.4		1.4	0.4		0.4	1.4	V
		5.5 V	0.5		1.6	0.4		0.5	1.6	
V_{OH}	I_{OH} = –50 mA	4.5 V	4.4	4.5		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.88		3.7		
V_{OL}	I_{OL} = 50 mA	4.5 V			0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			1		10		10	µA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10		10	pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

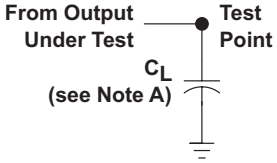
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C		T_A = –40°C to 85°C		Recommended T_A = –40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF	4	7	1	8	1	9	ns
t_{PHL}				4	7	1	8	1	9	
t_{PLH}	A	Y	C_L = 50 pF	5.5	8	1	9	1	10	ns
t_{PHL}				5.5	8	1	9	1	10	

OPERATING CHARACTERISTICS

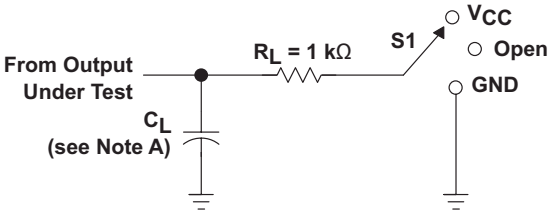
V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION

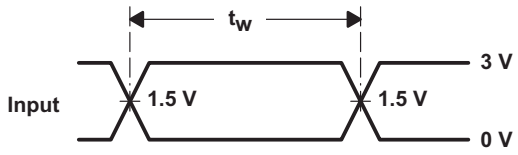


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

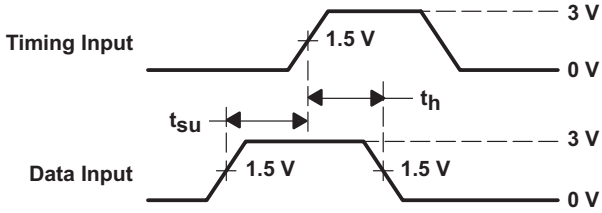


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

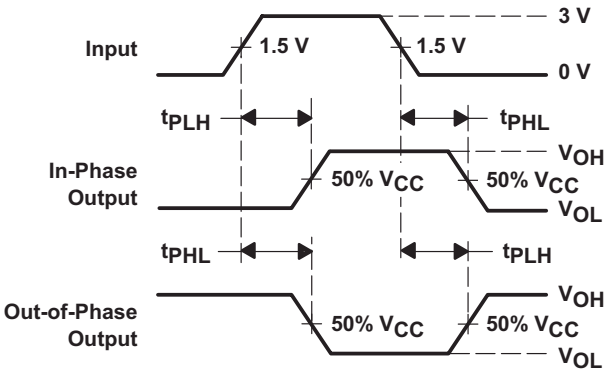
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



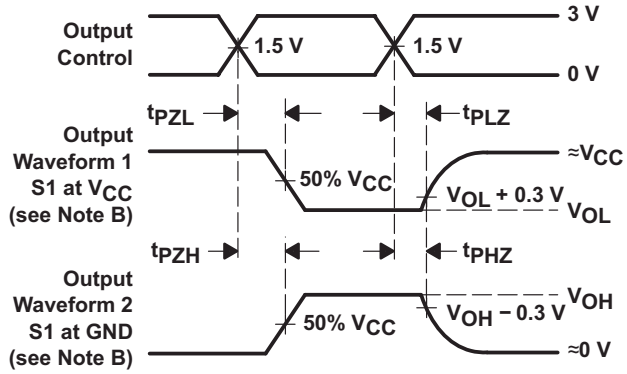
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision O (January 2003) to Revision P	Page
• Changed document format from Quicksilver to DocZone.	1
• Extended operating temperature range to 125°C	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHCT1G14DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B14G	Samples
74AHCT1G14DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B14G	Samples
74AHCT1G14DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BF3	Samples
74AHCT1G14DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BF3	Samples
SN74AHCT1G14DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(B143, B14G, B14J, B14L, B14S)	Samples
SN74AHCT1G14DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(B143, B14G, B14J, B14L, B14S)	Samples
SN74AHCT1G14DCK3	ACTIVE	SC70	DCK	5	3000	Pb-Free (RoHS)	SNBI	Level-1-260C-UNLIM	-40 to 125	BFY	Samples
SN74AHCT1G14DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BF3, BFG, BFJ, BFL, BFS)	Samples
SN74AHCT1G14DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BF3, BFG, BFJ, BFL, BFS)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

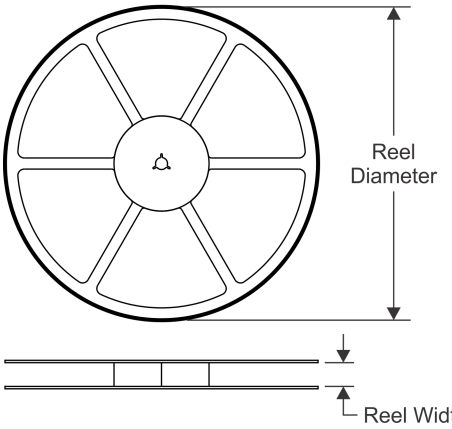
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

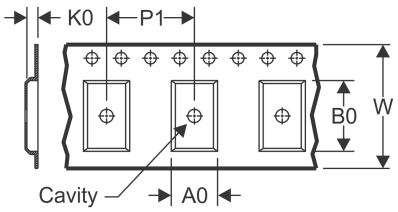
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

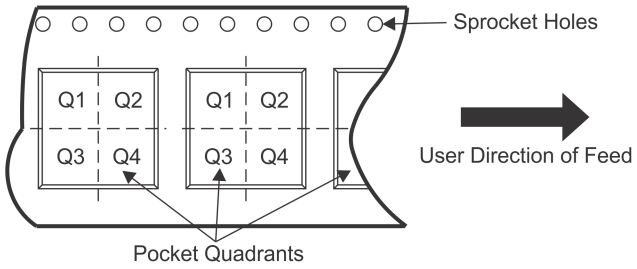


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

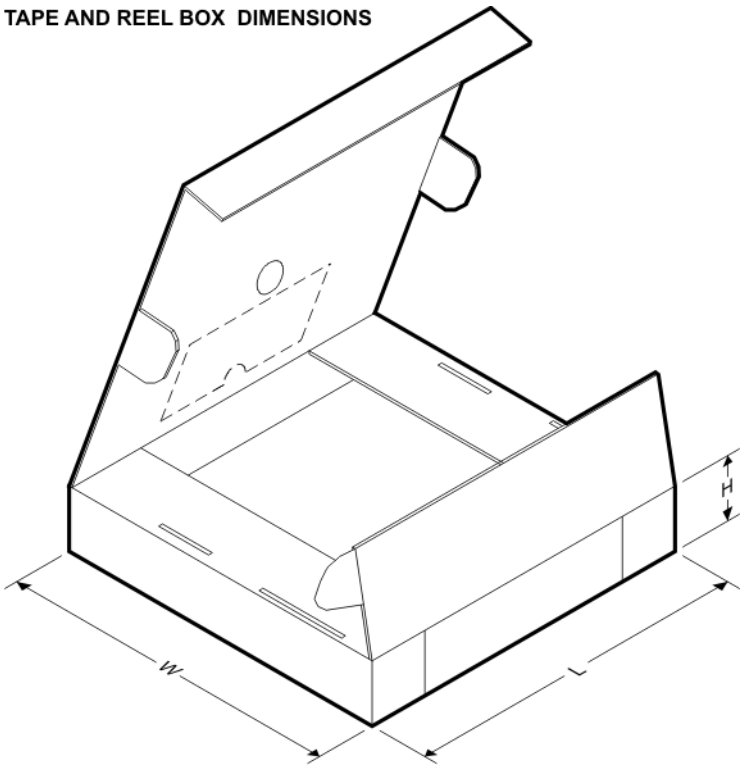
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G14DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G14DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G14DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G14DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHCT1G14DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G14DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G14DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G14DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

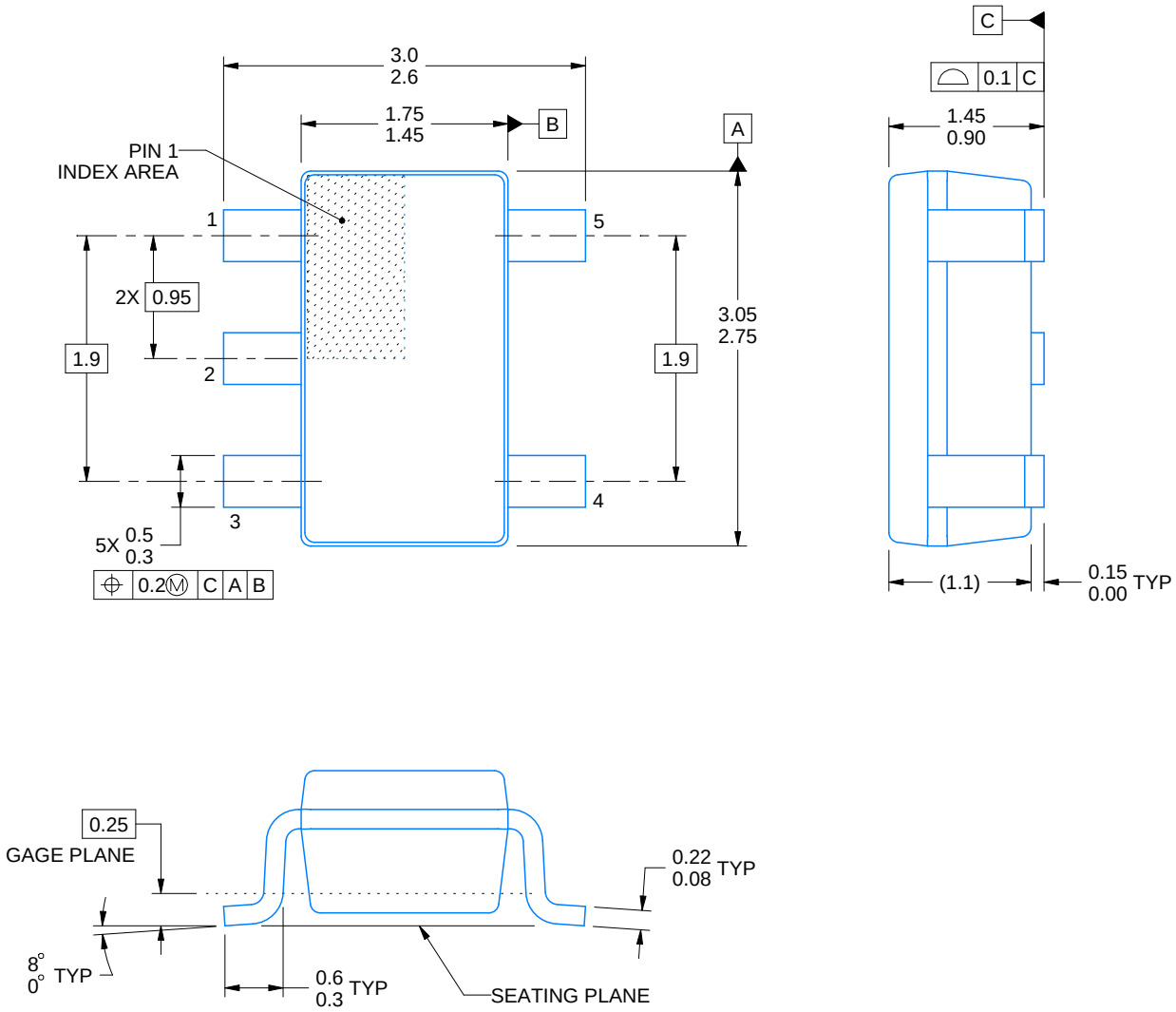
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G14DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G14DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHCT1G14DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHCT1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHCT1G14DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G14DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AHCT1G14DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G14DCKT	SC70	DCK	5	250	202.0	201.0	28.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

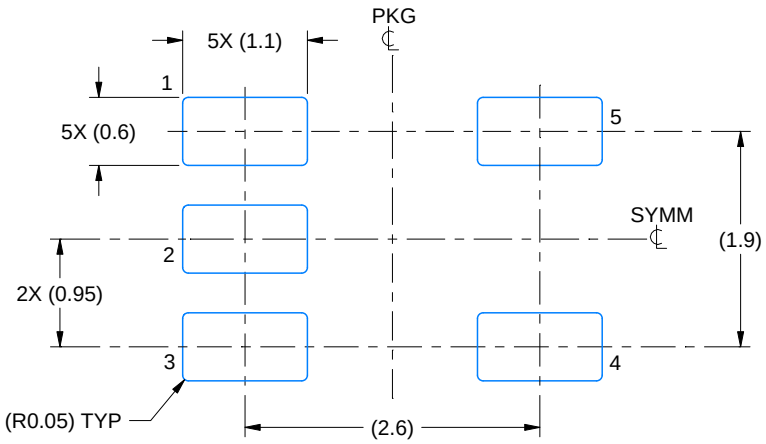
SMALL OUTLINE TRANSISTOR



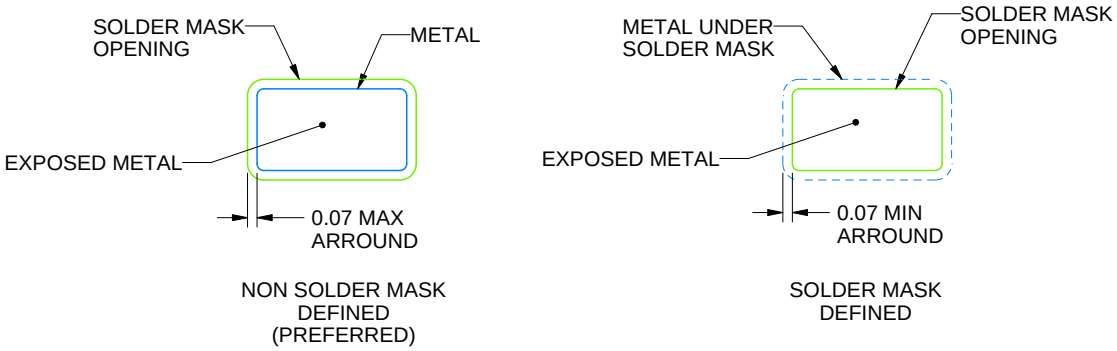
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

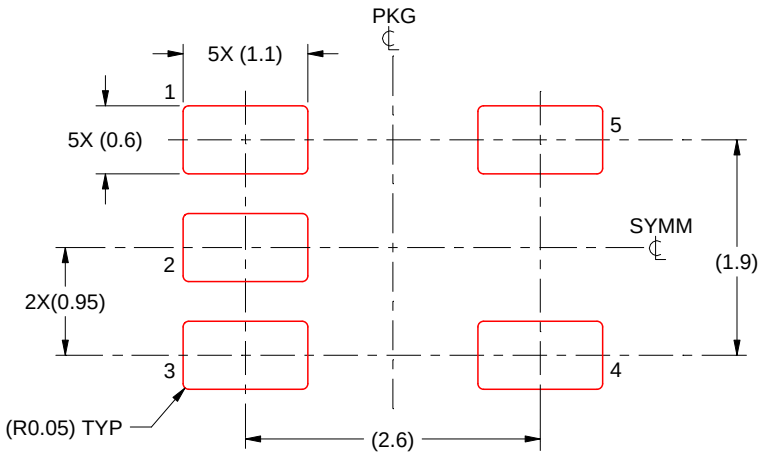


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



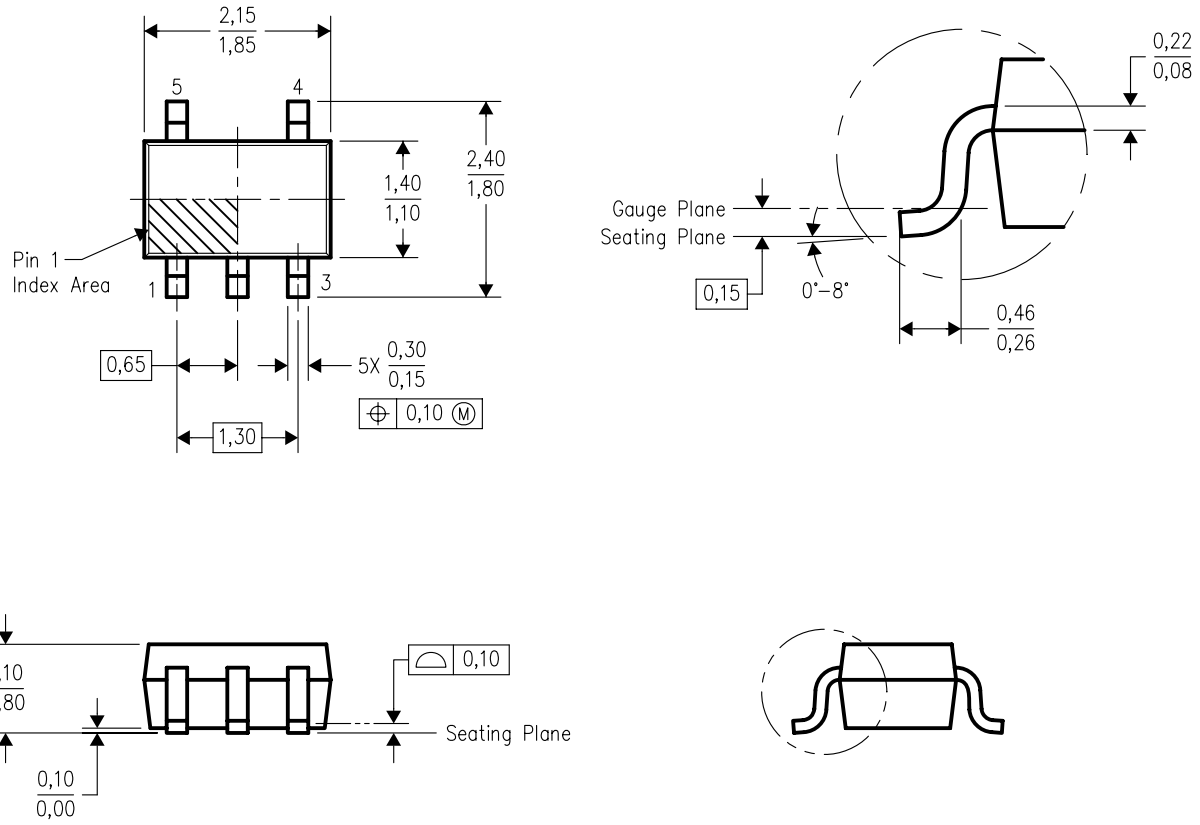
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

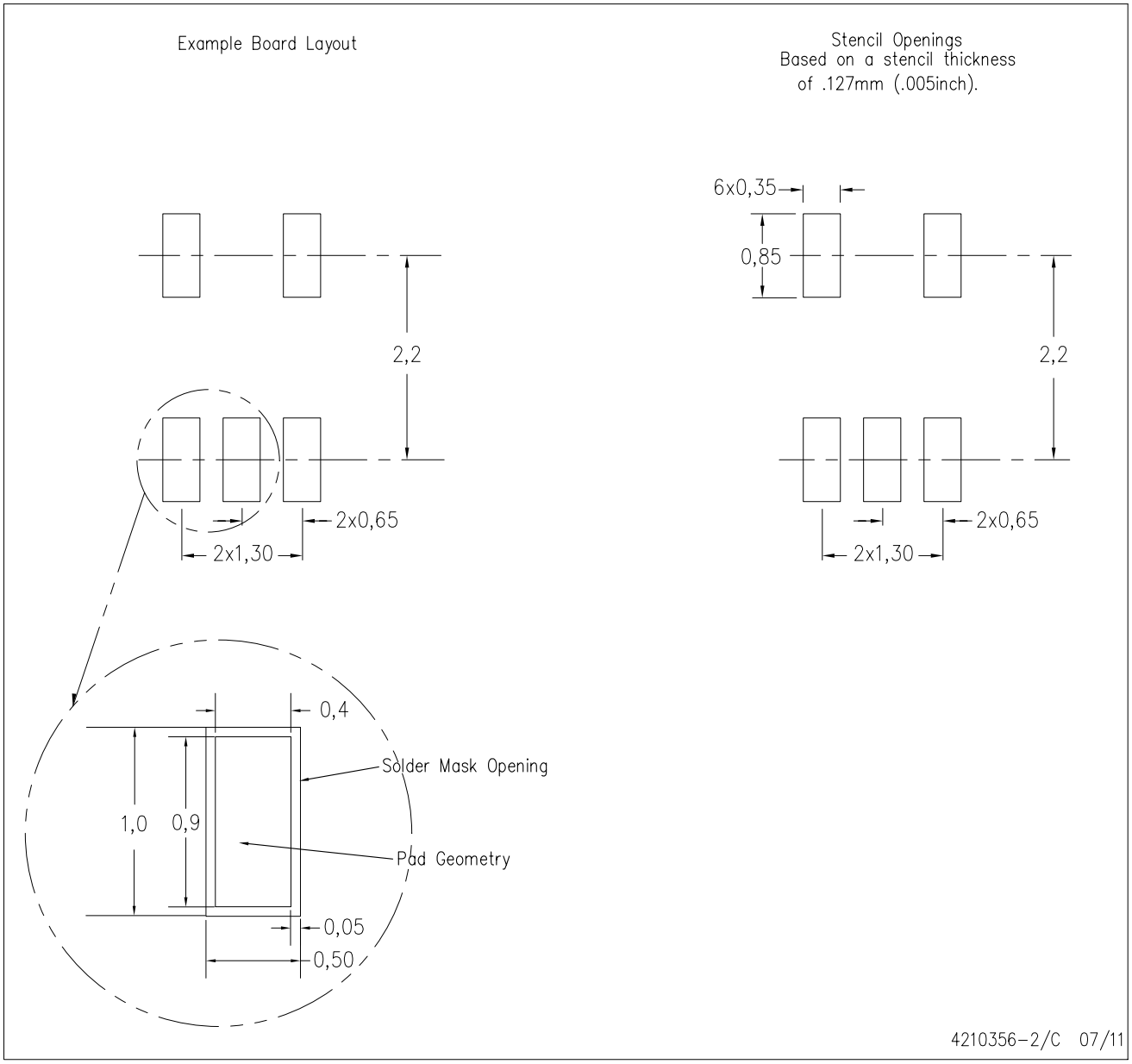
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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