LP2981-N Micropower 100-mA Ultralow Dropout Regulator in SOT-23 Package

1 Features

- Operating Input Voltage Range: 2.1 V to 16 V
- Ultralow-Dropout Voltage
- Output Voltage Accuracy 0.75% (A Grade)
- Specified 100-mA Output Current
- < 1-µA Quiescent Current when Shutdown
- Low Ground Pin Current at All Load Currents
- High Peak Current Capability (300 mA Typical)
- Wide Supply Voltage Range (16 V Maximum)
- Fast Dynamic Response to Line and Load
- Low Z_{OUT} Over Wide Frequency Range
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

2 Applications

- Cellular Phones
- Palmtop and Laptop Computers
- Personal Digital Assistants (PDA)
- Camcorders, Personal Stereos, Cameras

3 Description

The LP2981-N is a 100-mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications.

Using an optimized Vertically Integrated PNP (VIP) process, the LP2981-N delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 200 mV at 100-mA load, and 7 mV at 1-mA load.

Ground Pin Current: Typically 600 µA at 100-mA load, and 80 µA at 1-mA load.

Sleep Mode: Less than 1-µA quiescent current when ON/$\overline{\text{OFF}}$ pin is pulled low.

Precision Output: 0.75% tolerance output voltages available (A grade).

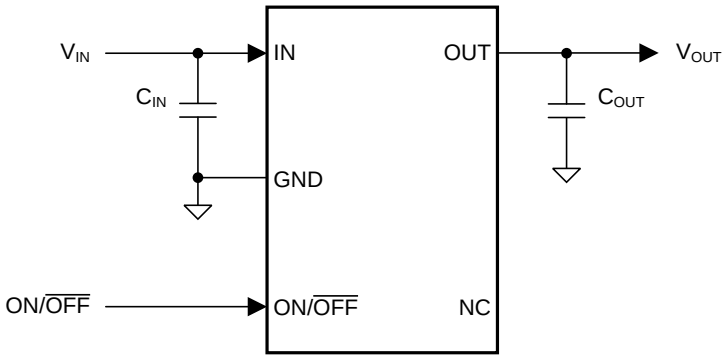
Assorted voltage options, from 2.5 V to 5 V, are available as standard products.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2981-N	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (September 2015) to Revision N — **Page**

- Changed update typical application drawing and change pin names from Vin, Vout to IN and OUT ... 1

Changes from Revision L (June 2015) to Revision M — **Page**

- Changed split out ESD values by specific pins ... 4
- Changed correct junction-to-case and junction-to-board values (typo from last format update) ... 5

Changes from Revision K (April 2013) to Revision L — **Page**

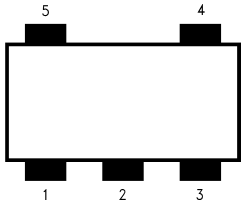
- Changed "Nine" to "Assorted" ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed text of NC pin description ... 3
- Changed thermal value in footnote 3 ... 4
- Changed thermal values to TI measure ... 5

Changes from Revision J (January 2009) to Revision K — **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN	I	Input voltage pin
2	GND	—	Common ground (device substrate)
3	ON/OFF	I	Logic high enable input
4	NC	—	DO NOT CONNECT. Device pin 4 is reserved for post packaging test and calibration of the LP2989 VOUT accuracy. Device pin 2 must be left floating. Do not connect to any potential. Do not connect to ground. Any attempt to do pin continuity testing on device pin 2 is discouraged. Continuity test results will be variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 2 may activate the trim circuitry forcing VOUT to move out of tolerance.
5	OUT	O	Regulated output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Power dissipation(3)	Internally limited		
Input supply voltage (survival)	−0.3	16	V
Input supply voltage (operating)	2.1	16	V
Shutdown input voltage (survival)	−0.3	16	V
Output voltage (survival)(4)	−0.3	9	V
I_{OUT} (survival)	Short-circuit protected		
Input-output voltage (survival)(5)	−0.3	16	V
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace-specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$. The value of $R_{\theta JA}$ for the SOT-23 package is 175.7°C/W. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2980-N output must be diode-clamped to ground.
(5) The output PNP structure contains a diode between the IN and OUT pins that is normally reverse-biased. Reversing the polarity from V_{IN} to V_{OUT} will turn on this diode (See *Reverse Current Path*).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 1, 2 and 5	±2000	V
			Pins 3 and 4	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating junction temperature	−40	125	°C
Input supply voltage (operating)	2.1	16	V

6.4 Thermal Information

THERMAL METRIC[1]		LP2981-N DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High-K	175.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.[1]

PARAMETER		TEST CONDITIONS	LP2981AI-XX[2]			LP2981I-XX[2]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_O	Output voltage tolerance	I_L = 1 mA	−0.75		0.75	−1.25		1.25	$\%V_{NOM}$
		1 mA < I_L < 100 mA	−1		1	−2		2	
		1 mA < I_L < 100 mA –40°C ≤ T_J ≤ 125°C	−2.5		2.5	−3.5		3.5	
$\Delta V_O/\Delta V_{IN}$	Output voltage line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V		0.007	0.014		0.007	0.014	%/V
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V –40°C ≤ T_J ≤ 125°C			0.032			0.032	
$V_{IN} – V_O$	Dropout voltage[3]	I_L = 0 mA		1	3		1	3	mV
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C			5			5	
		I_L = 1 mA		7	10		7	10	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C			15			15	
		I_L = 25 mA		70	100		70	100	
		I_L = 25 mA, –40°C ≤ T_J ≤ 125°C			150			150	
		I_L = 100 mA		200	250		200	250	
		I_L = 100 mA, –40°C ≤ T_J ≤ 125°C			375			375	
I_{GND}	Ground pin current	I_L = 0 mA		65	95		65	95	µA
		I_L = 0 mA, –40°C ≤ T_J ≤ 125°C			125			125	
		I_L = 1 mA		80	110		80	110	
		I_L = 1 mA, –40°C ≤ T_J ≤ 125°C			170			170	
		I_L = 25 mA		200	300		200	300	
		I_L = 25 mA, –40°C ≤ T_J ≤ 125°C			550			550	
		I_L = 100 mA		600	800		600	800	
		I_L = 100 mA, –40°C ≤ T_J ≤ 125°C			1500			1500	
		$V_{ON/\overline{OFF}}$ < 0.3 V		0.01	0.8		0.01	0.8	
		$V_{ON/\overline{OFF}}$ < 0.15 V –40°C ≤ T_J ≤ 125°C		0.05	2		0.05	2	

(1) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1-V differential.

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.(1)

PARAMETER		TEST CONDITIONS	LP2981AI-XX(2)			LP2981I-XX(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage(4)	High = O/P ON		1.4			1.4		V
		High = O/P ON –40°C ≤ T_J ≤ 125°C	1.6			1.6			
		Low = O/P OFF	0.5			0.5			
		Low = O/P OFF –40°C ≤ T_J ≤ 125°C			0.15			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0 V		0.01			0.01		µA
		$V_{ON/\overline{OFF}}$ = 0 V –40°C ≤ T_J ≤ 125°C			–1			–1	
		$V_{ON/\overline{OFF}}$ = 5 V		5			5		
		$V_{ON/\overline{OFF}}$ = 5 V –40°C ≤ T_J ≤ 125°C			15			15	
$I_{O(PK)}$	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ − 5%	150	400			150		mA

(4) The ON/$\overline{OFF}$ inputs must be properly driven to prevent misoperation. For details, see *Operation With ON/$\overline{OFF}$ Control*.

Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 1 mA, C_{OUT} = 1 µF, $V_{ON/\overline{OFF}}$ = 2 V.(1)

PARAMETER		TEST CONDITIONS	LP2981AI-XX(2)			LP2981I-XX(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz C_{OUT} = 10 µF		160			160		µV
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{OUT} = 10 µF		63			63		dB
$I_{O(MAX)}$	Short-circuit current	R_L = 0 Ω (steady state)(5)		150			150		mA

(5) See related curve(s) in *Typical Characteristics* section.

6.6 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

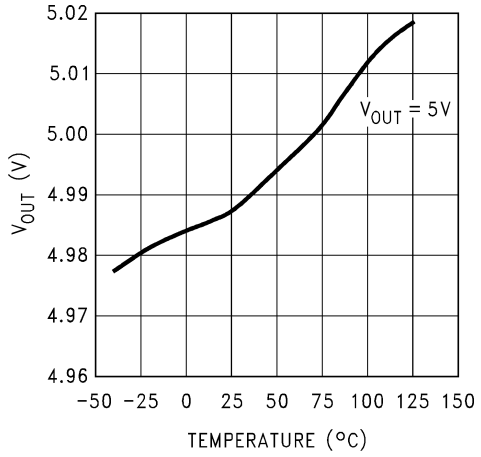


Figure 1. 5-V Output Voltage vs Temperature

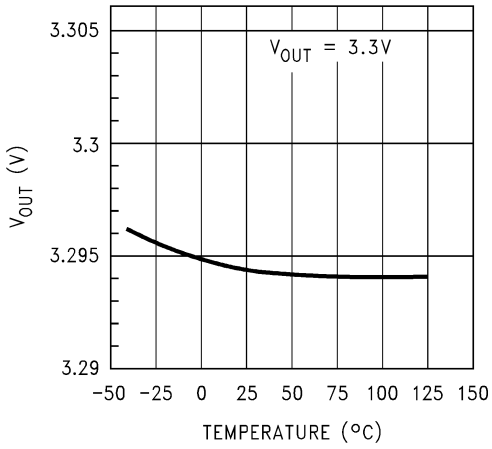


Figure 2. 3.3-V Output Voltage vs Temperature

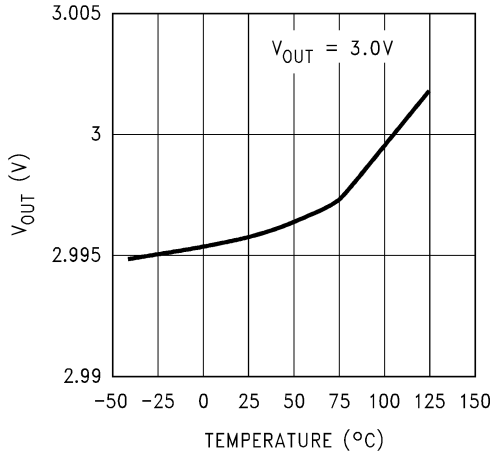


Figure 3. 3-V Output Voltage vs Temperature

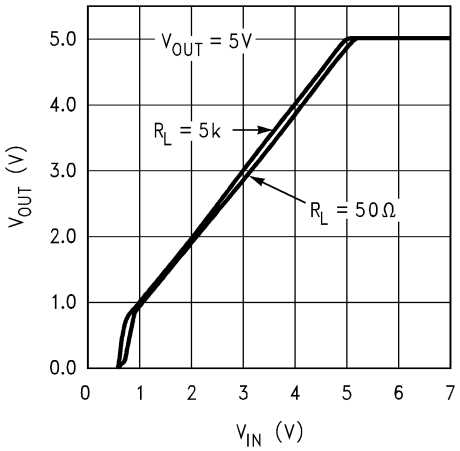


Figure 4. 5-V Dropout Characteristics

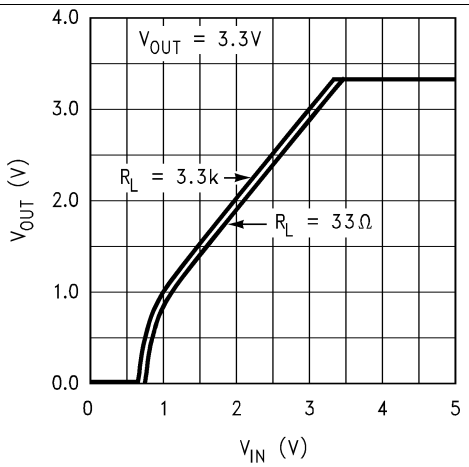


Figure 5. 3.3-V Dropout Characteristics

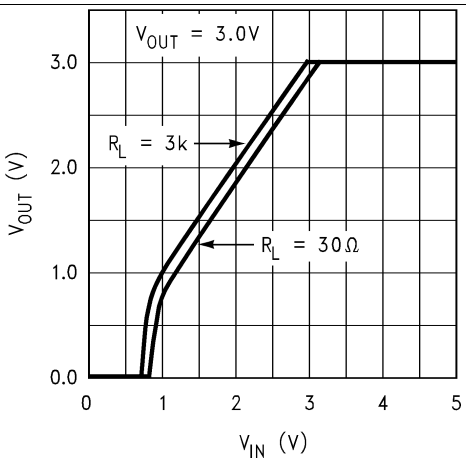


Figure 6. 3-V Dropout Characteristics

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

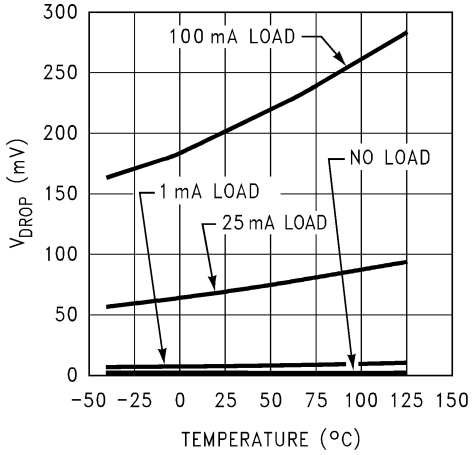


Figure 7. Dropout Voltage vs Temperature

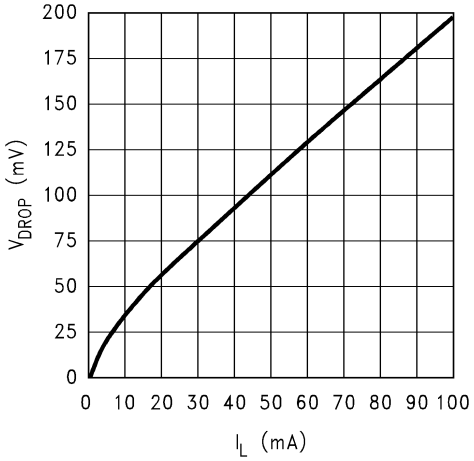


Figure 8. Dropout Voltage vs Load Current

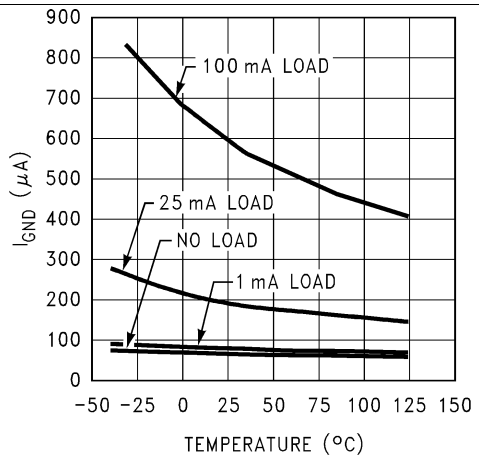


Figure 9. Ground Pin Current vs Temperature

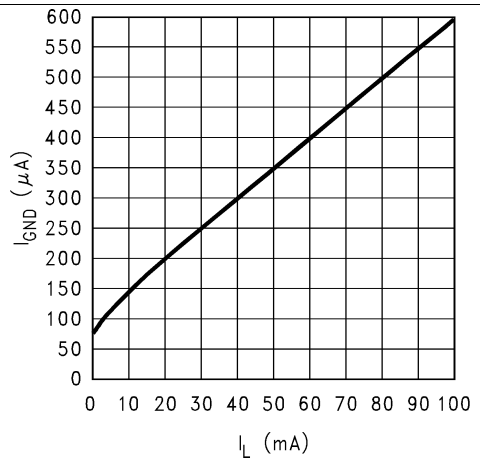


Figure 10. Ground Pin Current vs Load Current

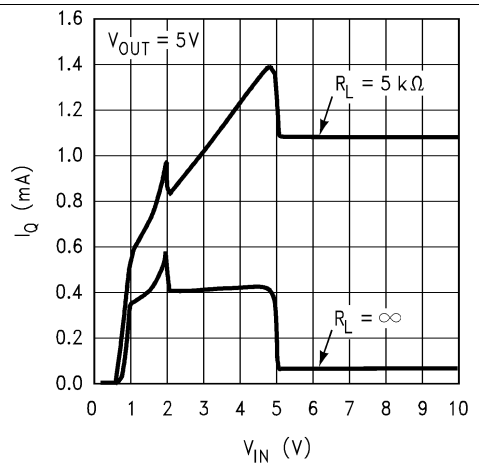


Figure 11. Input Current vs V_{IN}

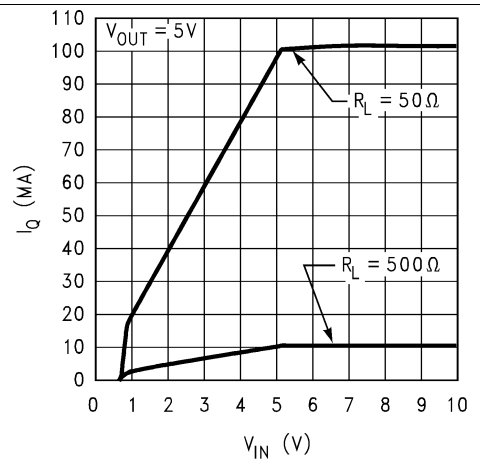


Figure 12. Input Current vs V_{IN}

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

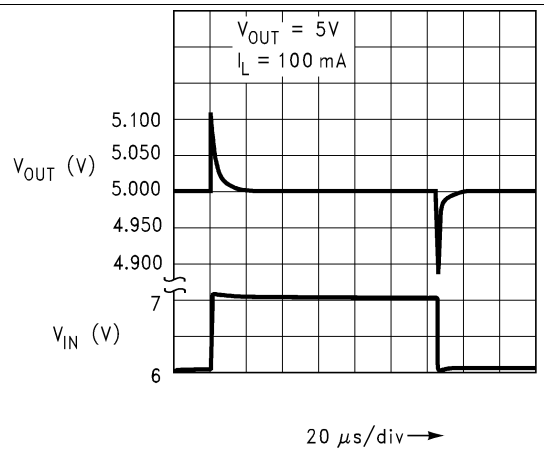


Figure 13. Line Transient Response

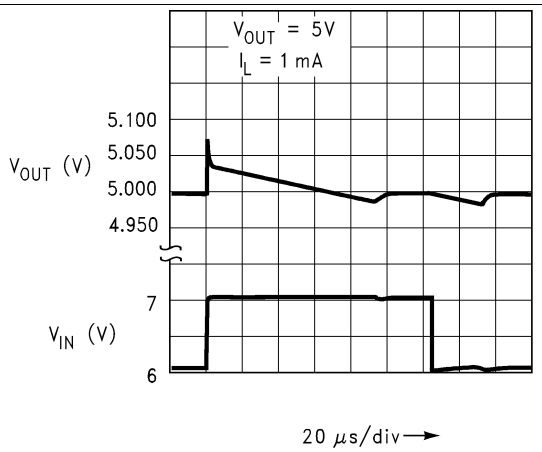


Figure 14. Line Transient Response

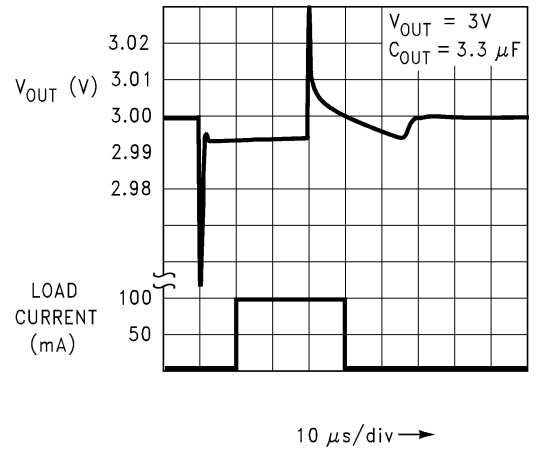


Figure 15. Load Transient Response

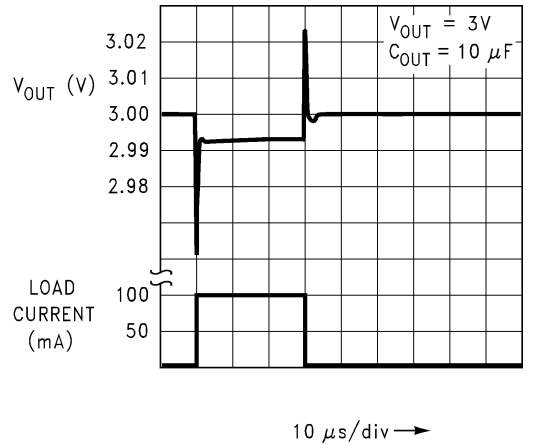


Figure 16. Load Transient Response

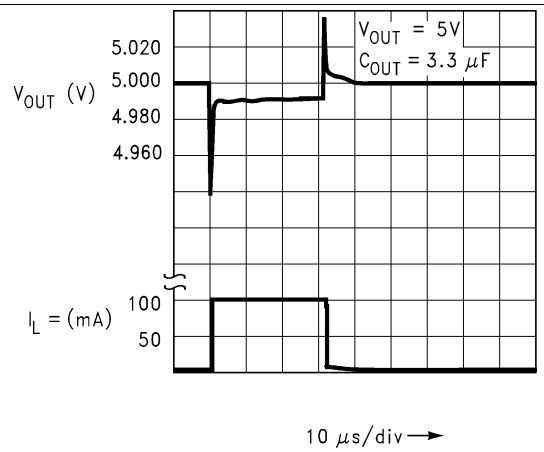


Figure 17. Load Transient Response

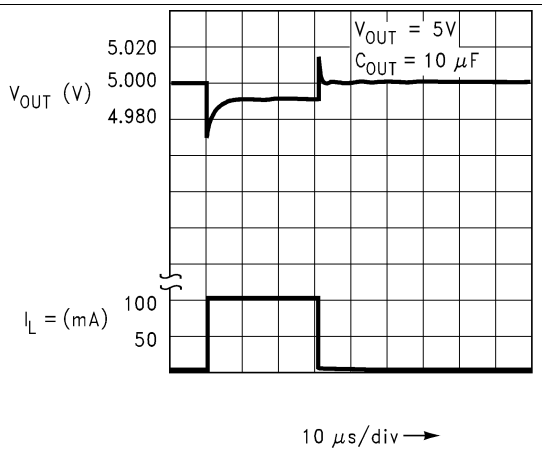


Figure 18. Load Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

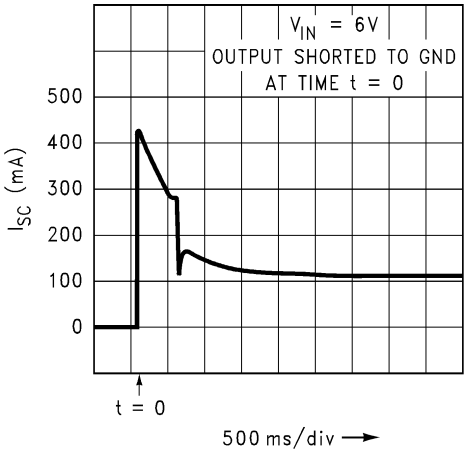


Figure 19. Short-Circuit Current

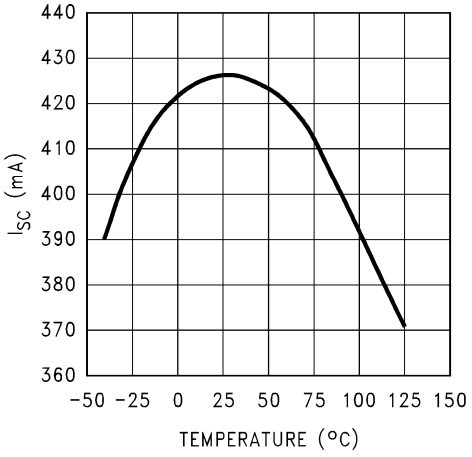


Figure 20. Instantaneous Short Circuit Current vs Temperature

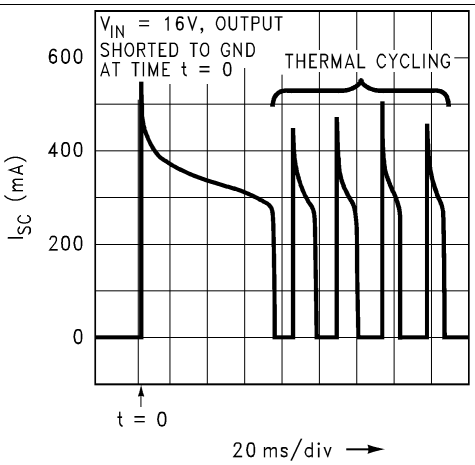


Figure 21. Short-Circuit Current

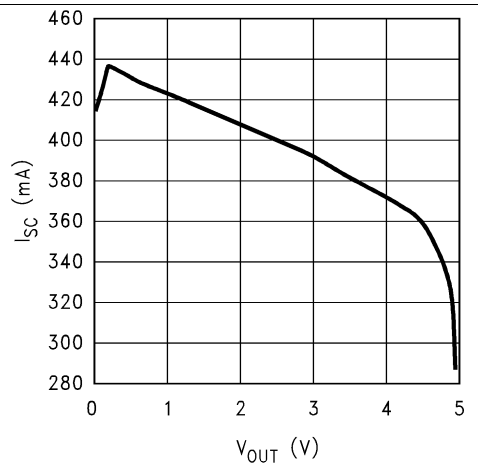


Figure 22. Instantaneous Short-Circuit Current vs Output Voltage

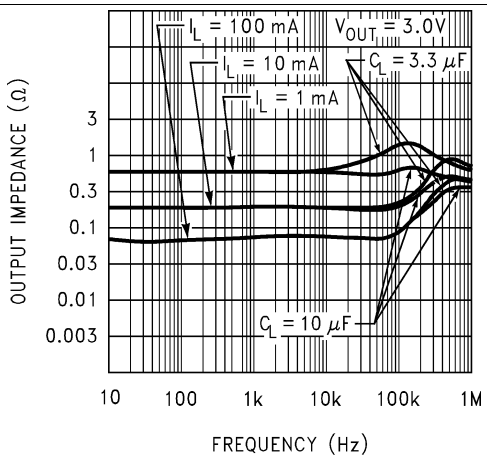


Figure 23. Output Impedance vs Frequency

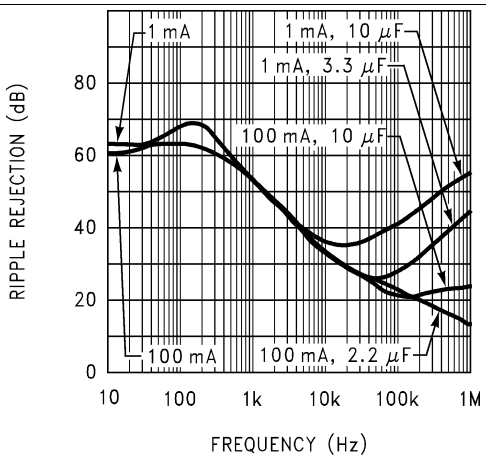


Figure 24. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

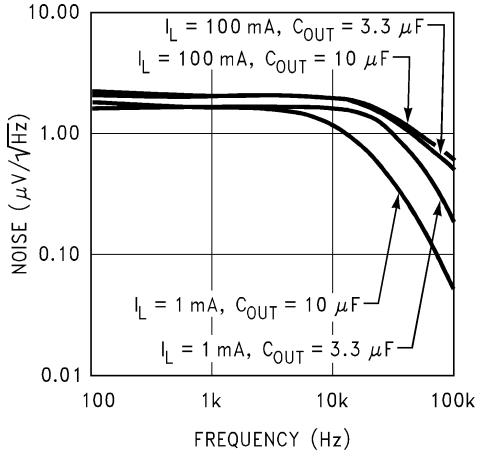


Figure 25. Output Noise Density

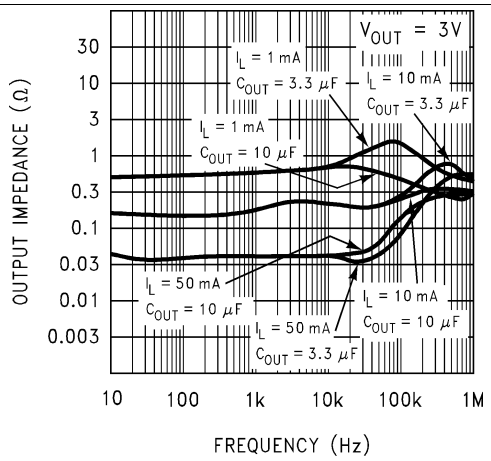


Figure 26. Output Impedance vs Frequency

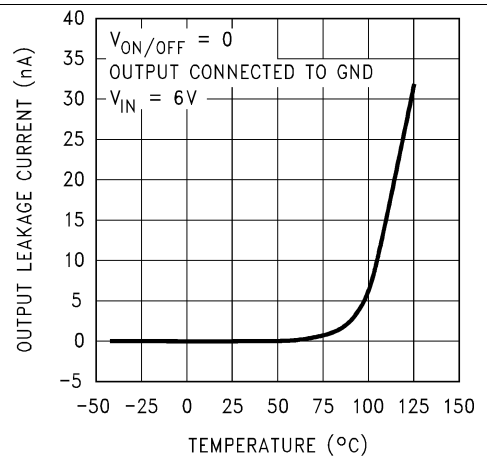


Figure 27. Input-to-Output Leakage vs Temperature

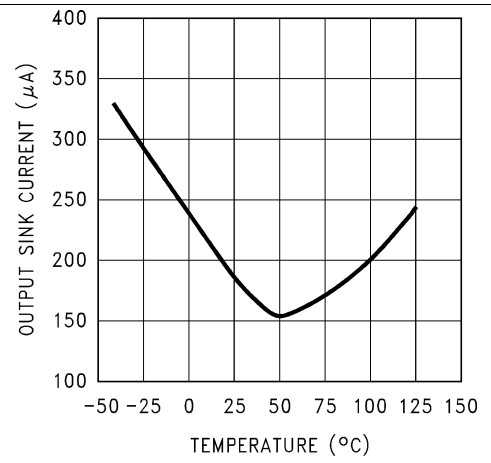


Figure 28. Output Reverse Leakage vs Temperature

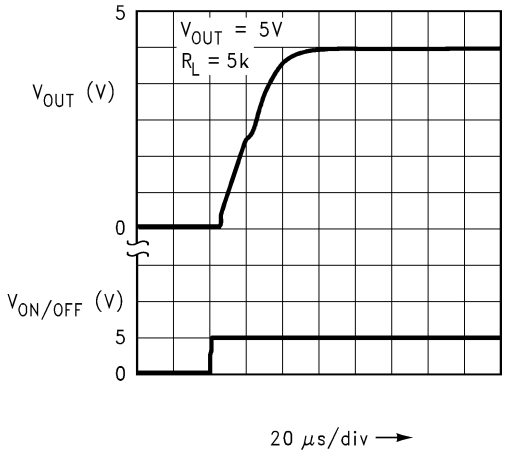


Figure 29. Turnon Waveform

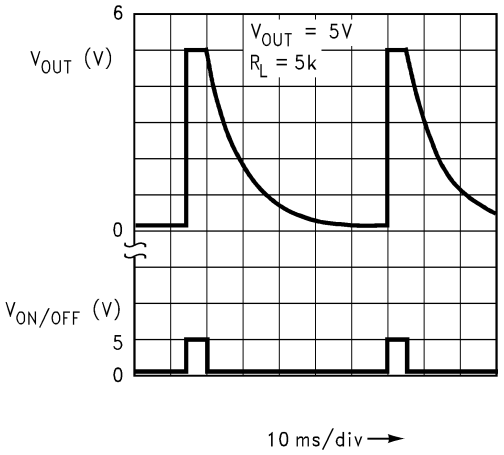


Figure 30. Turnoff Waveform

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF all voltage options, ON/$\overline{OFF}$ pin tied to V_{IN}.

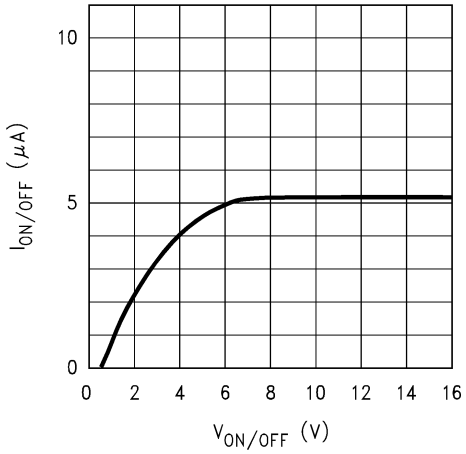


Figure 31. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$

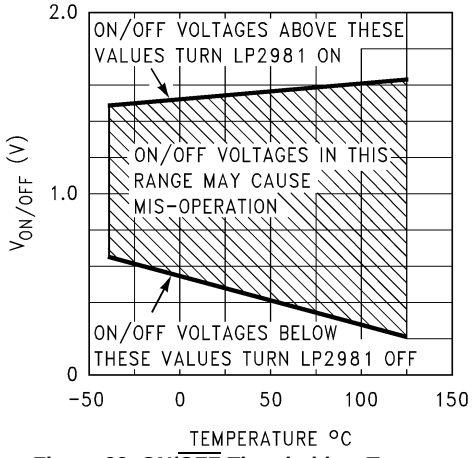


Figure 32. ON/$\overline{OFF}$ Threshold vs Temperature

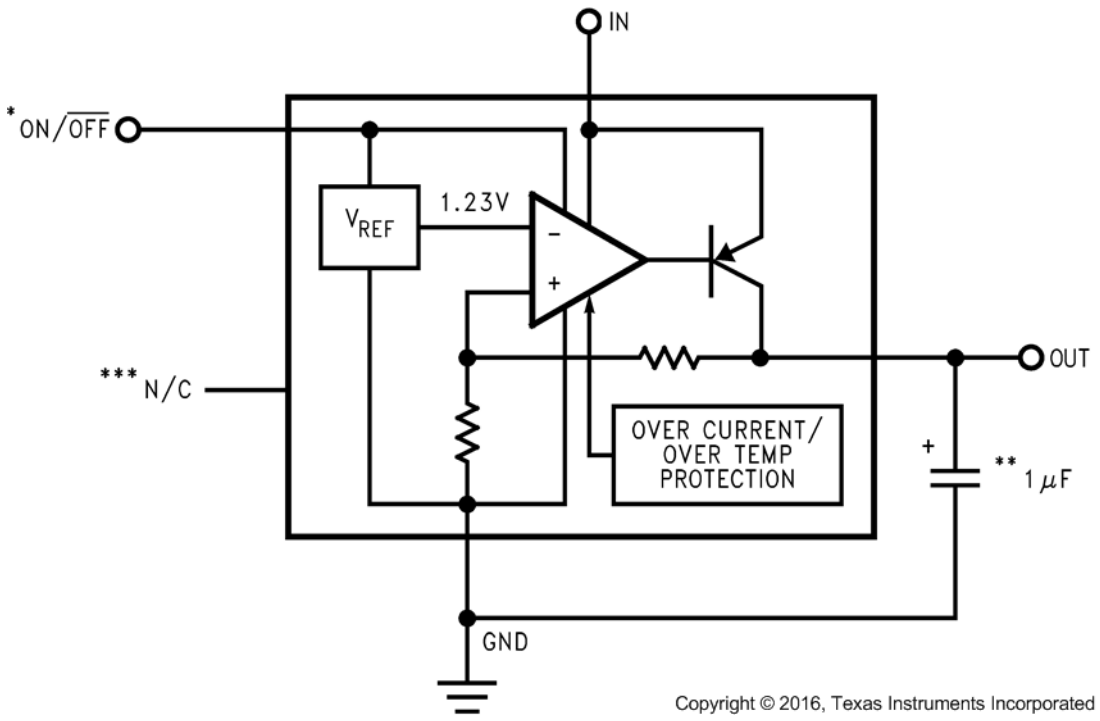
7 Detailed Description

7.1 Overview

The LP2981-N is a 100-mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications. Available in assorted output voltages from 2.5 V to 5 V, the device has an output tolerance of 0.75% for the A grade (1.25% for the non-A version). Using a VIP process, the LP2981-N contains these features to facilitate battery-powered designs:

- Fixed 5-V, 3.6-V, 3.3-V, 3-V, and 2.5-V output versions
- Very high-accuracy 1.23-V reference
- Low-dropout voltage, typical dropout of 200 mV at 100-mA load current and 7 mV at 1-mA load
- Low ground current, typically 600 µA at 100-mA load and 80 µA at 1-mA load
- A sleep mode feature is available, allowing the regulator to consume only 1 µA (typical) when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Overtemperature protection and overcurrent protection circuitry is designed to safeguard the device during unexpected conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiple Voltage Options

To meet the different application requirements, the LP2981-N provides multiple fixed output options from 2.5 V to 5 V.

7.3.2 High-Accuracy Output Voltage

With special careful design to minimize all contributions to the output voltage error, the LP2981-N distinguishes itself as a very high-accuracy output voltage micropower LDO. This includes a tight initial tolerance (0.75% typical), extremely good line regulation (0.007%/V typical), and a very low output voltage temperature coefficient, making the part an ideal low-power voltage reference.

Feature Description (continued)

7.3.3 Ultra-Low-Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage (VDO = V_{IN} – V_{OUT}), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. VDO indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary.

7.3.4 Low Ground Current

LP2981-N uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 600 µA at 100-mA load and 80 µA at 1-mA load.

7.3.5 Sleep Mode

When pulling the ON/$\overline{\text{OFF}}$ pin to low level, LP2981-N will enter sleep mode, and less than 1-µA quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

7.3.6 Short-Circuit Protection (Current Limit)

The internal current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If OUT is forced below 0 V before EN goes high and the load current required exceeds the foldback current limit, the device may not start up correctly.

7.3.7 Thermal Protection

The LP2981-N contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced. The internal protection circuitry of the LM2981-N is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

7.4 Device Functional Modes

7.4.1 Operation with $V_{OUT(TARGET)}$ + 1 V ≤ V_{IN} < 16 V

The device operates if the input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 0.6 V. At input voltages below the minimum V_{IN} requirement, the device does not operate correctly and output voltage may not reach target value.

7.4.2 Operation With ON/$\overline{\text{OFF}}$ Control

If the voltage on the ON/$\overline{\text{OFF}}$ pin is less than 0.15 V, the device is disabled, and the shutdown current does not exceed 1 µA. Raising ON/$\overline{\text{OFF}}$ above 1.4 V initiates the start-up sequence of the device.

8 Application and Implementation

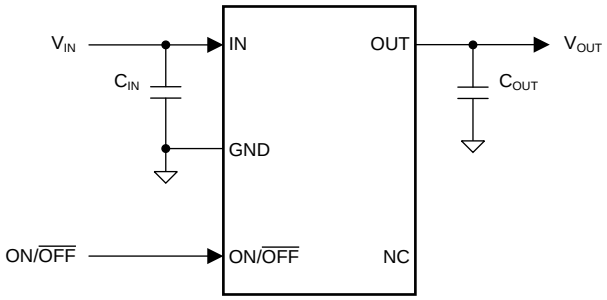
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP2981-N is a linear voltage regulator operating from 2.1 V to 16 V on the input and regulates voltages between 2.5 V to 5 V with 0.75% accuracy and 100-mA maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2981-N is a linear voltage regulator. To achieve high efficiency, the dropout voltage ($V_{IN} – V_{OUT}$) must be as small as possible, thus requiring a very-low-dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

8.2 Typical Application



*ON/$\overline{OFF}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used.
**Minimum output capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance and additional stability margin (see *Capacitor Characteristics*).
***Do not make connections to this pin.

Figure 33. LP2981-N Typical Application

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V ±10%, provided by the DC-DC converter switching at 1 MHz
Output voltage	3.3 V ±5%
Output current	100 mA (maximum), 1 mA (minimum)
RMS noise, 300 Hz to 50 kHz	< 1 mV_{RMS}
PSRR at 1 kHz	> 40 dB

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the external capacitors used with the LP2981-N must be carefully selected to assure regulator loop stability.

8.2.2.1.1 Input Capacitor

An input capacitor with a value ≥ 1 µF is required with the LP2981-N (amount of capacitance can be increased without limit).

This capacitor must be located a distance of not more than 0.5 inches from the input pin of the LP2981-N and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.

8.2.2.1.2 Output Capacitor

The output capacitor must meet both the requirement for minimum amount of capacitance and equivalent series resistance (ESR) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (refer to Figure 36, Figure 37, Figure 38, and Figure 39).

NOTE

Important: The output capacitor must maintain its ESR in the stable region over the full operating temperature range to ensure stability. Also, capacitor tolerance and variation with temperature must be considered to ensure the minimum amount of capacitance is provided at all times.

This capacitor should be located not more than 0.5 inches from the OUT pin of the LP2981-N and returned to a clean analog ground.

8.2.2.2 Capacitor Characteristics

8.2.2.2.1 Tantalum

Tantalum capacitors are the best choice for use with the LP2981-N. Most good quality tantalums can be used with the LP2981-N, but check the manufacturer's data sheet to be sure the ESR is in range.

It is important to remember that ESR increases at lower temperatures and a capacitor that is near the upper limit for stability at room temperature can cause instability when it gets cold.

In applications which must operate at very low temperatures, it may be necessary to parallel the output tantalum capacitor with a ceramic capacitor to prevent the ESR from going up too high (see below for important information on ceramic capacitors).

8.2.2.2.2 Ceramic

Ceramic capacitors are not recommended for use at the output of the LP2981-N. This is because the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2981-N. A 2.2-µF ceramic was measured and found to have an ESR of about 15 mΩ, which is low enough to cause oscillations.

If a ceramic capacitor is used on the output, a 1-Ω resistor should be placed in series with the capacitor.

8.2.2.2.3 Aluminum

Because of large physical size, aluminum electrolytics are not typically used with the LP2981-N. They must meet the same ESR requirements over the operating temperature range, more difficult because of their steep increase at cold temperature.

An aluminum electrolytic can exhibit an ESR increase of as much as 50x when going from 20°C to −40°C. Also, some aluminum electrolytics are not operational below −25°C because the electrolyte can freeze.

8.2.2.3 Reverse Current Path

The internal PNP power transistor used as the pass element in the LP2981-N has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse biased (See Figure 34).

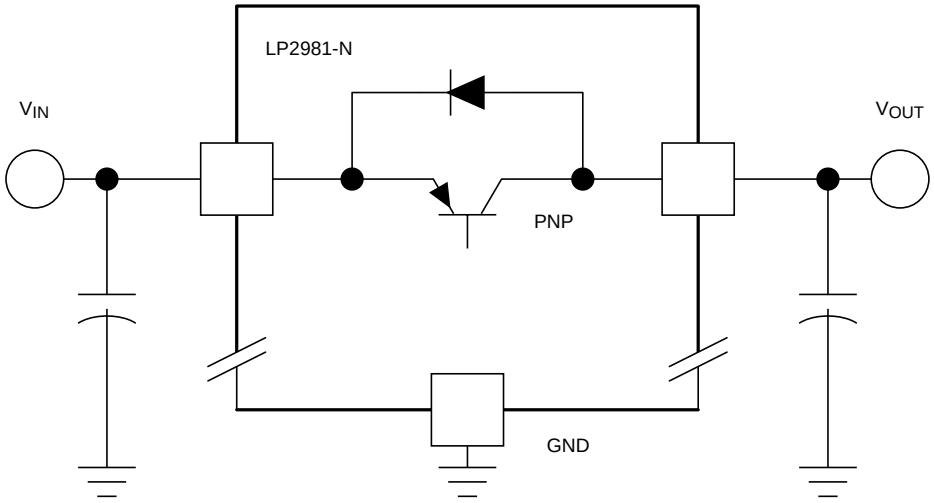


Figure 34. LP2981-N Reverse Current Path

However, if the input voltage is more than a V_{BE} below the output voltage, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into the V_{IN} pin and out the ground pin, which can damage the part.

The internal diode can also be turned on if the input voltage is abruptly stepped down to a voltage which is a V_{BE} below the output voltage.

In any application where the output voltage may be higher than the input voltage, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}; see Figure 35), to limit the reverse voltage across the LP2981-N to 0.3 V (see *Absolute Maximum Ratings*).

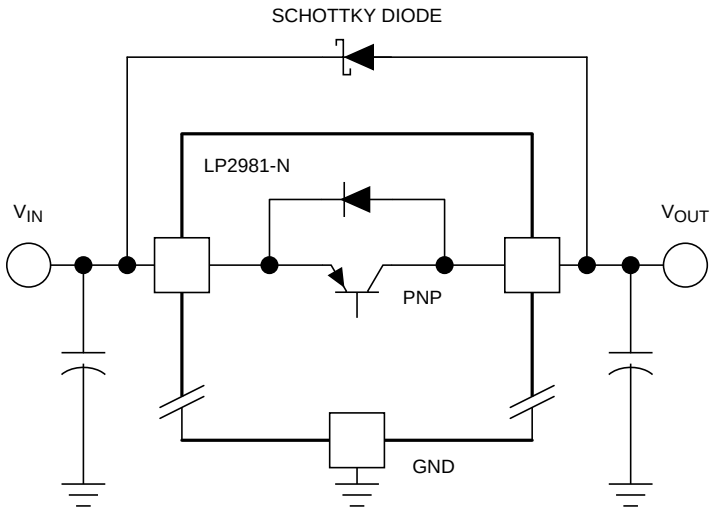


Figure 35. Adding External Schottky Diode Protection

8.2.2.4 ON and $\overline{OFF}$ Input Operation

The LP2981-N is shut off by pulling the ON/$\overline{OFF}$ input low, and turned on by driving the input high. If this feature is not to be used, the ON/$\overline{OFF}$ input should be tied to V_{IN} to keep the regulator on at all times (the ON/$\overline{OFF}$ input must **not** be left floating).

To ensure proper operation, the signal source used to drive the ON/$\overline{OFF}$ input must be able to swing above and below the specified turnon/turnoff voltage thresholds which specify an ON or $\overline{OFF}$ state (see *Electrical Characteristics*).

The ON/$\overline{\text{OFF}}$ signal may come from either a totem-pole output, or an open-collector output with pullup resistor to the LP2981-N input voltage or another logic supply. The high-level voltage may exceed the LP2981-N input voltage, but must remain within the *Absolute Maximum Ratings* for the ON/$\overline{\text{OFF}}$ pin.

It is also important that the turnon/turnoff voltage signals applied to the ON/$\overline{\text{OFF}}$ input have a slew rate which is greater than 40 mV/µs.

NOTE

IMPORTANT: The regulator shutdown function will not operate correctly if a slow-moving signal is applied to the ON/$\overline{\text{OFF}}$ input.

8.2.3 Application Curves

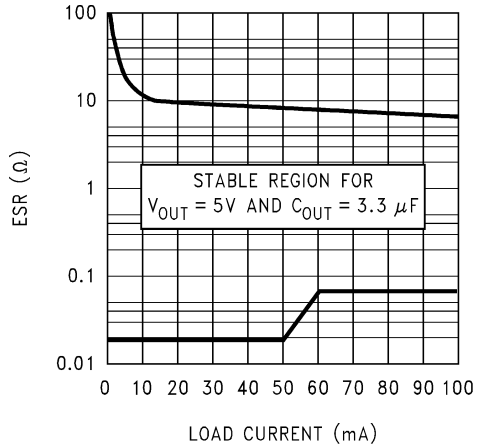


Figure 36. 5-V, 3.3-µF ESR Curves

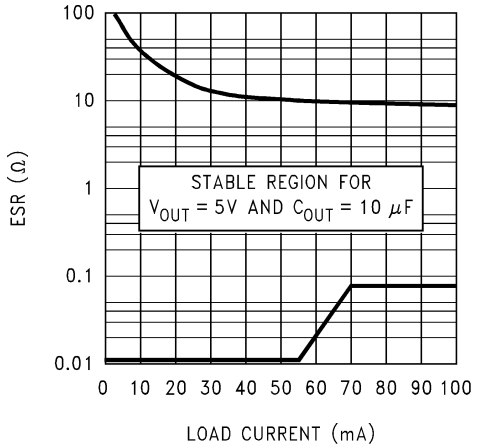


Figure 37. 5-V, 10-µF ESR Curves

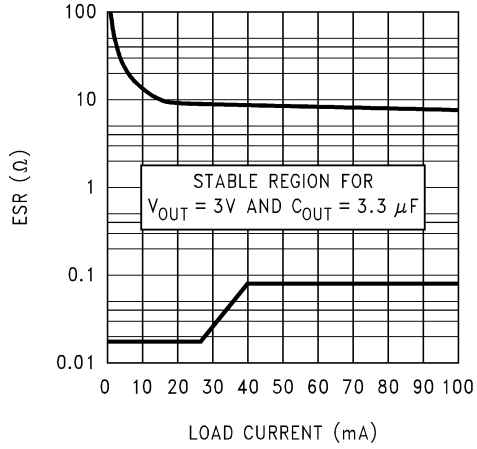


Figure 38. 3-V, 3.3-µF ESR Curves

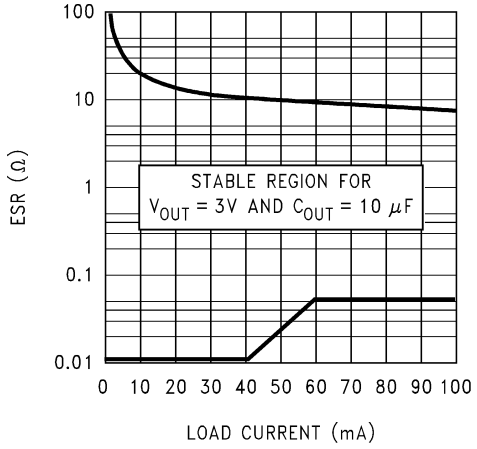


Figure 39. 3-V, 10-µF ESR Curves

9 Power Supply Recommendations

The LP2981-N is designed to operate from an input voltage supply range between 2.1 V and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

10.2 Layout Example

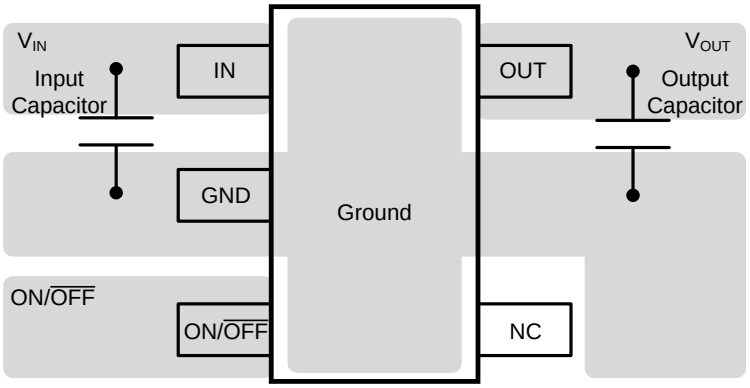


Figure 40. LP2981-N Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2981AIM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0CA	
LP2981AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CA	Samples
LP2981AIM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L05A	Samples
LP2981AIM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L04A	
LP2981AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L04A	Samples
LP2981AIM5-3.6/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0JA	Samples
LP2981AIM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L03A	
LP2981AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L03A	Samples
LP2981AIM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L05A	Samples
LP2981AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L04A	Samples
LP2981AIM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0JA	Samples
LP2981AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L03A	Samples
LP2981IM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L0CB	
LP2981IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0CB	Samples
LP2981IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L05B	Samples
LP2981IM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L04B	
LP2981IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L04B	Samples
LP2981IM5-3.6/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0JB	Samples
LP2981IM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	L03B	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2981IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L03B	Samples
LP2981IM5X-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L05B	Samples
LP2981IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L04B	Samples
LP2981IM5X-3.6/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L0JB	Samples
LP2981IM5X-5.0	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	L03B	
LP2981IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L03B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

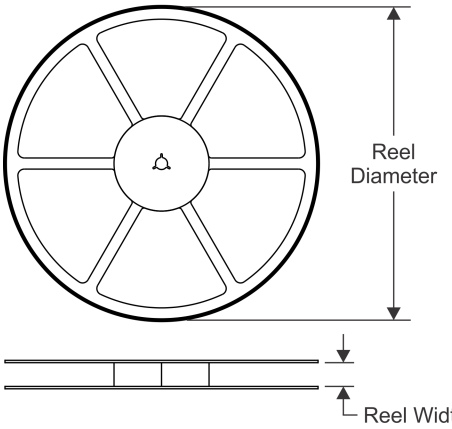
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

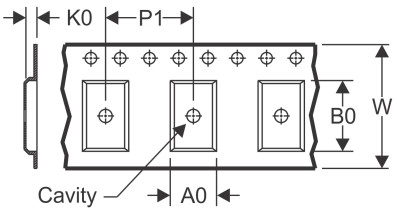
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

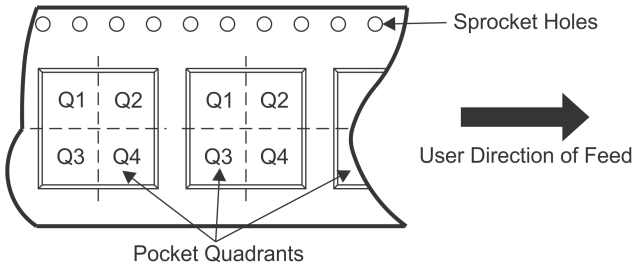


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

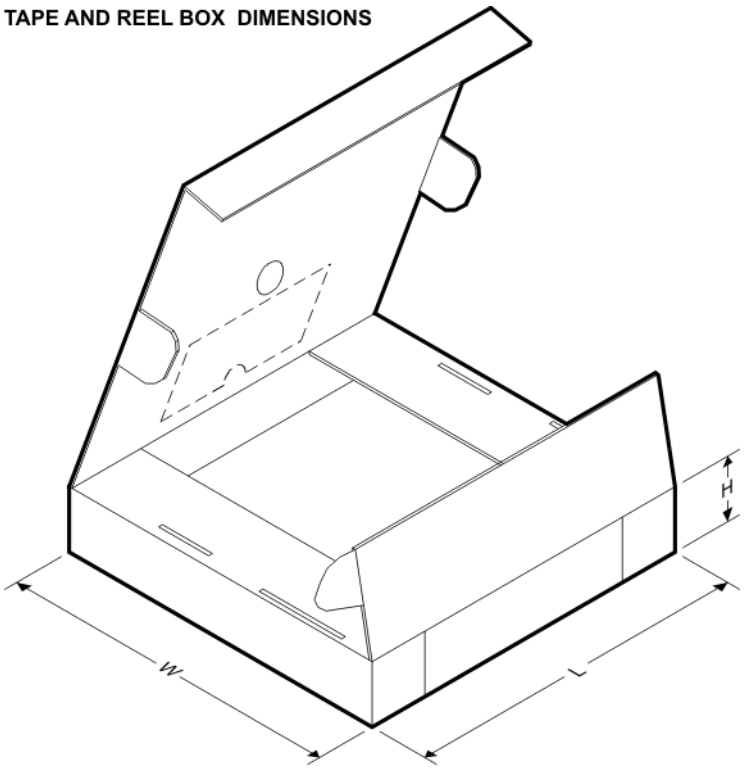


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2981AIM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2981IM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-5.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2981IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2981AIM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-3.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

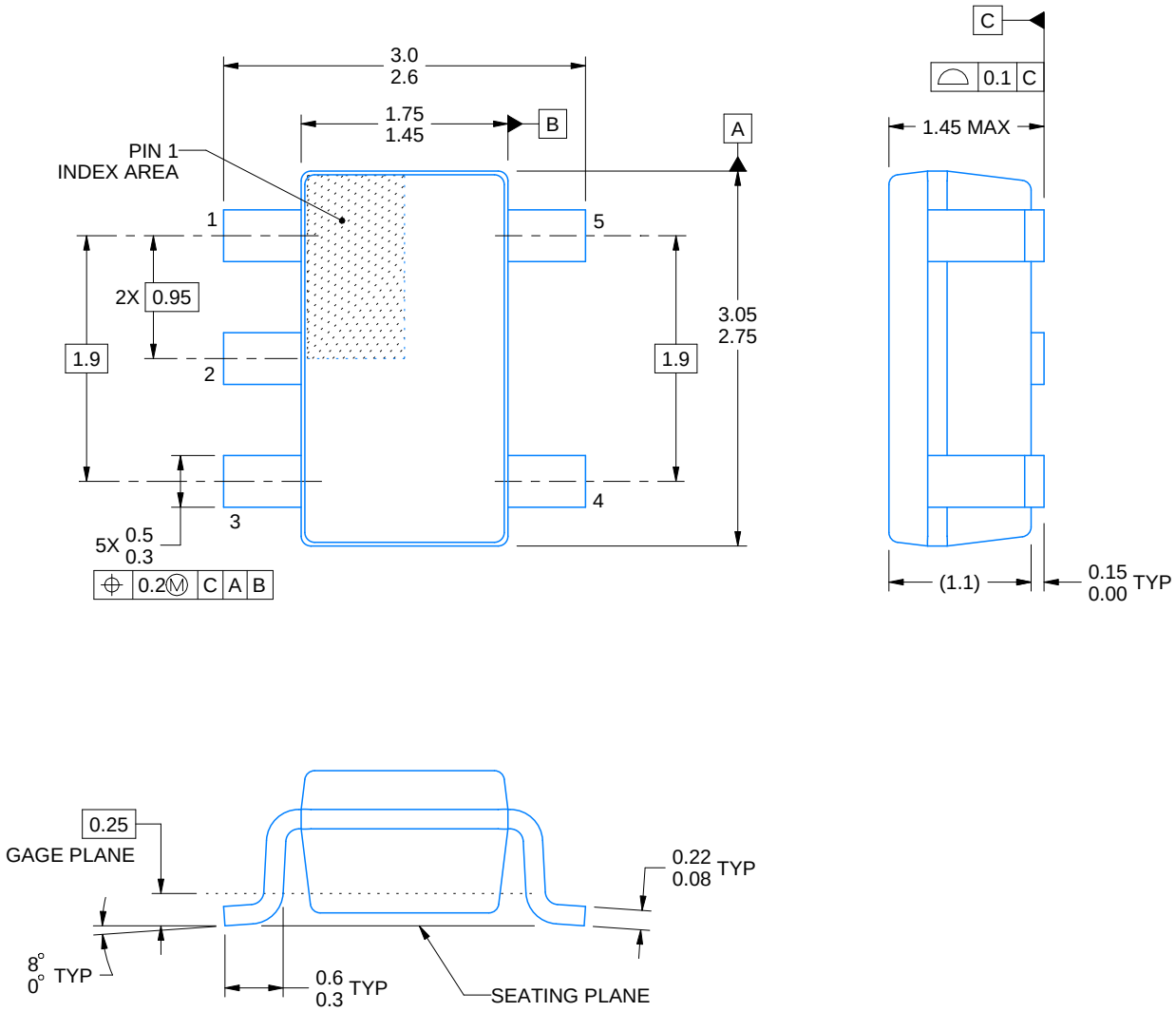
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2981AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981IM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-3.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2981IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981IM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981IM5X-5.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2981IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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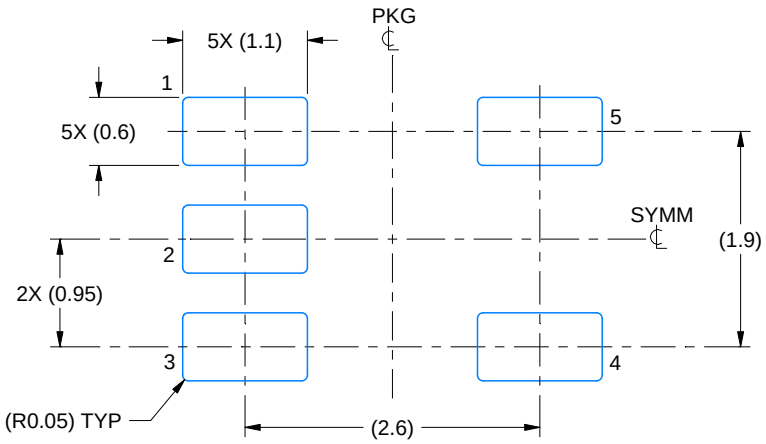
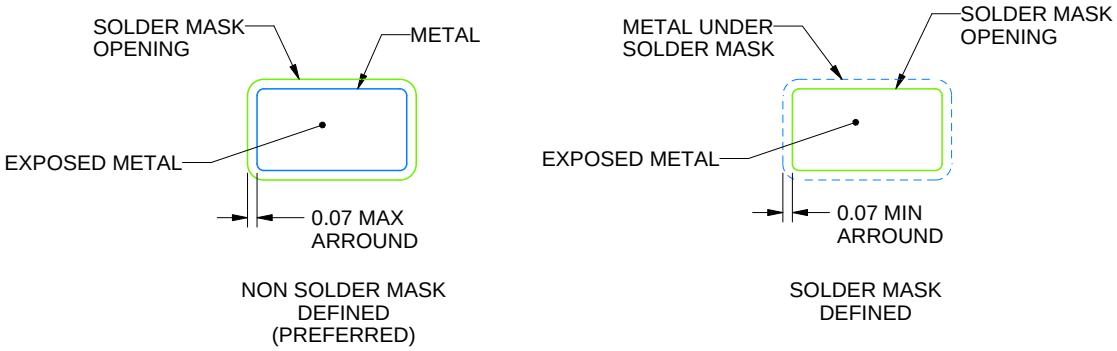
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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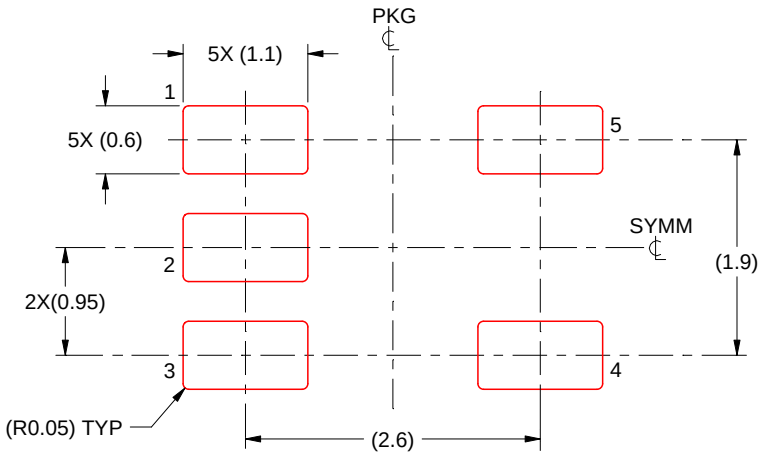
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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