

**Vishay Siliconix** 

# N-Channel 8 V (D-S) MOSFET

PRODU	CT SUMMARY		
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
	0.086 at $V_{GS}$ = 4.5 V	1.34 <sup>a</sup>	
8	0.093 at V <sub>GS</sub> = 2.5 V	1.29	7.1
0	0.102 at V <sub>GS</sub> = 1.8 V	1.23	7.1
	0.120 at V <sub>GS</sub> = 1.5 V	0.7	

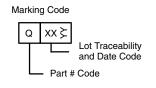
# SC-89 (6-LEADS)

### FEATURES

- Halogen-free According to IEC 61249-2-21
  Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

### **APPLICATIONS**

Load Switch for Portable Devices



Ordering Information: Si1050X-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATING	<b>S</b> (T <sub>A</sub> = 25 °C, un	less otherwise r	noted)		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	8	V	
Gate-Source Voltage		V <sub>GS</sub>	± 5	v	
Continuous Drain Current (T 150 °C)	T <sub>A</sub> = 25 °C		1.34 <sup>b, c</sup>		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C	D	1.07 <sup>b, c</sup>	A	
Pulsed Drain Current		I <sub>DM</sub>	6		
Continuous Source-Drain Diode Current	Diode Current T <sub>A</sub> = 25 °C		0.2 <sup>b, c</sup>		
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	0.236 <sup>b, c</sup>	w	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	'D	0.151 <sup>b, c</sup>	vv	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Manianan karatian ta Anthianth d	t ≤ 5 s	R <sub>thJA</sub>	440	530	°C/W		
Maximum Junction-to-Ambient <sup>b, d</sup>	Steady State	thJA ا	540	650	0/10		

Notes:

a. Based on  $T_C = 25$  °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. Maximum under steady state conditions is 650 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$	8			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		18.2			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	i <sub>D</sub> = 230 μA		- 2.55		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	0.35		0.9	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 5 V$			± 100	nA	
Zaus Cata Maltana Dusin Cumant	I <sub>DSS</sub>	$V_{DS} = 8 V, V_{GS} = 0 V$			1		
Zero Gate Voltage Drain Current		$V_{DS} = 8 V, V_{GS} = 0 V, T_{J} = 85 °C$			10	- μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = \ge 5 V, V_{GS} = 4.5 V$	6			A	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.34 A		0.071	0.086	Ω	
	P	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 1.29 A		0.078	0.093		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 1.23 A		0.085	0.102		
		V <sub>GS</sub> = 1.5 V, I <sub>D</sub> = 0.76 A		0.092	0.120		
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 4 V, I <sub>D</sub> = 1.34 A		4.12		S	
Dynamic <sup>b</sup>	-						
Input Capacitance	C <sub>iss</sub>			585		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 0 V, f = 1 MHz		190			
Reverse Transfer Capacitance	C <sub>rss</sub>			130			
·		V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1.34 A		7.7	11.6		
Total Gate Charge	Qg			7.1	10.7	nC	
Gate-Source Charge	Q <sub>qs</sub>	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.34 A		1.14			
Gate-Drain Charge	Q <sub>qd</sub>			1.69			
Gate Resistance	R <sub>a</sub>	f = 1 MHz	3.5		4.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			6.8	10.2		
Rise Time	t <sub>r</sub>	$V_{DD} = 4 V, R_1 = 3.6 \Omega$		35	53	- ns	
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 1.1 \text{ A}, V_{GEN} = 4.5 \text{ V}, \text{ R}_a = 1 \Omega$		25	37.5		
Fall Time	t <sub>f</sub>			6	9		
Drain-Source Body Diode Characterist	ics				I	L	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				6	А	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.0 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	~		18.5	28	nC	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			3.7	5.7	-	
Reverse Recovery Fall Time	t <sub>a</sub>	I <sub>F</sub> = 1.0 A, dI/dt = 100 A/μs		6.7		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			11.8			

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

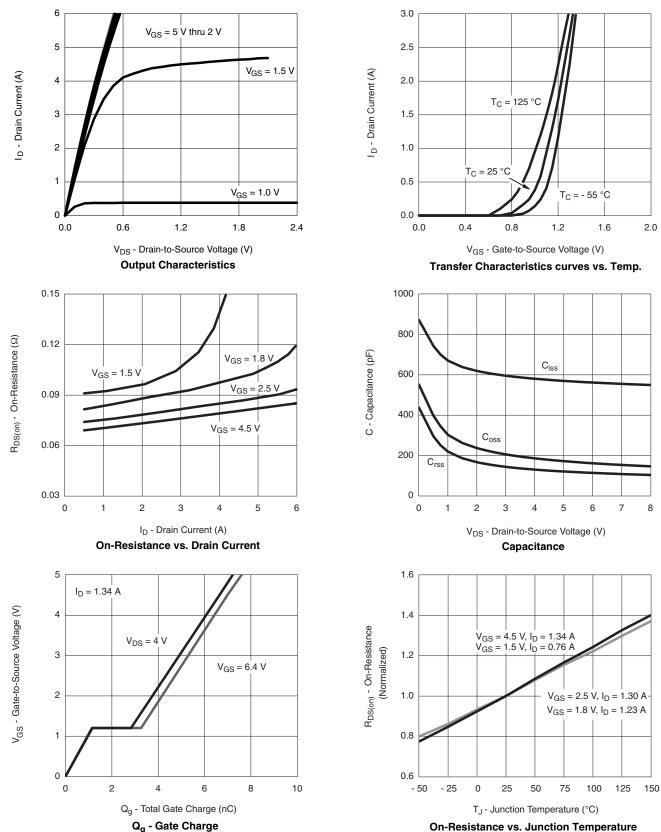
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# Si1050X Vishay Siliconix

### **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

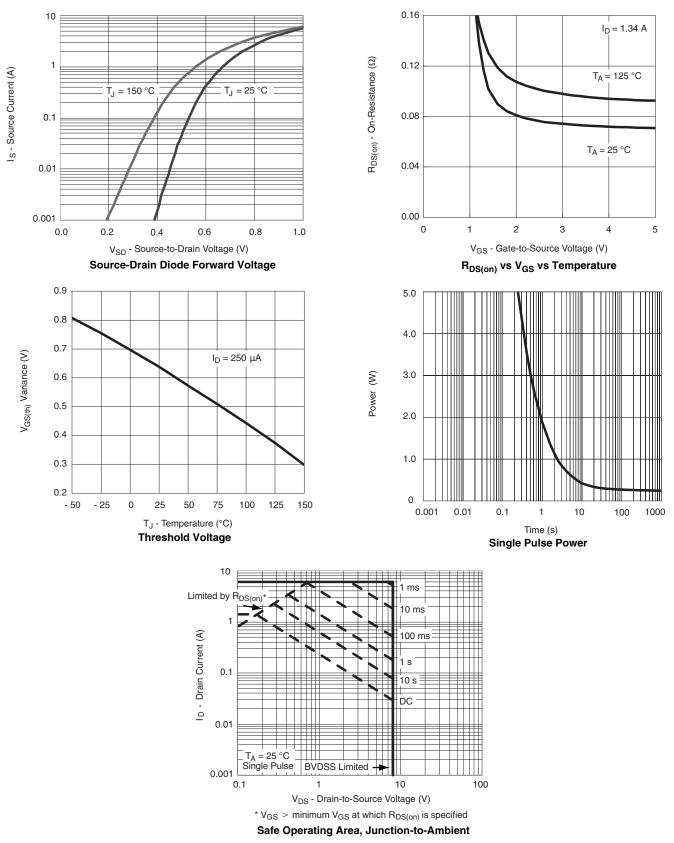


Document Number: 73896 S10-2544-Rev. D, 08-Nov-10

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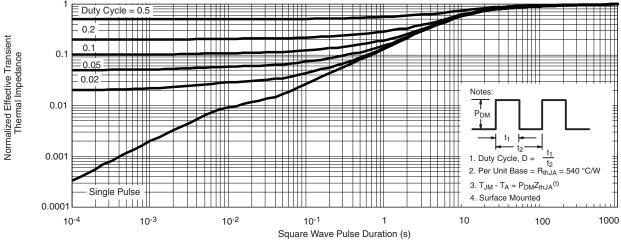


### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)





### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



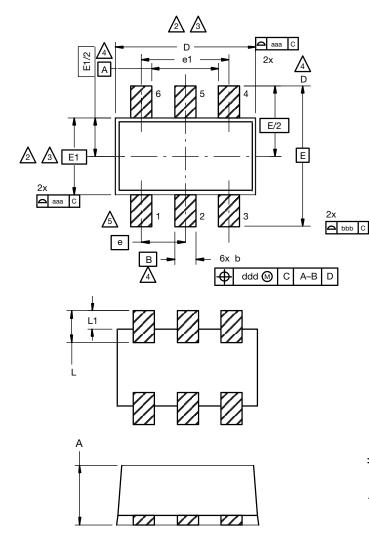
Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?73896</u>.



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### SC-89 6-Leads (SOT-563F)



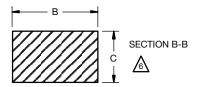
Notes

- 1. Dimensions in millimeters.
- Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

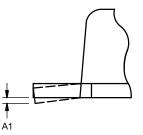
A Datums A, B and D to be determined 0.10 mm from the lead tip.

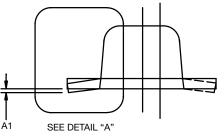
 $\triangle$  Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.









DIM.	MILLIMETERS				
	MIN.	NOM.	MAX.		
А	0.56	0.58	0.60		
A1	0	0.02	0.10		
b	0.15	0.22	0.30		
С	0.10	0.14	0.18		
D	1.50	1.60	1.70		
E	1.50	1.60	1.70		
E1	1.15	1.20	1.25		
е	0.45	0.50	0.55		
e1	0.95	1.00	1.05		
L	0.25	0.35	0.50		
L1	0.10	0.20	0.30		
C14-0439-Rev DWG: 5880	v. C, 11-Aug-14				

Revision: 11-Aug-14

1 For technical questions, contact: <u>analogswitchtechsupport@vishay.com</u> Document Number: 71612

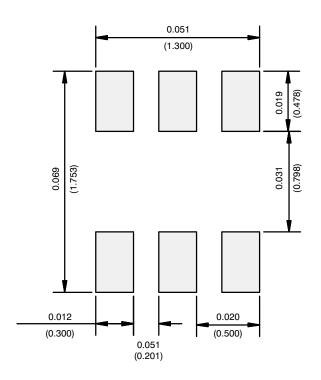
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# Application Note 826

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### **RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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